Electrical Compliance Test Specification
SuperSpeed Universal Serial Bus

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Revision: 1.0

Scope of this Revision

This revision of the specification describes the testing to be applied to hardware based on the Universal Serial Bus 3.0 Specification, revision 1.0.

Revision History

Revision	Issue Date	Comments
0.5	02/25/2009	For review only.
0.7	06/03/2009	For review only.
.9	09/10/2009	Complete draft of test algorithms.
.9RC1	9/15/2009	Final .9 draft release candidate after workgroup reviews.
1.0RC1	11/27/2013	Updates for all 3.0 ECNs and .9 testing learnings
1.0RC2	3/5/2014	Updates for compliance workgroup walkthrough review.
1.0RC3	4/2/2014	Final workgroup review updates. Workgroup approved as final.

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1 Introduction

This document provides the compliance criteria and test descriptions for SuperSpeed USB devices, hubs and host controllers that conform to the Universal Serial Bus 3.0 Specification, rev 1.0. It is relevant for anyone building SuperSpeed USB hardware. These criteria address the electrical requirements for a SuperSpeed physical layer design. Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

1.1 Related Documents

[1] Universal Serial Bus 3.0 Specification, revision 1.0, November 12, 2008

[2] USB 3.0 Super Speed Electrical Compliance Methodology, revision 0.5.

[3] Universal Serial Bus Specification, Revision 2.0, April 27, 2000.

[4] *USB-IF USB 2.0 Electrical Test Specification*, Version 1.03, January 2005.

1.2 USB 2.0 Compliance

USB 2,0 testing is required for USB 3.0 devices and is covered by a separate compliance testing program. Refer to [3] and [4] for details.

2 Test Descriptions

TD.1.1 Low Frequency Periodic Signaling TX Test.

This test verifies that the low frequency periodic signal transmitter meets the timing requirements when measured at the compliance test port.

Overview of Test Steps

1. The test performs the following steps. Connect the DUT to a simple breakout test fixture. Disconnect bus power if the DUT is a bus powered device.
2. Power on the device under test (connect bus powered if DUT is a bus powered device) and let it pass through the Rx.Detect state to the Polling.LFPS substate.
3. Trigger on the initial LFPS burst sent by the DUT and capture the first five bursts for analysis..
4. Measure the following LFPS parameters and compare against the USB 3.0 specification requirements: tburst, trepeat, tperiod, tRiseFall2080, Duty cycle, $V_{CM\text{-}AC\text{-}LFPS}$, and $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$. For these measurements the start of an LFPS burst is defined as starting when the absolute value of the differential voltage has exceeded 100 mV and the end of an LFPS burst is defined as when the absolute value of the differential voltage has been below 100 mV for 50 ns. tperiod, tRiseFall2080, Duty cycle, $V_{CM\text{-}AC\text{-}LFPS,}$ and $V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$ are only measured during the period from 100 nanoseconds after the burst start to 100 nanoseconds before the burst stop.

TD.1.2 Low Frequency Periodic Signaling RX Test.

This test verifies that the DUT low frequency periodic signal receiver recognizes LFPS signaling with voltage swings and duty cycles that are at the limits of what the specification allows. The link test specification includes test that vary additional LFPS parameters to test the LFPS receiver.

Overview of Test Steps

The test performs the following steps.

1. Connect the DUT to a simple breakout test fixture. Disconnect bus power if the DUT is a bus powered device.
2. Power on the device under test (connect bus powered if DUT is a bus powered device) and let it pass through the Rx.Detect state to the Polling.LFPS substate.
3. Trigger on the initial LFPS burst sent by the DUT and send LFPS signals to the DUT with the following parameters:
    a. tPeriod 50 ns.
    b. $V_{TX-DIFF-PP-LFPS}$ 800 mV.
    c. Duty Cycle 50%
4. The test passes if the device recognizes the LFPS and starts sending the TXEQ sequence.
5. The test is repeated with the following parameters:
    a. tPeriod 50 ns, $V_{TX-DIFF-PP-LFPS}$ 1200 mV, Duty Cycle 50%.
    b. tPeriod 50 ns, $V_{TX-DIFF-PP-LFPS}$ 1000 mV, Duty Cycle 40%.
    c. tPeriod 50 ns, $V_{TX-DIFF-PP-LFPS}$ 1000 mV, Duty Cycle 60%.

TD.1.3 Transmitted Eye Test

This test verifies that the transmitter meets the eye width, deterministic jitter and random jitter requirements when measured at the compliance test port with nominal transmitter equalization and after processing with the appropriate channels and post processing as shown in Table 2-1.

Connector Type	Channel	Reference Equalizer
Std-A	3m Cable + 5” PCB	Long Channel
Std-B	3m Cable + 11” PCB	Long Channel
Micro-B	1m Cable + 11” PCB	Long Channel
Micro-AB (Host Only)	1m Cable + 5” PCB	Long Channel
Micro-AB (DRD)	1m Cable + 11” PCB	Long Channel
Tethered (Standard A Plug)	11” PCB	Long Channel
All Types	No Channel (fixture only)	Short Channel

Table 2-1 Channels and Reference Equalizer for Testing Device Types

Note: Refer to USB.ORG for s-parameter files for embedding the long channels when using breakout fixtures.

In order to comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Overview of Test Steps

The test runs in the Polling.Compliance substate, and performs the following steps.

1. Connect the DUT to a simple break-out test fixture without VBUS supplied.

2. Power on the device under test and apply VBUS if the DUT is not a host, let it pass through the Rx.Detect state to the Compliance state. SSC shall be enabled.
3. Transmit the CP0 compliance pattern on the SuperSpeed USB port under test and capture the transmitted waveform on a high speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps in a single scope capture.
4. Send a PING.LFPS to the RX port of the device under test to cause the compliance pattern to transition to CP1. A single PING.LFPS burst is sent with the following parameters:
    a. 100 nanosecond duration.
    b. 20 Mhz frequency (2 periods).
5. Transmit the CP1 compliance pattern on the SuperSpeed USB port under test and capture the transmitted waveform on a high speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps in a single scope capture.
6. The required compliance channel shown in Table 2-1 for the connector type under test is embedded to the measured CP0 and CP1 data.

The following analysis in steps 7-9 is done applying the appropriate equalizer shown in Table 2-1 and JTF in the waveform analysis.

7. Compute the data eye using CP0 and compare it against the normative transmitter specifications contained in table 6-12 of the USB 3.0 specification.
8. Compute Rj using the CP1 data and compare it against the normative transmitter specifications contained in table 6-12 of the USB 3.0 specification.
9. Compute the total jitter at 10^{-12} BER using the CP0 data to compute a measured Tj and the Rj value from CP1 with the dual dirac method and compare it against the normative transmitter specification contained in table 6-12 of the USB 3.0 specification.

Note: Extrapolate Tj E-12 based on Tj measured with CP0 and CP1 Rj only.

10. Repeat the analysis in steps 7-9 for the short channel and reference equalizer shown in Table 2-1.

TD.1.4 Transmitted SSC Profile Test

This test verifies that the transmitter meets SSC profile requirements when measured at the compliance test port with -3.5dB of transmitter equalization and after processing with the JTF.

In order to comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Note: A PCI Express host adaptor is tested in a system that provides a 100 Mhz PCI Express reference clock with a valid SSC profile and in a system with a 100 Mhz PCI Express reference clock that does not have SSC. The host adaptor must pass all tests in both cases.

No transmitter testing is done with multiple downstream ports active on hosts/hubs.

Overview of Test Steps

The test runs in the Polling.Compliance substate, and performs the following steps.

1. Connect the DUT to a simple break-out test fixture.
2. Power on the device under test, let it pass through the Rx.Detect state to the Polling.Compliance substate.
3. Send a PING.LFPS to the RX port of the device under test to cause the compliance pattern to transition to CP1.

4. Transmit the CP1 compliance pattern on the SuperSpeed USB port under test and capture the transmitted waveform on a high speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps in a single scope capture.
5. The CP1 waveform is used to analyze that the slew rate (derivative) of the period jitter after applying the CDR filter does not exceed $T_{CDR\_SLEW\_MAX}$ at any point in any of the captured SSC cyles.
6. The CP1 waveform is used to test that $t_{SSC\text{-}MOD\text{-}RATE}$ and $t_{SSC\text{-}FREQ\text{-}DEVIATION}$ meet the USB 3.0 specification for each SSC cycle. $t_{SSC\text{-}FREQ\text{-}DEVIATION}$ must vary between one of the following two ranges:
    a. +300/-300 and -3700/-5300 PPM
    b. 1700/-2300 and -3700/-5300 PPM

TD.1.5 Receiver Jitter Tolerance Test

This test verifies that the receiver properly functions in the presence of deterministic and random jitter at multiple frequencies. The jitter characteristics are defined by the USB 3.0 specification. In order to reduce test time, the receiver is tested to a bit error ratio (BER) of 10^{-10}. In order to comprehend noise effects, such as crosstalk, it is up to the component manufacturer to make sure that any other links are active for the DUT.

The receiver test is performed with asynchronous SSC clocks in the test system and the device under test. The test system SSC shall be triangular at the maximum specified SSC frequency (33 Khz) and downspread 5000 ppm. The test system SSC shall meet the specification limits on slew rate.

Note: When the DUT is in loopback for this test it shall not exit loopback unless it receives a warm reset or an LFPS Exit Handshake.

Note: The test procedures for channels involving a 1 meter Micro-A to Micro-B cable assume the cable is selected to have a well-controlled nominal loss of 3.5 DB at 2.5 GHz.

Connector Type	Calibration Channel (Using breakout fixture to measure at end of channel)	Test Channel
Std-A	3m Cable + 5” PCB	3m Cable + 5” PCB
Std-B	3m Cable + 11” PCB	3m Cable + 11” PCB
Micro-B	3m Cable + 11” PCB	1m Cable + 11” PCB
Micro-AB (Host Only)	3m Cable + 5” PCB	1m Cable + 5” PCB + Micro-A to Std-A Receptacle adapter
Micro-AB (DRD)	3m Cable + 11” PCB	3m Cable + 11” PCB + Std-A to Micro-B adapter
Tethered (Standard A Plug)	3m Cable + 11” PCB	8” (short) Std-A to Std-B cable + 11” PCB
All Connector Types Must Also Perform Short Channel Test	Same as above (Either 3m Cable + 5” PCB or 3m Cable + 11” PCB) depending on connector type	Breakout Fixture Only

Note: Refer to http://www.usb.org/developers/estoreinfo/SuperSpeedTestTopologies.pdf

Overview of Test Steps

The test runs in the Polling.Loopback substate, and performs the following steps.

1. Calibrate swing and de-emphasis
    a. Connect the end of the cables that will connect to the SMAs on the test fixture (as directly as possible) to a real time oscilloscope and the other end to the test equipment generator.
    b. Calibrate the differential amplitude of the measured signal to 800 mV peak to peak.
    c. Calibrate the measured de-emphasis to 3.0 + 0.3/-0 dB fixed de-emphasis.

Note: The signal source must support full bit de-emphasis.

2. Connect the calibration channel to the signal source.

Calibrate Rj (2.42 +/- 10% ps RMS/30.8 +/- 10% ps peak to peak at a BER of 10^{-10}) with clock pattern (CP1). Calibrate at the end of the channel applying the CTLE and JTF. SSC and all other noise sources are off for this step.

Calibrate Sj (40.0 ps +0/-10% at 50 MHz) with CP0. Calibrate at the end of the channel applying only CTLE. SSC is off for this step. (Calibration is done by testing measured maximum peak to peak jitter without extrapolation (measured TJ) without Sj and then adding Sj until measured maximum peak to peak jitter without extrapolation (measured Tj) increased by 40 ps). All other noise sources are off during this calibration.

Measure eye height with CP0 at a BER of 10^{-6} at the end of the channel with the host fixtures with all jitter sources and SSC on applying JTF and the Long channel reference equalizer. Adjust the signal source amplitude to provide

180 mV +5/-0 mV of eye height with host test fixtures for testing a host.

145 mV +5/-0 mV of eye height with device test fixtures for testing a device.

Note: Amplitude should be calibrated to be as close to the minimum value as possible without going under the minimum.

Note: De-emphasis at the instrument output must be adjusted to remain at 3.0 + 0.3/ - 0 dB after the eye height calibration process is complete.

After calibration is complete the Tj at a BER of 10^{-12} with CP0 and all jitter sources on must be between 90 and 95 picoseconds. This measurement is done only with the Sj frequency of 50 Mhz and is performed by checking the average Tj over three 1 million unit interval oscilloscope captures. Due to degradation in connections in the test channel or other test channel issues it may be necessary to switch to a new test channel to achieve a calibrated Tj value in the expected range.

3. Connect the DUT to the appropriate test channel.
4. Power on the device under test.
5. Transmit 200 Polling.LFPS (2ms).

    Note that all jitter sources are added during all transmissions to the device under test. If the device does not go into loopback it fails the test.

6. Transmit 65536 TSEQ.
7. Transmit 256 TS1.
8. Transmit 256 TS2 with loopback bit set.
9. Start transmitting the BDAT test pattern.
10. Transmit BDAT for 2 ms before starting error calculations.

11. Transmit the BDAT sequence from the signal source for a total of $3x10^9$ symbols ($3x10^{10}$ bits). A single SKP ordered set is inserted in the sequence every 354 symbols.

12. The DUT fails if more than one error is encountered. .

    Note: The channel to the test equipment receiver is kept as short and clean as possible.

13. Repeat steps 3-11 with 40.0 +0/-10% ps of periodic (sinusoidal) at a 33 MHz frequency with -3dB of equalization.
14. Repeat steps 3-11 with 40.0 +0/-10% ps of periodic (sinusoidal) at a 20 MHz frequency with -3dB of equalization.
15. Repeat steps 3-11with 40.0 +0/-10% ps of periodic (sinusoidal) at a 10 MHz frequency with -3dB of equalization.
16. Repeat steps 3-11 with 40.0 +0/-10% ps of periodic (sinusoidal) at a 4.9 MHz frequency with -3dB of equalization.
17. Repeat steps 3-11 with 100 +0/-5% ps of periodic (sinusoidal) at a 2 MHz frequency with -3dB of equalization.
18. Repeat steps 3-11 with 200 +0/-5% ps of periodic (sinusoidal) at a 1 MHz frequency -3dB of equalization.
19. Repeat steps 3-11 with 400 +0/-5% ps of periodic (sinusoidal) at a 500 KHz frequency -3dB of equalization.

Connect the breakout fixture only (short channel) to the signal source with the signal source keeping all settings the same as the calibrated settings with the calibration channel.

20. Measure the maximum peak to peak differential voltage with CP0 with a record depth of one million unit intervals at the end of the breakout fixture only channel with all jitter sources and SSC on applying JTF and the short channel reference equalizer. Adjust amplitude to provide a maximum peak to peak differential voltage of 1200 mV +0/-20 mV.

Note: Amplitude should be calibrated to be as close to the maximum value as possible without going over the maximum.

Note: De-emphasis at the instrument output must be adjusted to remain at 3.0 + 0.3/ - 0 dB.

21. Repeat steps 3-19.