

Universal Serial Bus Implementers Forum Host High-speed Electrical Test Procedure

Revision 1.0

Dec 23, 2001

Revision History

Rev	Date	Filename	Comments
0.8	26-Jun-2001	Host HS Test.DOC	Initial draft revision
0.81	12-Jul-01	Host HS Test.DOC	Changed el_17 on page 36 to reference Section 7.1.6.2.
0.9 (Beta)	Aug-31-2001	Host HS Test.DOC	Switch to integrated Test Tool software in place of SSTD and Test Mode software; remove redundant tests; Align test assertion section number (EL_xx) to Version 1.00 of USB-IF USB 2.0 Electrical Test Specification
1.0	Dec-23-2001	Host HS Test.DOC	Edit for final release. Delete TDR section.

Please send comments via electronic mail to techsupp@usb.org

USB-IF High-speed Electrical Test Procedure
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1 Introduction

The USB-IF High-speed Electrical Test Procedures are developed by the USB 2.0 Compliance Committee under the direction of USB-IF, Inc. There are three High-speed Electrical Test Procedures. The Host High-speed Electrical Test Procedure is for EHCI host controllers. The Hub High-speed Electrical Test Procedure is for high-speed capable hubs. The Device High-speed Electrical Test Procedure is for high-speed capable devices.

The High-speed Electrical Compliance Test Procedures verify the electrical requirements of high-speed USB operation of these devices designed to the USB 2.0 specification. In addition to passing the high-speed test requirements, high-speed capable products must also complete and pass the applicable legacy compliance tests identified in these documents in order to be posted on the USB-IF Integrators List and use the USB-IF logo in conjunction with the said product (if the vendor has signed the USB-IF Trademark License Agreement). These legacy compliance tests are identified in the Legacy USB Compliance Test section in this document.

2 Purpose

This USB-IF High-speed Electrical Test Procedure documents a series of tests used to evaluate USB peripherals and systems operating at high-speed. These tests are also used to evaluate the high-speed operation of USB silicon that has been incorporated in ready-to-ship products, reference designs, proofs of concept and one of a kind prototypes of peripherals, add-in cards, motherboards, or systems.

This test procedure makes reference to the test assertions in the USB-IF USB2.0 Electrical Test Specification, Version 1.00.

This Host USB-IF High-speed Electrical Test Procedure is one of the three USB-IF High-speed Electrical Compliance Test Procedures. The other two are Hub USB-IF High-speed Electrical Test Procedure and Device USB-IF High-speed Electrical Test Procedure. The adoption of the individual procedures based on the device class makes it easier to use.

3 Equipment Required

The commercial test equipment listed here are base on positive experience by the USB-IF members in executing the USB high-speed electrical tests. This test procedure is written with a set of specific models we use to develop this procedure. In time, there will be other equivalent or better test equipment suitable for use. Some minor adaptation of the procedure will be required in those cases.

Digital Sampling Oscilloscope:

- Tektronix TDS694C digital sampling oscilloscope
 - Tektronix P6247 or P6248 or equivalent differential probe, qty = 1
 - Tektronix P6245 FET probes, qty = 2
- 3 ½ Digital Multimeter – Fluke Model 77 or equivalent

- Mini-clip DMM lead – one each of black and red color
- Digital Signal Generator
 - Tektronix DG2040 Digital Signal Generator
 - 5x attenuator – for scaling the DSG output voltages needed for receiver sensitivity test, qty = 2
 - 50-ohm coaxial cable with female SMA connectors at both ends, qty = 4
 - High-speed USB Electrical Test Fixtures
 - Host high-speed signal quality test fixture, qty = 1
 - Disconnect test fixture, qty = 1
 - 5V test fixture power supply, qty = 1
 - Female Serial B to female Serial A adaptor, qty = 1
 - Miscellaneous Cables
 - 1M USB cable, qty = 1
 - 1.5M USB cable, qty = 1
 - Modular AC power cord, qty = 2
 - High-speed Signal Quality Analysis Computer

This is a computer with Windows 2000 Profession OS, and have the GPIB-DAQ and Mathworks, Inc's Matlab installed. It retrieves the captured data from the oscilloscope through a GPIB interface. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

- High-speed USB Test Bed Computer

This is the computer that hosts a USB 2.0 compliance host controller for high-speed hub or device electrical test, or serves as a test bed host for a USB 2.0 host controller under test. This OS on this computer is Windows 2000 Professional. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

Note: One can consolidate the High-speed Signal Quality Analysis Computer and the High-speed USB Test Bed Computer into one single PC.

3.1 Equipment Setup

3.1.1 Test Equipment Setup Diskettes

3 setup floppy diskettes are needed for the test equipments used in this procedure. The setup files simplify equipment setup. Insert the Scope Tek 694C setup floppy diskette into the Tektronix TDS694C oscilloscope. Insert the Data Generator Pattern DG2040 into the Tektronix DG2040 data generator.

3.1.2 TDS694C Digital Sampling Oscilloscope

Before turning on the oscilloscope. Attach a P6247 or P6248 differential probe to Channel-1. Attach two P6245 FET probes, one to Channel-2 and one to Channel-3. The probe assignment will be used through out the entire test procedure. Turn on the oscilloscope to allow for 10 minutes of warm up time prior to use. Perform the signal path compensation procedure built into the TDS694C (in the Utility menu) if the ambient temperature has changed more than 5 degrees. The compensation should be performed with the probes disconnected from the oscilloscope.

The two single-end FET probes must be calibrated to minimize gain and offset errors. The offset errors of the diff probes will be cancelled later as a part of the test procedure process. The offset of the differential probe will be adjusted by the step identified in the test procedure.

For P6247/P6248 differential probes, the following setting will be used through out the entire test procedure:

- DC Reject <OFF> (P6247 only)
- BW <Full> (P6247 only)
- Attenuation <+1>

Note: In certain test situation, there may not be a ground connection between the DSO and the device under test. This may lead to the signal seen by the differential probe to be modulated up and down due to mid frequency switching power supply. Connecting the DSO ground to the DUT ground will be require to establish a common ground reference.

3.1.3 DG2040 Digital Signal Generator

The DSG is needed to perform the receiver sensitivity test that is structured toward the end of this test procedure. For energy conservation consideration, one may choose to turn on the DSG about 15 minutes prior to performing the measurement.

3.2 Operating Systems, Software, Drivers, and Setup Files

3.2.1 Operation Systems

Microsoft Windows 2000 Professional is required on the High-speed Electrical Test Bed Computer. Microsoft Windows 2000 Professional is required on the High-speed Signal Quality Analysis Computer. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

3.3 Special Purpose Software

The following special purpose software is required. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

- High-speed Electrical Test Tool Software – To be used in the High-speed Electrical Test Bed Computer.
- Proprietary EHCI Driver Stack - The High-speed Electrical Test Tool software requires the use of a proprietary EHCI driver stack. The use of this proprietary EHCI driver stack facilitates the electrical testing that requires direct control of the command registers of the USB EHCI host controllers. The end result much more robust test bed environment. Since the proprietary EHCI driver stack is designed for debug and test validation purposes, this driver stack does not support the normal functionality as found in the EHCI drivers from Microsoft (or the device vendor). An automatic driver stack switching function has been implemented into the High-speed Electrical Test Tool for easy switching between the proprietary EHCI driver stack and that from Microsoft. Upon invocation of the HS Electrical Test Tool software, the driver stack will automatically switch to the Intel proprietary EHCI driver stack. Upon exit of the HS Electrical Test Tool software, the driver stack will automatically switch to the Microsoft EHCI driver stack.
- Matlab 6 – Data analysis programming software
- USB Electrical Test Analysis Scripts for Matlab 6 – For performing electrical signal quality test on USB devices.
- GPIB DAQ – This is developed by USB-IF for importing the digitized signal in TSV (Tab Separated Value) file format from the DSO into the Matlab analysis script for signal analysis.

3.3.1 Test Equipment Setup Files

These are 3 ½ inch floppy diskettes that contain the setup files for the test equipment. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these setup disks.

DSO Setup Disk – Contain setup files for Tektronix TDS694C DSO (Digital Storage Oscilloscope).

DPG Setup Disk – Contain setup files for Tektronix DG2040 DPG (Digital Pattern Generator).

4 Test Procedure

4.1 Test Record

Appendix A contains the test result entry form for this test procedure. Please make copies of the Appendix A for use as test record documentation for compliance test submission. All fields must be filled in. Fields not applicable for the device under test should be indicated as N/A, with appropriate note explaining the reason. The completed test result shall be retained for the compliance test submission.

In addition to the hardcopy test record, the electronic files from the signal quality, and power delivery (inrush, drop and droop) shall be retained for compliance test submission.

4.2 Vendor and Product Information

Collect the following information and enter into a copy of the test record in Appendix A before performing any tests.

1. Test date
2. Vendor name
3. Vendor address and phone, and the contact name
4. Test submission ID number
5. Product name
6. Product model and revision
7. USB silicon vendor name
8. USB silicon model
9. USB silicon part marking
10. USB silicon stepping
11. Test conducted by

4.3 Legacy USB Compliance Tests

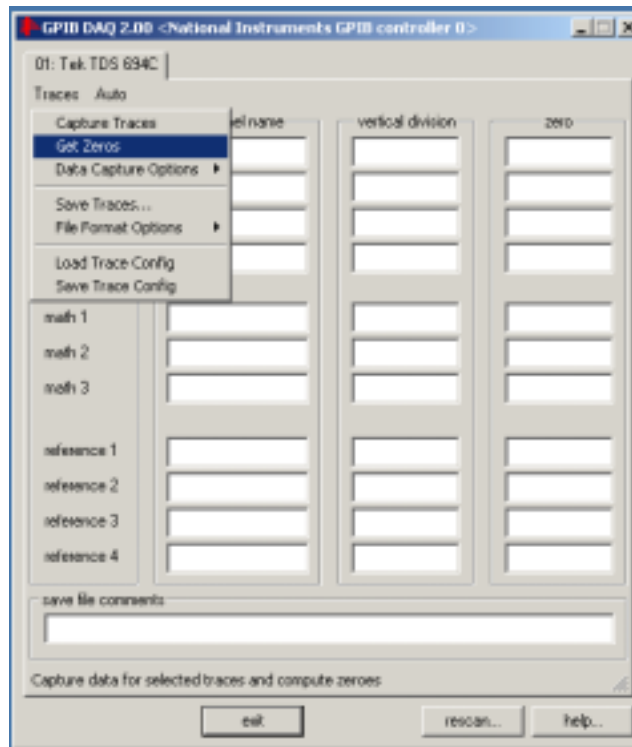
In addition to the high-speed electrical tests prescribed in this document, the host controller under test must also pass the following compliance tests applicable to the EHCI Host Controller:

- Low speed signal quality
- Full speed signal quality
- Drop/Droop
- Interoperability

Perform all these tests and record the measurements and summarized Pass/Fail status in Appendix A.

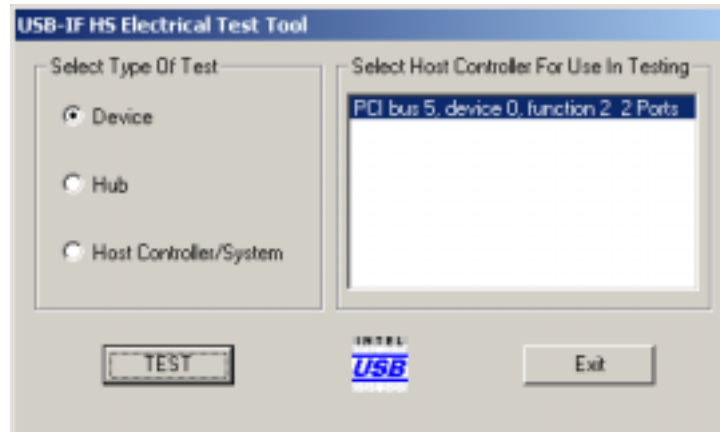
4.4 Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

1. Turn on the oscilloscope if not have already done so. Allow about 10 minutes for warm up.
2. Boot the High-speed Signal Quality Analysis Computer to the Windows 2000 OS. Invoke the GPIB-DAQ program. Invoke also Mathworks' Matlab program.
3. Recall HS_SQ_1.SET oscilloscope setup. Ensure the differential probe is not connected to anything. Force-trigger the oscilloscope to capture a near-zero differential measurement.



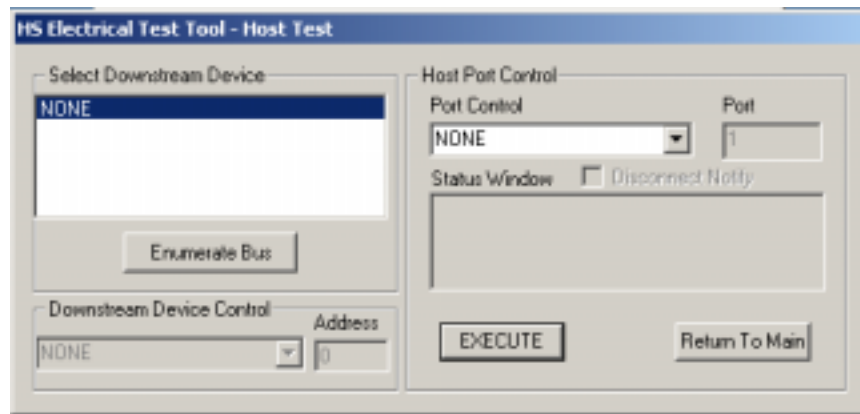
Get Zeros on GPIB-DAQ

4. On the GPIB-DAQ, click Get Zeros from the Traces drop down menu. This should generally be less than a few millivolts. The near-zero differential measurement will be used by the Matlab script to null out the residual offset on the probe/oscilloscope combination.
5. Attach the 5V power supply to J8 of the Host High-Speed Signal Quality test fixture and verify the green Power LED (D1) is lit. Set the Test switch (S1) of the test fixture to TEST and verify the yellow TEST LED is lit.
6. Attach the differential probe to J7 of the test fixture. Ensure + on probe lines up with D+ on fixture.
7. Invoke the High-speed Electrical Test Tool software on the High-speed Electrical Test Bed computer. The main menu appears and shows the USB2.0 host controller.



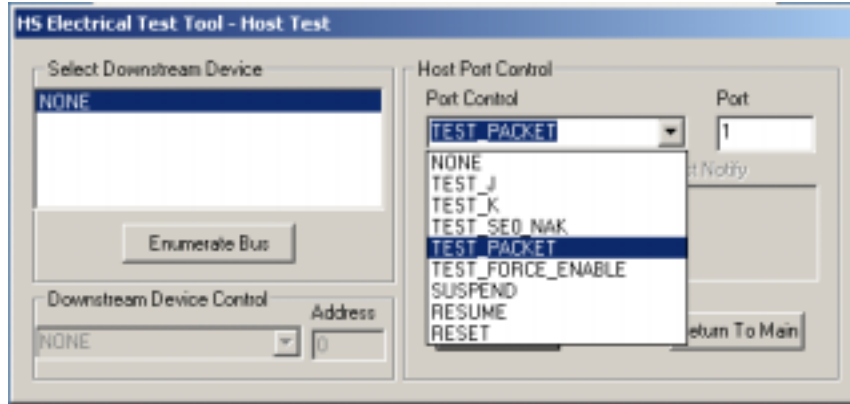
Main Menu

8. Select Host Controller/System and click the TEST button to enter the Host Test menu.



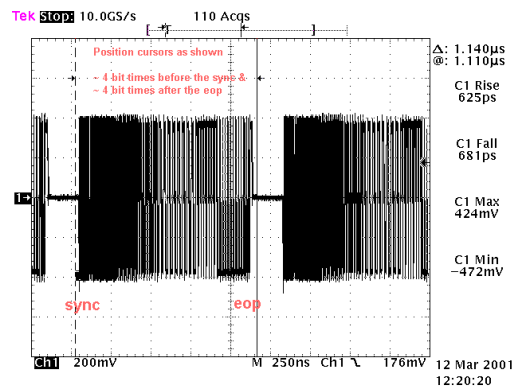
Host Test Menu

9. Connect the Test port of the Host High-speed Signal Quality test fixture into the port under test of the Host controller.
10. Select TEST_PACKET from the Port Control drop down menu. Enter the port number of the port being tested and click Execute. This forces the port under test to continuously transmit test packets.



TEST_PACKET

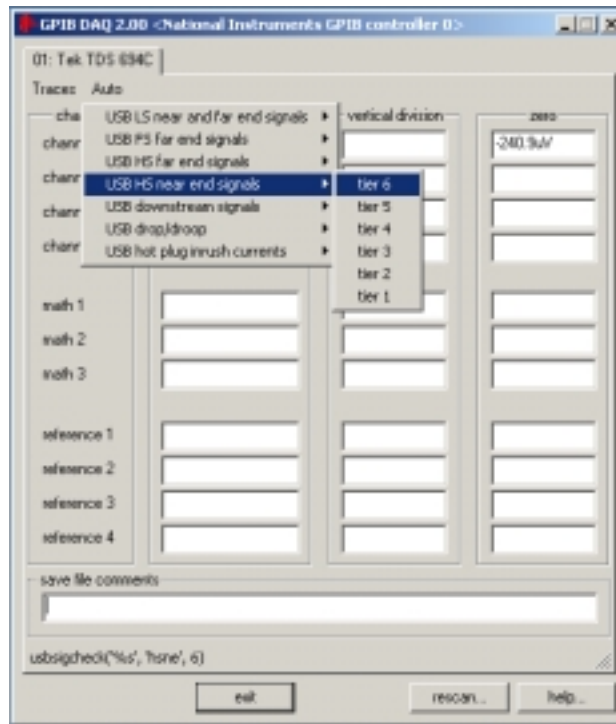
11. Using the oscilloscope, verify test packets are being transmitted from the port under test. Adjust the trigger level as necessary. If a steady trigger cannot be obtained by adjusting the trigger level, try slight change to the trigger holdoff.
12. Pause the oscilloscope acquisitions using the Run/Stop button.
13. On the oscilloscope place the two vertical cursors around one test packet, one just (about one bit time) before the sync field and the other just (about one bit time) after the EOP (END OF PACKET). Refer to the following figure.



High-speed Test Packet

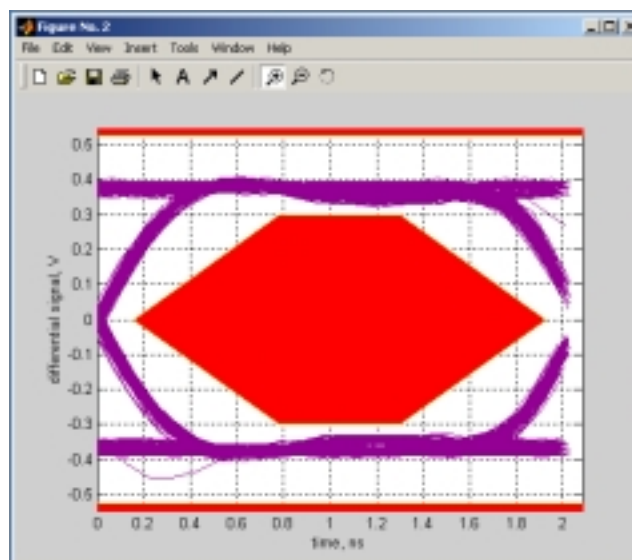
14. Using the GPIB DAQ graphical user interface select:

Auto -> USB HS near end signals -> Tier 6.

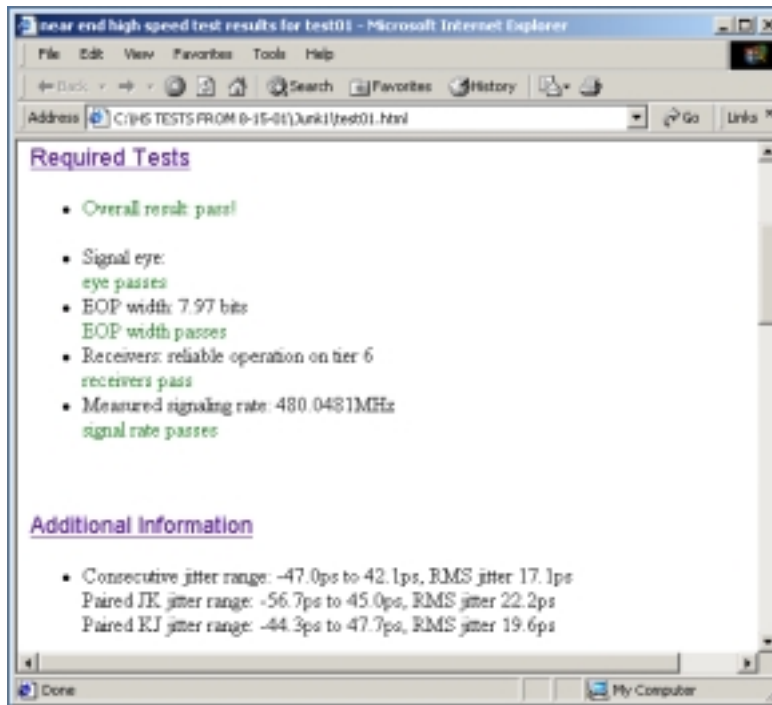


GPIB-DAQ

15. Enter a descriptive file name (e.g. TIDxxxxxxx port 1 HSNE.tsv) and save the *.tsv to the desired directory.
16. Switch to the Matlab command window. Verify that the directory path, file name and test selected are correct. Press the Enter key to initiate the analysis.
17. Verify the Signal Eye, EOP Width, and Signaling Rate all pass. The results displayed in the Matlab command window are also recorded to an HTML report located in the same directory as the *.tsv file.



High-speed SQ Eye Diagram



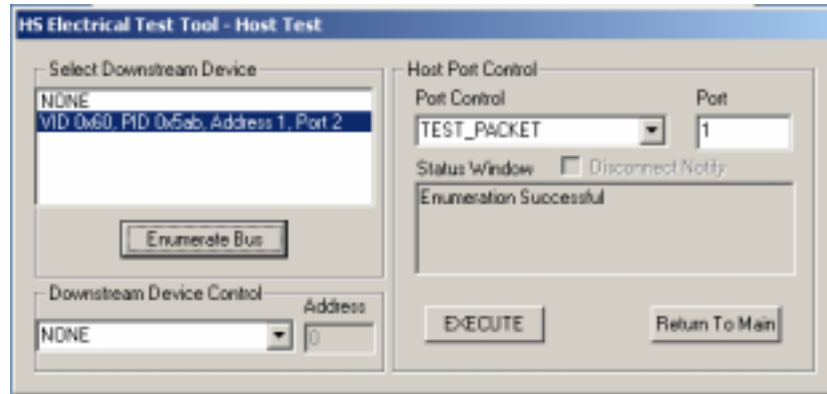
High-speed SQ HTML Report

18. Record the test result in EL_2, EL_3, EL_6, and EL_7.
19. Remove the Host Signal Quality test fixture from the port.
20. Repeat steps 9 through 19 for all remaining ports.
21. Save all files created during the tests. Remove the Host Signal Quality test fixture from the host controller.

Note: If you desire to save a file to the same name as a previous test run, be sure you delete the old file first since the GPIB DAQ software will append the new data to the old file. This will cause the Matlab analysis script to fail.

4.5 Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55)

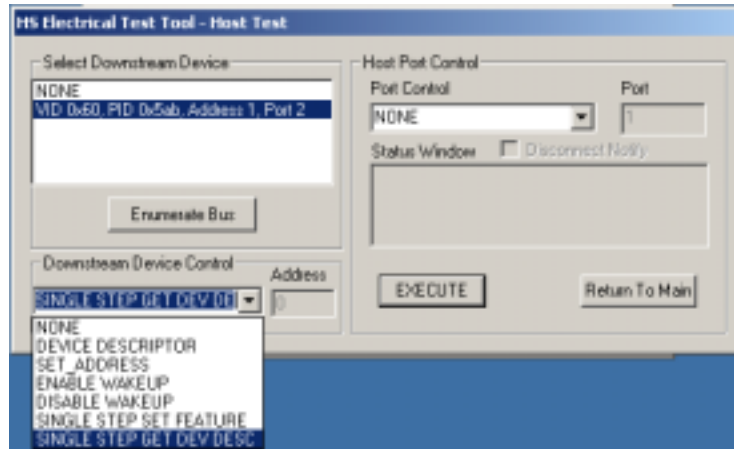
1. Connect the Device Signal Quality test fixture (Test Port) into B receptacle of a known good high-speed device. Apply power to the known good device.



Known-Good Device Enumerated

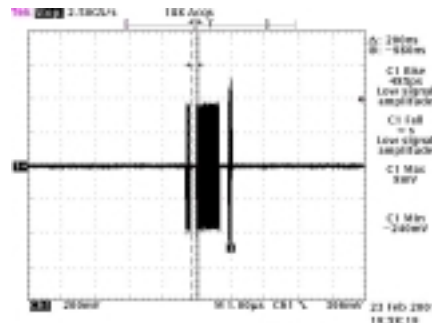
Note: The use of the Device High-speed Signal Quality test fixture makes it possible to trigger on packets generated by the device because the differential probe is located closer to the device transmitter, hence the device packets are larger in amplitude.

2. Attach the differential probe to J7 on the fixture near the device connector. Ensure + on probe lines up with D+ on fixture.
3. Recall the PACKPARAM.SET oscilloscope setup.
4. Connect the Device Signal Quality test fixture (Init Port) into host controller port under test. Click Enumerate Bus and verify that the device enumerates properly.
5. Using the oscilloscope, verify SOFs (Start Of Frame packets) are being transmitted on port under test. You may need to lower the trigger level to somewhat below 400mV to obtain a trigger.
6. Now raise the oscilloscope trigger level slowly until it doesn't trigger on SOFs (or any host traffic). Typically this is around or slightly below 400mV, depending on the device used and length of cable used on the fixture. Ensure the RUN/STOP of the oscilloscope is set to RUN.
7. In the Host Test menu of the High-speed Electrical Test Tool software, ensure the device under test is selected (highlighted). Select SINGLE STEP GET DEV DESC from the Downstream Device Control menu and click Execute once.



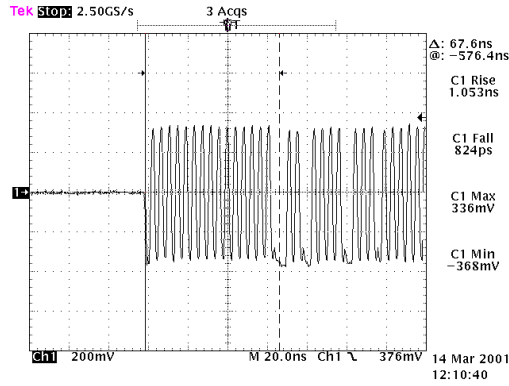
Device Single Step Get Descriptor

8. The oscilloscope capture should appear as follows. Press STOP on the oscilloscope to prevent mistrigger from random noise. If the oscilloscope doesn't trigger on the device traffic the trigger level is set too high. Lower the trigger level slightly (but not so low that it triggers on host SOFs) and repeat from step 10.



Packet from Host and Device

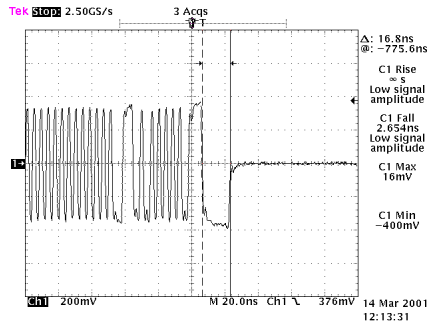
9. Use the zoom function of the oscilloscope, measure the sync field length (number of bits) of the first and second packets on the oscilloscope and verify that they are both 32 bits per EL_21. Refer to the figure below for reference. Note that Sync Field starts from the high-speed idle transitions to a falling edge (due to the first zero). Count both rising and falling edges until the first two consecutive 1's and include the first 1. There must be 32 bits. Record the number in EL_21.



Host Packet Sync Field

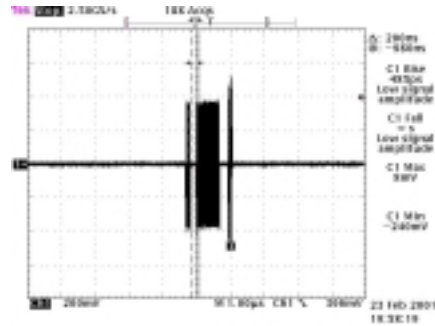
10. Measure the EOP length (number of bits) of the second packet on the oscilloscope and verify that it is 8 bits per EL_25. It is advisable to use the cursors to measure the EOP pulse width to determine the number of bits, based on 2.08nS/bit (480Mbps). Record the result in EL_25.

Please note that the EOP could appear as a negative going pulse, or a positive going pulse on differential measurement. The figure below illustrates the negative going pulse.



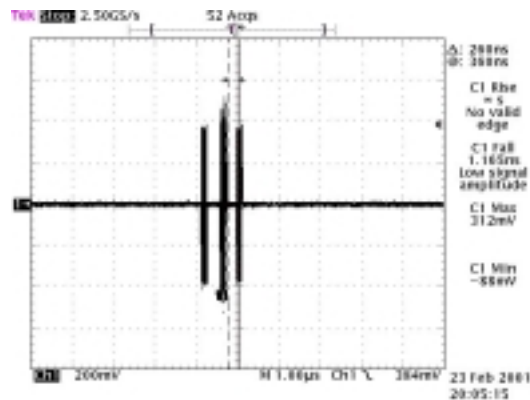
Host Packet EOP

11. Measure the inter-packet gap between the first two packets shown on the oscilloscope. These are back-to-back packets from the host. Compute the bits by dividing the time measure by 2.08nS. The requirement is it must be between 88 bits and 192 bits. (EL_23). Record the computed number of bits in EL_23. The oscilloscope should appear as shown in the following figure.



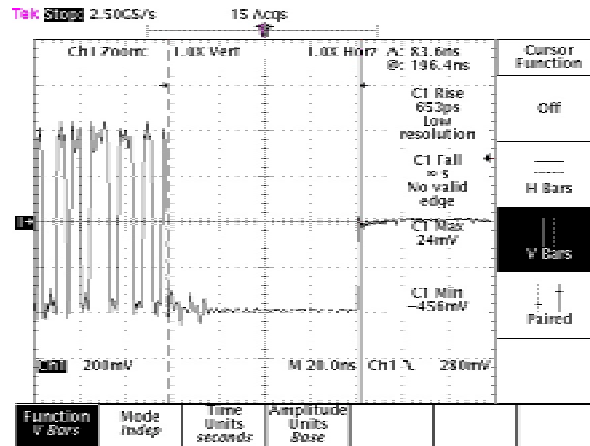
Inter-packet Gap – Between Packets from Host

12. Ensure the oscilloscope is armed (press run/stop button).
13. On the Host Test menu click Execute once. The oscilloscope capture should appear as the figure below. Pause the oscilloscope with the run/stop button.
14. Measure the inter-packet gap between the second and the third packets shown on the oscilloscope. The second (of higher amplitude) is a device packet and the third is the host response. Compute the number of bits by dividing the time measure by 2.08nS. The requirement is it must be between 8 bits and 192 bits. (EL_22). Record the computed number of bits in EL_22.



Inter-packet Gap – Host Respond to Device

15. Set the oscilloscope to RUN. Adjust the trigger if necessary until the oscilloscope is continuously being triggered by the SOF packets. Stop the oscilloscope. Measure the time period of the EOP width. Compute the number of bits by dividing the time measure by 2.08nS. The requirement is it must be 40 bits. Record the result in EL_55.



EOP Width - SOF Packet

16. Repeat step 4 through 15 for the remaining ports.
17. Remove the Device Signal Quality test fixture and the known good device from the host controller port under test.

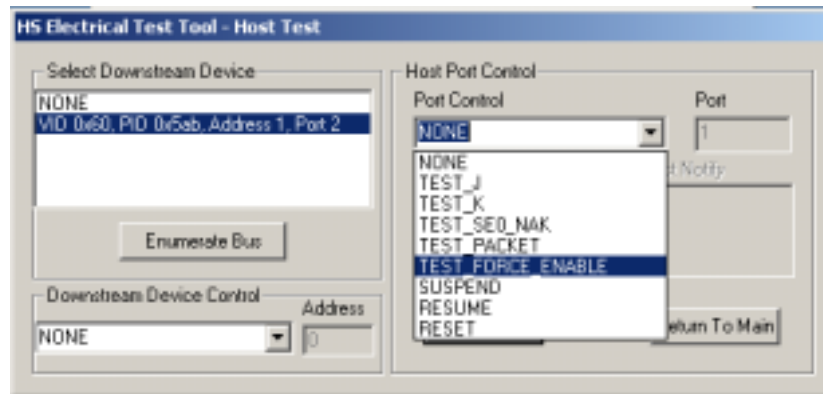
4.6 Host Disconnect Detect (EL_36, EL_37)

This section uses the Disconnect test fixture to verify the disconnect thresholds of the port under test by simulated disconnect condition.

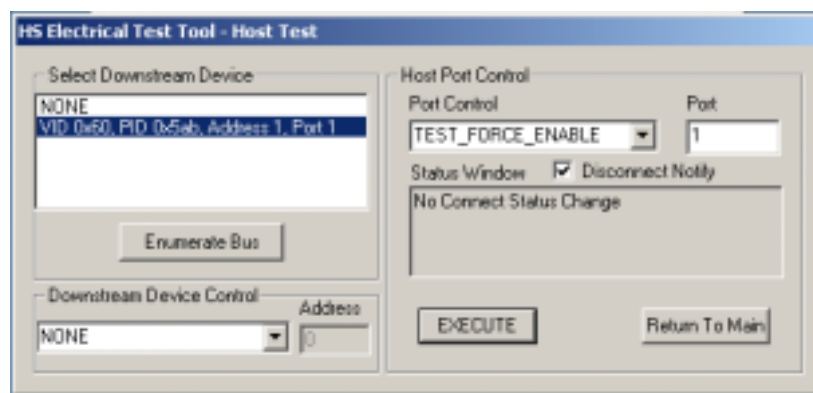
When the TEST switch on the test fixture is in the Test position, the port under test is subjected to a threshold $<525\text{mV}$. The port should not detect a disconnection.

When the TEST switch is in the Normal position, the port under test is subjected to a threshold $>625\text{mV}$. The port should detect a disconnection.

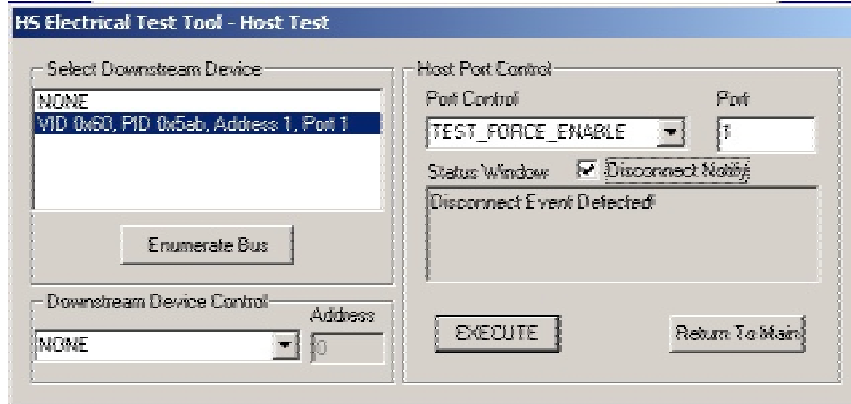
1. Attach the 5V power supply to Disconnect test fixture (J8).
2. Attach the differential probe to J7. Ensure the + tip on probe lines up with D+ on the fixture. Recall the DISCDETE.SET oscilloscope setup.
3. Set the TEST switch to the Test position. Verify the green Power LED (D1) is lit, and the yellow Test LED (D2) is also lit. This sets the test fixture to emulate a must-not-disconnect threshold.
4. Attach the Test port of the test fixture to the port under test. In the Host Test menu of the High-speed Electrical Test Tool software select TEST_FORCE_ENABLE from the Port Control window. Enter the port number and click Execute once and ensure the operation is successful in the Status Window.



5. Click the Disconnect Notify check box to monitor the disconnect status in the Status Window.



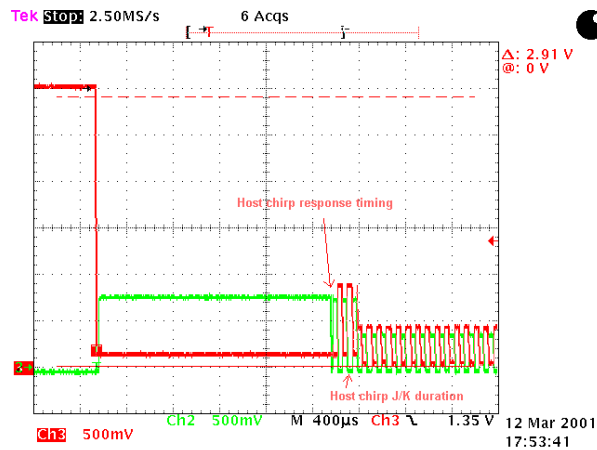
6. Using the oscilloscope, verify the SOF packets are being transmitted from the port under test. The differential amplitude should be less than +/- 525mV. Verify that the Status Window does not display Disconnect Event Detected. Record the pass/fail result in EL_37.
7. Set the TEST switch of the Disconnect test fixture to the Normal position and verify the yellow TEST LED (D2) is not lit.
8. Use the oscilloscope to monitor the differential amplitude of the SOF. It should be greater than +/- 625mV. Verify that the Status Window now displays the Disconnect Event Detected. Record the pass/fail result in EL_36.



9. Return the TEST switch on the fixture back to the TEST position and verify the yellow TEST LED (D2) is lit.
10. Repeat step 4 through 9 for all the remaining ports.
11. Remove the Disconnect test fixture from the port under test before proceeding.

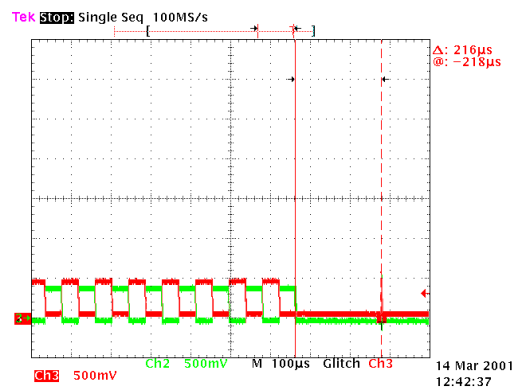
4.7 Host CHIRP Timing (EL_33, EL_34, EL_35)

1. Replace the Disconnect test fixture with the Host High-speed Signal Quality test fixture.
2. Connect Channel 2 and Channel 3 FET probes to test fixture at J7. Connect Ch2 to D- and Ch3 to D+. Connect the probe grounds to J10 and J11.
3. Recall the CHRP2&3.SET oscilloscope setup.
4. Connect a known-good HS device into the INIT port of the test fixture.
5. Connect the TEST port of the fixture to the port under test. Apply power to the known-good HS device.
6. Click Enumerate Bus and capture the CHIRP handshake as in the figure below.



High-speed Chirp

7. Measure the host's Chirp response timing ($T_{WTRSTFS}$). This is the time between the device's de-assertion of Chirp-K and the start of alternate Chirp-K and Chirp-J sent by the host. Verify this timing is $T_{WTRSTFS} \leq 100\mu\text{s}$. Record the result in EL_33.
8. Measure and record the durations of the individual Chirp-K and Chirp-J states and verify both are between $40\mu\text{s} \leq T_{DCHBIT} \leq 60\mu\text{s}$ (EL_31). Record the measurement in EL_34.
9. Recall the SOFCHP23.SET oscilloscope setup.
10. Unplug the known good device and then reattach it.
11. Ensure the oscilloscope trigger is armed.
12. Click Enumerate Bus once. The oscilloscope capture should appear as follows.

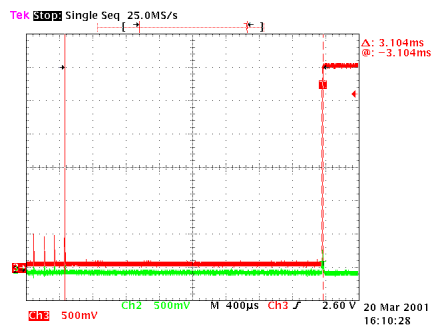
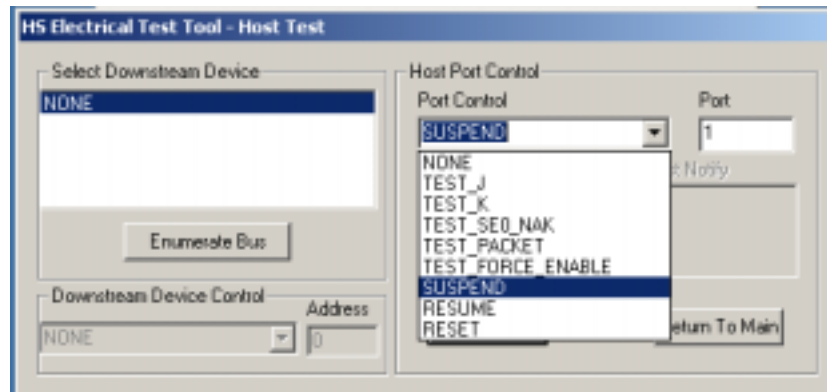


Time between SOF and Last Chirp- (J or K)

13. Measure the time from the end of host Chirp-J/K to the first SOF sent out by the host. Verify this is $100\mu\text{s} \leq T_{DCHSE0} \leq 500\mu\text{s}$. Record in EL_35.
14. Repeat step 5 through 13 for the remaining down stream facing ports.

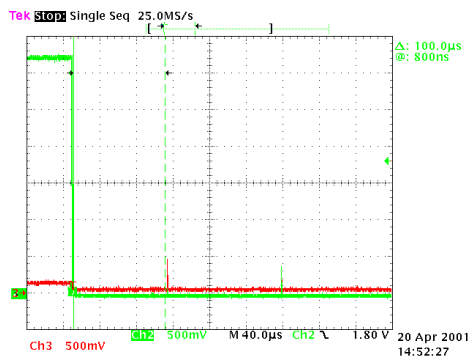
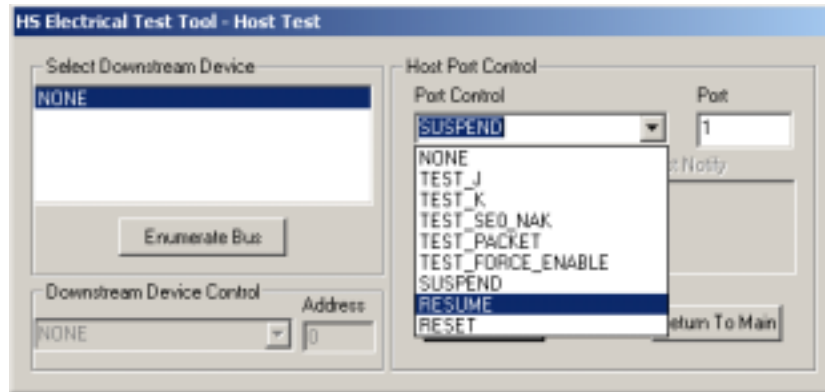
4.8 Host Suspend/Resume timing (EL_39, EL_41)

1. Connect a known good high-speed device into the INIT port of the Host High-speed Signal Quality test fixture.
2. Connect Channel 2 and Channel 3 FET probes to the test fixture at J7. Connect Ch2 to D- and Ch3 to D+. Connect the probe grounds to J10 and J11.
3. Recall the SUSP2&3.SET oscilloscope setup and verify the oscilloscope is armed.
4. Attach the TEST port of the fixture into the port under test at the host controller.
5. On the Host Test menu, select SUSPEND from the Port Control drop down menu and enter the port number. Click Execute once to place the port into suspend. The captured suspend transition should appear as in the figure below.



Device Enters Suspend

6. Observe the time interval from the end of last SOF packet issued by the host to when the device attached its full speed pull-up resistor on D+ (transition to full speed J-state). This time should be between 3.000mS and 3.125mS. No measurement is required as this sequence verify the host supports Suspend state. Record the Pass/Fail result in EL_39.
7. Recall the RESUM2&3.SET oscilloscope setup and verify the oscilloscope is armed.
8. On the Host Test menu, select RESUME from the Port Control drop down menu and enter the port number. Click Execute once to resume the port. The captured suspend transition should appear as in the figure below.



Time to First EOP from Start of HS Idle

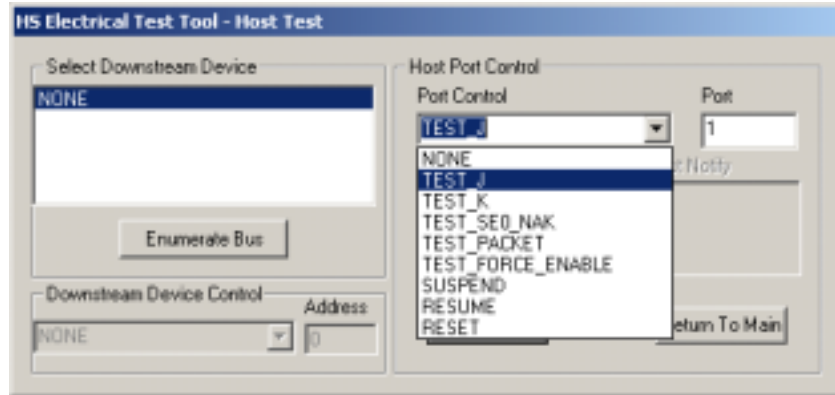
- Measure the time from the falling edge of D+ to the first SOF issued by the host (EL_41) as shown in the figure below. Record the results in EL_41.

Note: Repeat the suspend and resume a number of times and verify the time from the falling edge of D+ to the first SOF issued by the host never exceeds 3mS.

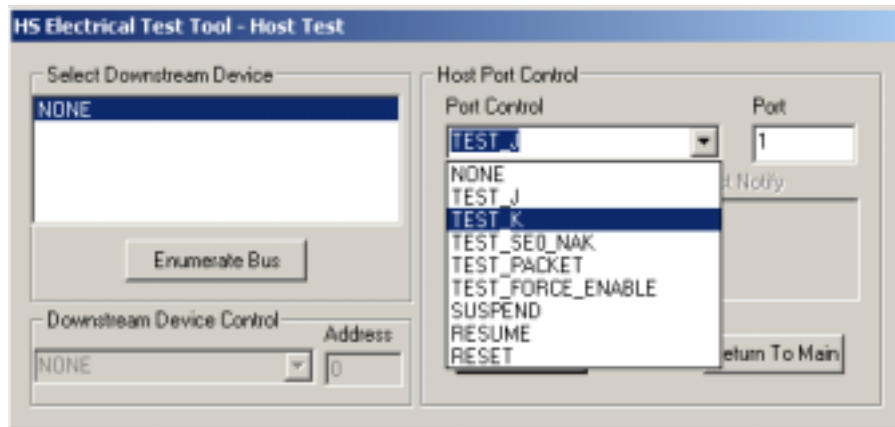
- Repeat step 4 through 9 for all the remaining ports.
- Unplug the know-good device from the test fixture. Click Enumerate Bus once before proceeding. Remove the FET probes from the test fixture.

4.9 Host Test J/K, SE0_NAK (EL_8, EL_9)

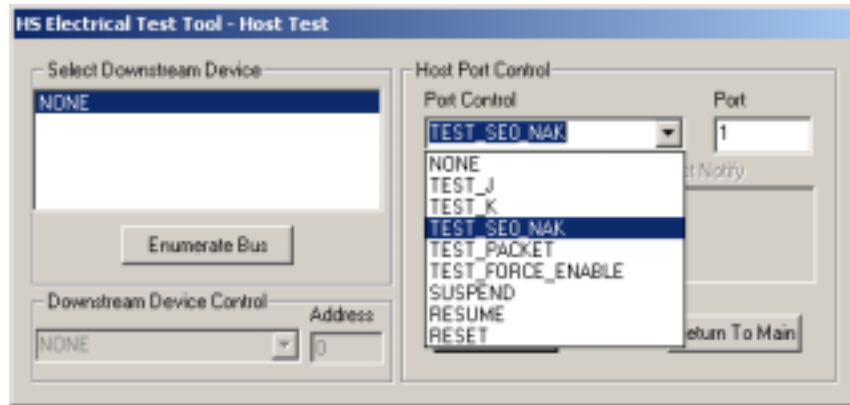
- Attach the 5V power supply to the Host Signal Quality test fixture (J8) and verify the green Power LED (D1) is lit. Place the TEST Switch (S1) in the Test position. Verify the yellow TEST LED is lit.
- Attach the TEST port of the Host Signal Quality test fixture into the port under test.
- Select TEST_J from the Port Control drop down menu. Enter the port number and click Execute once to place the port under test into TEST_J test mode.

Host Port TEST_J

4. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_8.
5. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_8.
6. On the Host Test menu, select TEST_K from the Port Control drop down menu. Enter the port number and click Execute once to place the port under test into TEST_K test mode.

Host Port TEST_K

7. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_8.
8. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground. Record in section EL_8.
9. On the Host Test menu, select TEST_SE0_NAK from the Port Control drop down menu. Enter the port number and click Execute once to place the port under test into TEST_SE0_NAK test mode.



Host Port TEST_SE0_NAK

10. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9.
11. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9.
12. Repeat step 2 through 11 for the remaining ports.

Appendix A

A.4 Host High-speed Electrical Test Data

This section is for recording the actual test result. Please use a copy for each device to be tested.

A.4.2 Vendor and Product Information

	Please fill in all fields. Please contact your silicon supplier if you are unsure of the silicon information.
Test Date	
Vendor Name	
Vendor Complete Address	
Vendor Phone Number	
Vendor Contact, Title	
Test ID Number	
Product Name	
Product Model and Revision	
USB Silicon Vendor Name	
USB Silicon Model	
USB Silicon Part Marking	
USB Silicon Stepping	
Tested By	

A.4.3 Legacy USB Compliance Tests

Legacy USB Compliance Checklist

Legacy Test	Downstream Ports					Comments
	P1	P2	P3	P4	P5	
LS SQ						
FS SQ						
Drop/ Droop						
Interop						

P = PASS

F = FAIL

N/A = Not applicable

A.4.4 Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb/s \pm 0.05%.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:

- Pass
- Fail
- N/A

Comments:

EL_3 A USB 2.0 downstream facing port must meet Template 1 transform waveform requirements measured at TP2 (each host downstream port).

Reference documents: *USB 2.0 Specification, Section 7.1.2.2.*

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:

- Pass
- Fail
- N/A

Comments:

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

Reference documents: *USB 2.0 Specification, Section 7.1.2.2.*

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

- Pass
- Fail
- N/A

Comments:

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

Reference documents: *USB 2.0 Specification, Section 7.1.2.2.*

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

- Pass
- Fail

- N/A

Comments:

A.4.5 Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55)

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

Reference documents: *USB 2.0 Specification, Section 8.2.*

SOF SYNC field

- Pass
- Fail
- N/A

Comments:

Data Packet SYNC field

- Pass
- Fail
- N/A

Comments:

EL_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing. (Note, that a longer EOP is waivable)

Reference documents: *USB 2.0 Specification, Section 7.1.13.2*

- Pass
- Fail
- N/A

Comments:

EL_23 Hosts transmitting two packets in a row must have an inter-packet gap of at least 88 bit times and not more than 192 bit times.

Reference documents: *USB 2.0 Specification, Section 7.1.18.2.*

- Pass
- Fail
- N/A

Comments:

--

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than 192 bit times.

Reference documents: *USB 2.0 Specification*, Section 7.1.18.2.

- Pass
- Fail
- N/A

Comments:

EL_55 Hosts transmitting SOF packets must provide a 40-bit EOP without bit stuffing where the first symbol of the EOP is a transition from the last data symbol.

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

- Pass
- Fail
- N/A

Comments:

A.4.6 Host Disconnect Detect (EL_36, EL_37)

EL_37 A USB 2.0 downstream facing port must not detect the high-speed disconnect state when the amplitude of the differential signal at the downstream facing driver's connector is ≤ 525 mV.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.3.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall:

- Pass
- Fail
- N/A

Comments:

--

EL_36 A USB 2.0 downstream facing port must detect the high-speed disconnect state when the amplitude of the differential signal at the downstream facing driver's connector is ≥ 625 mV.

Reference documents: *USB 2.0 Specification, Section 7.1.7.3.*

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall:

- Pass
- Fail
- N/A

Comments:

--

A.4.7 Host CHIRP Timing (EL_33, EL_34, EL_35)

EL_33 Downstream ports start sending and alternating sequence of Chirp K's and Chirp J's within 100us after the device Chirp K stops.

Reference documents: *USB 2.0 Specification, Section 7.1.7.5.*

- Pass
- Fail
- N/A

Comments:

--

EL_34 Downstream port Chirp K and Chirp J durations must be between 40us and 60us duration.

Reference documents: *USB 2.0 Specification, Section 7.1.7.5.*

- Pass
- Fail
- N/A

Comments:

--

EL_35 Downstream ports begin sending SOFs within 500us and not sooner than 100us from transmission of the last Chirp (J or K).

Reference documents: *USB 2.0 Specification, Section 7.1.7.5.*

- Pass
- Fail
- N/A

Comments:

A.4.8 Host Suspend/Resume timing (EL_39, EL_41)

EL_39 A device must support the Suspend state.

Reference documents: *USB 2.0 Specification, Section 7.1.7.6.*

- Pass
- Fail
- N/A

Comments:

EL_41 After resuming a port, the host must begin sending SOFs within 3ms of the start of the idle state.

Reference documents: *USB 2.0 Specification, Section 7.1.7.7.*

- Pass
- Fail
- N/A

Comments:

A.4.9 Host Test J/K, SE0_NAK (EL_8, EL_9)

EL_8 When either D+ or D- are driven high, the output voltage must be 400 mV \pm 10% when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification, Section 7.1.1.3.*

Port	1		2		3		4		5	
Test	D+	D-	D+	D-	D+	D-	D+	D-	D+	D-
TEST_J										
TEST_K										

- Pass
- Fail
- N/A

Comments:

EL_9 When either D+ and D- are not being driven, the output voltage must be $0V \pm 10\text{ mV}$ when terminated with precision $45\ \Omega$ resistors to ground.

Reference documents: *USB 2.0 Specification, Section 7.1.1.3.*

Port	1		2		3		4		5	
Signal	D+	D-	D+	D-	D+	D-	D+	D-	D+	D-
Measure WRT Ground (mV)										

- Pass
- Fail
- N/A

Comments: