Where Are We?

- **Device or Host**
- **PROTOCOL**
- **LINK**
- **PHYSICAL**

### End-to-End
- Device Driver/Application
- USB System Software
- Notifications
- Transactions
- Data Packets
- Link Management Packets
- Default Control Pipe
- Transaction Packets
- Link Control/Mgmt
- Link Delims
- Link Cdr
- Spread Clock CDR
- Elasticity Buffer/Skips
- 8b10b encode/decode
- Scramble/descramble
- LFPS

### Port-to-Port
- Pipe Bundle (per Function Interface)
- Default Control Pipe
- Transaction Packets
- Data Packets
- Link Management Packets
- Pkt Delims
- Link Cdr
- 8b10b encode/decode
- Scramble/descramble
- LFPS

### Chip to Chip
- Device to Host
- Hub to Device
- 8b10b encode/decode
- Scramble/descramble
- Elasticity Buffer/Skips
- Spread Clock CDR
- LFPS

- USB Function Power Management
- USB Device Power Management (Suspend)
- Localized Link Power Management
Key Messages

Keys to scaling USB to 5 Gb/s with legacy form factors & minimum cost impact:

- Use Moore’s Law
  - Value add in silicon: equalization, training
- Evolve Platform Technology
  - USB 3.0 cable
- Decrease Margin Requirements for Robustness
  - Jitter budgeting with scrambled data
  - Make compliance channel ≈ worst case application channel
Keys to scaling USB to 5 Gb/s with legacy form factors & minimum cost impact:

- Careful Device Design
  - Non-interleaved package/PCB
  - Advanced equalization

LFPS provides a mechanism for:

- Transition from low power state to SuperSpeed
- Forced link retraining via Warm Reset
Agenda

• Challenges
  • PHY Overview & Channel Descriptions
• 5 Gb/s Features
  • USB 3.0 Cable
  • Equalization
  • Scrambling
  • Compliance
  • Device Design
  • Low Frequency Periodic Signaling
• Summary
Challenges

- 5 Gb/s data rate at $10^{-12}$ BER
- Low cost
  - 4 layer PCB, extension of USB cable technology
- Same design & usage flexibility as USB 2.0
  - front panel & back panel connectors, up to 3 m cable
- Robust compliance testing methodology
  - Strong correlation to actual performance
- Transition out of low power states

Stays the same: platform flexibility & cost

Changes: 10x performance boost (480 Mb/s $\rightarrow$ 5 Gb/s)

Today’s focus: features that get us to 5 Gb/s.
PHY Overview

Channel characteristics:
- 2”-12” host PCB length
- 0m to 3m cable
- 1”-6” device PCB length

This is the same channel as for 480 Mb/s USB 2.0
Channel Description

Key Performance Limiters:
- Insertion loss: -8dB to -20dB
- Crosstalk: both NEXT & FEXT
5 Gb/s Data Rate

Frequency dependent loss & crosstalk closes the 5 Gb/s eye
Agenda

• Challenges
• Key Features
  • USB 3.0 Cable
  • Equalization
  • Scrambling
  • Compliance
  • Device Design
  • Low Frequency Periodic Signaling
• Summary
USB 3.0 Cable Assembly

New features added to the cable assembly for SuperSpeed operation
USB 3.0 Cable Assembly

USB 2.0 Cable Attenuation Spec

![Graph showing dB attenuation against frequency in GHz.](image)
USB 3.0 Cable Assembly

USB 2.0 Cable Attenuation Spec

5 Gb/s Requires:
- Extension to 5+ GHz
- Reduced attenuation
USB 3.0 specs make sure cable assemblies support 5 Gb/s transfer rate

SuperSpeed specs:
- Attenuation ($S_{DD12}$)
- Crosstalk (NEXT, FEXT)
- Differential-to-Common mode conversion ($S_{CD12}$)
- Return Loss ($S_{DD11}$)
- Characteristic Impedance
Agenda

• Challenges
• Key Features
  • USB 3.0 Cable
  • Equalization
  • Scrambling
  • Compliance
  • Device Design
  • Low Frequency Periodic Signaling
• Summary
Equalization

Frequency dependent loss & crosstalk closes the 5 Gb/s eye
Equalization increases the useable bandwidth of the channel
Equalization

USB 3.0 uses equalization @ transmitter & receiver to open up the 5 Gb/s data eye
Transmitter Equalization

Example Waveform

1 bit of equalization @ -3.5±0.5dB

Discrete Linear Equalizer (DLE)
TSEQ is transmitted $2^{16}$ times at initialization to allow optimization of equalizer settings.
Agenda

• Challenges
• Key Features
  • USB 3.0 Cable
  • Equalization
  • Scrambling
  • Compliance
  • Device Design
  • Low Frequency Periodic Signaling
• Summary
Jitter Budget

- Dual-Dirac Model @ 10^{-12} BER
  - $TJ = \text{total jitter}$
  - $RJ = \text{random jitter}$
  - $DJ = \text{deterministic jitter}$
- Data scrambling gives channel jitter a quasi-random component
- Improves budget margins by ~20ps

\[
\sigma_{RJTotal} = \left( \sigma_{RJ Tx}^2 + \sigma_{RJ Channel}^2 + \sigma_{RJ Rx}^2 \right)^{\frac{1}{2}}
\]

\[
\sigma_{RJ} = 4.03 \text{ps}
\]

\[
DJ_{Total} = DJ_{Tx} + DJ_{Channel} + DJ_{Rx}
\]

\[
DJ = 143 \text{ps}
\]

\[
TJ = DJ + 14.069\sigma_{RJTotal}
\]

\[
TJ = 200 \text{ps}
\]

<table>
<thead>
<tr>
<th></th>
<th>$\sigma_{RJ}$ (ps)</th>
<th>DJ (ps)</th>
<th>TJ (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx</td>
<td>2.42</td>
<td>41</td>
<td>75</td>
</tr>
<tr>
<td>Channel</td>
<td>2.13</td>
<td>45</td>
<td>75</td>
</tr>
<tr>
<td>Rx</td>
<td>2.42</td>
<td>57</td>
<td>91</td>
</tr>
<tr>
<td>Total</td>
<td>4.03</td>
<td>143</td>
<td>200</td>
</tr>
</tbody>
</table>
Data Scrambling

- Channel jitter spec contains both DJ and RJ terms because...
- scrambling randomizes the bit stream...
- & makes channel jitter look like a truncated Gaussian
Data Scrambling

- Approximate channel jitter w/ the Dual Dirac model
- Channel jitter is specified by RJ & DJ
Data Scrambling

- Approximate channel jitter with the Dual Dirac model
- Channel jitter is specified by RJ & DJ

Scrambling allows us to avoid over-spec of jitter
Agenda

• Challenges
• Key Features
  • USB 3.0 Cable
  • Equalization
  • Scrambling
  • Compliance
  • Device Design
  • Low Frequency Periodic Signaling
• Summary
Compliance Testing

- **Goal:** Compliance test results that accurately predict product performance
- **Constraints:** Observability & Cost
- **Features:**
  - Compliance Fixtures
  - Compliance Patterns
  - Reference CTLE
  - Loopback BERT
Method:
• Transmit into compliance channel
• Measure $10^6$ UI @ TP1
• Post-process through the reference CTLE
• Extrapolate to $10^{-12}$ BER

<table>
<thead>
<tr>
<th>Spec</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Height</td>
<td>100</td>
<td>1200</td>
<td>mV</td>
</tr>
<tr>
<td>Dj</td>
<td>86</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>Rj</td>
<td>46</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>Tj</td>
<td>132</td>
<td>ps</td>
<td></td>
</tr>
</tbody>
</table>
Method:
- Rx in loopback mode
- Spread spectrum clocking (SSC) turned on
- Transmit scrambled D0.0 into compliance channel
- Inject 0.17UI RJ & the specified amount of sinusoidal jitter
- Measure either bit errors or symbol errors
Agenda

- Challenges
- Key Features
  - USB 3.0 Cable
  - Equalization
  - Scrambling
  - Compliance
- Device Design
- Low Frequency Periodic Signaling
- Summary
CTLE Training

Training the CTLE improves margins by 15-25mV & 5-15 ps
While the spec does not require DFE…

…it improves margin by up to~50mV & 20ps @ $10^{-12}$ BER
Non-interleaved Tx/Rx routing gives margin.

- **Pkg**: different layers or maximize inter-pair spacing
- **PCB**: different layers or 0.040+” between pairs on same layer

### Example Margins

<table>
<thead>
<tr>
<th>Dev Pkg Interleave</th>
<th>No</th>
<th>No</th>
<th>No</th>
<th>Yes</th>
<th>No</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dev PCB Space</td>
<td>0.020”</td>
<td>0.026”</td>
<td>0.040+”</td>
<td>0.020”</td>
<td>0.040+”</td>
</tr>
<tr>
<td>Host PCB</td>
<td>10.6” trace w/ 2 vias</td>
<td>12.6” w/ 3 vias</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Agenda

• Challenges
• Key Features
  • USB 3.0 Cable
  • Equalization
  • Scrambling
  • Compliance
  • Device Design
  • Low Frequency Periodic Signaling
• Summary
LFPS
Low Frequency Periodic Signaling

• Use:
  • Low power state exit
  • Polling for link training
  • Warm Reset

• Messages encoded via tBurst duration
  • Single burst for U1/U2 exit, U3 wakeup, Loopback exit, Warm Reset
LFPS Handshake

Examples:
U1/U2 Exit
U3 Wakeup

- LP1 initiates exit with LFPS burst (t11)
- LP2 detects & responds with LFPS burst (t12)
- LP1 detects & declares success
- LP2 transmits over min interval (t13-t11) & declares success
  - Valid timing ranges for the events depend upon power state
    - See table 6-22 for specific quantities
Key Messages

Keys to scaling USB to 5 Gb/s with legacy form factors & minimum cost impact:

- Use Moore’s Law
  - Value add in silicon: equalization, training
- Evolve Platform Technology
  - USB 3.0 cable
- Decrease Margin Requirements for Robustness
  - Jitter budgeting with scrambled data
  - Make compliance channel ≈ worst case application channel
Key Messages

Keys to scaling USB to 5 Gb/s with legacy form factors & minimum cost impact:

- Careful Device Design
  - Non-interleaved package/PCB
  - Advanced equalization

LFPS provides a mechanism for:

- Transition from low power state to SuperSpeed
- Forced link retraining via Warm Reset