Why USB On-the-Go?

- Transfer information between USB-enabled products without requiring a PC
- Throughput required to feel “instantaneous:”
  - Keystrokes 1-byte @ 50wpm = 33-bps
  - Pictures 1-MB per 1 sec = 8-Mbps
  - Music files 3-MB per 1 sec = 24-Mbps
- Do we need High Speed operation?
- We certainly want it – “instant gratification”
  - Share 20 songs or 60 pictures in 1 second!
  - Transfer 6-GBytes of data in 2 minutes at HS, instead of 1 hour and 20 minutes at FS
On-The-Go was specified to Support Full Speed and High Speed dual role devices

- Software Architecture
- Implementation
- On-The-Go Protocols
- Mechanicals
- Compliance Program

Higher Bandwidth and faster signaling does create some new issues
Challenges to High Speed On-the-Go Operation

- Power consumption
- Dual Role Controller Architecture
- Transceiver standard for High Speed OTG
Challenges to High Speed On-the-Go Operation

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Power Consumption

- The 8mA of Host-supplied bus power insufficient to drive even FS devices
- OTG Bus Power will enable a handful of Low Bandwidth bus powered devices
- All High Speed and most Full Speed OTG devices will be self powered
- Battery life is the real issue
  - *Energy* consumption, not *power* consumption
- How do LS, FS and HS compare?
Energy to Transfer 1-MB Data Payload

"Specification" Data Transfer Rate (Mbps)

Aggressively Manage HS Power

HS USB is more energy-efficient than FS or LS!
Challenges to High Speed On-the-Go Operation

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Elements of High Speed Dual Role Controller

- Device Software Stack
  - Device Controller Interface
    - HS/FS Device Controller
      - System Interface
      - Endpoint Resources
      - HS/FS Speed SIE
  - HS Host Controller Interface
    - HS Host Controller
      - System Interface
      - Transaction Scheduler
      - High Speed SIE
  - FS/LS Host Controller Interface
    - LS/FS Host Controller
      - System Interface
      - Transaction Scheduler
      - FS/LS Speed SIE
- Transceiver
  - HS Transceiver
  - FS/LS Transceiver
  - OTG Functions
- Host Software Stack
- OTG State Machines

June 12, 2002
USB 2.0 Host Controller

- Allows port functionality regardless of OS version
  - USB 1.1 OS will ‘just work’ as USB 1.1 ports
- USB 1.1 HCs can go away over time
  - Replaced with integrated USB 2.0 Hub

Credit: John Howard, Intel
October 10, 2000
USB 2.0 Hub

- Hub controller same as USB1.1
- Routing logic connects device to appropriate path

Credit: John Howard, Intel
October 10, 2000
PC Architecture Not Suited to Embedded Application

- Lots of redundant Hardware
- Different data models for HS traffic than for FS or LS traffic
- Multiple Control and Status register sets with redundant information
- Creates unwanted host software complexity for HS USB OTG
Simplified High Speed Dual Role Controller

Host Software Stack
Device Software Stack
OTG State Machines

Dual Role Controller Interface

Dual Role Controller
System Interface

Transaction Scheduler
Transaction Translator
Endpoint Resources

HS/FS/LS SIE

Transceiver

HS/FS/LS Transceiver
OTG Functions

OTG State Machines

Host Software Stack
Device Software Stack

OTG State Machines

Dual Role Controller Interface

Dual Role Controller
System Interface

Transaction Scheduler
Transaction Translator
Endpoint Resources

HS/FS/LS SIE

Transceiver

HS/FS/LS Transceiver
OTG Functions

June 12, 2002
Challenges to High Speed On-the-Go Operation

- Power consumption
- Dual Role Controller Architecture
- Transceiver proposal for High Speed OTG
Benefits of a specification

- Multiple vendor support
- Acceleration of USB product development
- Reduction of the speed on the interface allows for easy integration into ASIC’s

Same Goals as UTMI
UTMI Requires Extension

- UTMI was only defined for USB peripheral development
  - No OTG support
    - Vbus sense and control
    - Session control
  - No Host Controller support
    - Bus signaling control
    - Low speed support
UTMI+ Overview

- Backwards compatible with UTMI as currently defined (Latest release v1.05, March 29, 2001)
- Uniform/Standard non-proprietary interface
- Enhancement of the UTMI interface
  - For On-the-Go
  - For host controllers
- Layered implementation approach
**UTMI+ Proposed Levels**

- **Level 0**
  - The UTMI+ is the same as UTMI

- **Level 1**
  - Addition of host and OTG
  - Only HS and FS

- **Level 2**
  - Direct connect LS support

- **Level 3**
  - Full speed hub support
    - Addition of LS preamble

**UTMI+ level 0 = UTMI spec. version 1.05**

**USB2.0 peripherals only**

**UTMI+ level 1**

USB2.0 peripheral, host controllers, On-the-Go devices
(HS, FS, LS only)

**UTMI+ level 2**

USB2.0 peripheral, host controllers, On-the-Go devices
(HS, FS, LS but no hub support)

**UTMI+ level 3**

USB2.0 peripheral, host controllers, On-the-Go devices
(HS, FS, LS with hub support)
Level 1 Additions to UTMI

- Distinguish between mini-A and mini-B receptacle for dual role peripheral
- Sensing of USB bus power
- Driving of the USB bus power to feed current, to charge and to discharge Vbus
- Control over the Dp & Dm pull-down resistors
- Detection of HS-peripheral disconnect
Level 2 & 3 Additions to UTMI

- **Level 2** – Direct connect Low Speed Support
  - LS data rate
  - LS keep-alive packets on a Low Speed USB ports
  - LS edge rate control

- **Level 3** – Full Speed Hub support
  - Switching to Low Speed within a transaction
  - Low Speed Preamble PID (PRE-PID)

12 Additional Signals
Macrocell Signal Overview

**UTMI (8 bit)**
- Total of 33 signals required
- Optional 13 vendor specific signals

**UTMI (16 bit)**
- 18 additional signals

**UTMI+**
- 12 additional signals
Discrete Interface Pin Count

- UTMI+ as currently defined only suited for Macrocell implementation

- What about discrete transceiver?
  - Minimal number of pins is highest priority
  - Preferred to have one spec. for both discrete and macrocell

Feasibility Study in Progress
Two Specification Tasks in Progress

- **UTMI+ for Macrocell**
  - Targeting a simple on chip interface
  - Based on Philips proposal

- **A low pin count solution for discrete transceiver**
  - Targeting a low Pin count solution.
  - 14-18 signal transceiver to SIE interface
  - 8-bit parallel bidirectional data bus
Unifying the Two Efforts

- Common module with two possible interfaces
  - Or
  - One a layered hierarchical solution
    - One interface a sub-module of the other
Recap: High Speed USB OTG

- Energy consumption is the issue, not power
  - High Speed is more efficient than FS or LS for large transfers
  - Manage power by aggressively using the suspend and session end protocols

- Embedded Controller Architectures to support HS OTG are arriving in the market place
  - Pay attention to the software interface, and the requirements of your application

- A Transceiver interface standard is in process
  - Leverage industry experience in UTMI and FS OTG
Call to Action

- Systems houses
  - Make plans to put Mobile High bandwidth capability into the hands of consumers

- Silicon and IP providers
  - Review and accept a High Speed capable OTG transceiver Interface standard.
  - Enable High Speed USB On-The-Go at the system and controller level
About ARC International

- USB cores formerly sold as VAutomation, Inc.
  - Acquired by ARC™ in March 2000
  - ARC provides RISC CPU, DSP, peripherals, software and development tools for system-on-chip designs

- Soft IP cores for USB
- USB Now™ Integrated System Solution
  - Full speed / Low speed
    - Device
    - Dual-role Host and Device OTG controller
  - High speed
    - Device
    - Dual-role Host and Device OTG controller
Among the top 10 semiconductor companies
- $4.4b in revenues for 2001
- Automotive, Consumer, Communications, Computing, Industrial & Home Appliances, Identification and Networking markets

USB Solutions : Discrete & Embedded
- Strong Player in developing USB standard
- FlexiUSB Architecture : Flexibility, Cost, TTM, Quality
- Industry’s first OTG prototype
  - HS : Transceiver, Host, Device, Hub, Host/Device
  - FS : Transceiver, Host, Device, Hub
  - OTG : Transceiver, Host
Further Information

- **ARC International:**
  - [www.ARC.com](http://www.ARC.com)
  - Device, Host and OTG Controller IP

- **Philips Semiconductors:**
  - [http://www.semiconductors.philips.com/buses/usb](http://www.semiconductors.philips.com/buses/usb)
  - USB chips, IP, and systems

- **OTG email reflector:**
  - [www.usb.org/developers/ontheago](http://www.usb.org/developers/ontheago)
  - UTMI+ specification discussion