



SuperSpeed USB Developers Conference

San Jose, California
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Physical Layer (PHY) Specification

Howard Heck

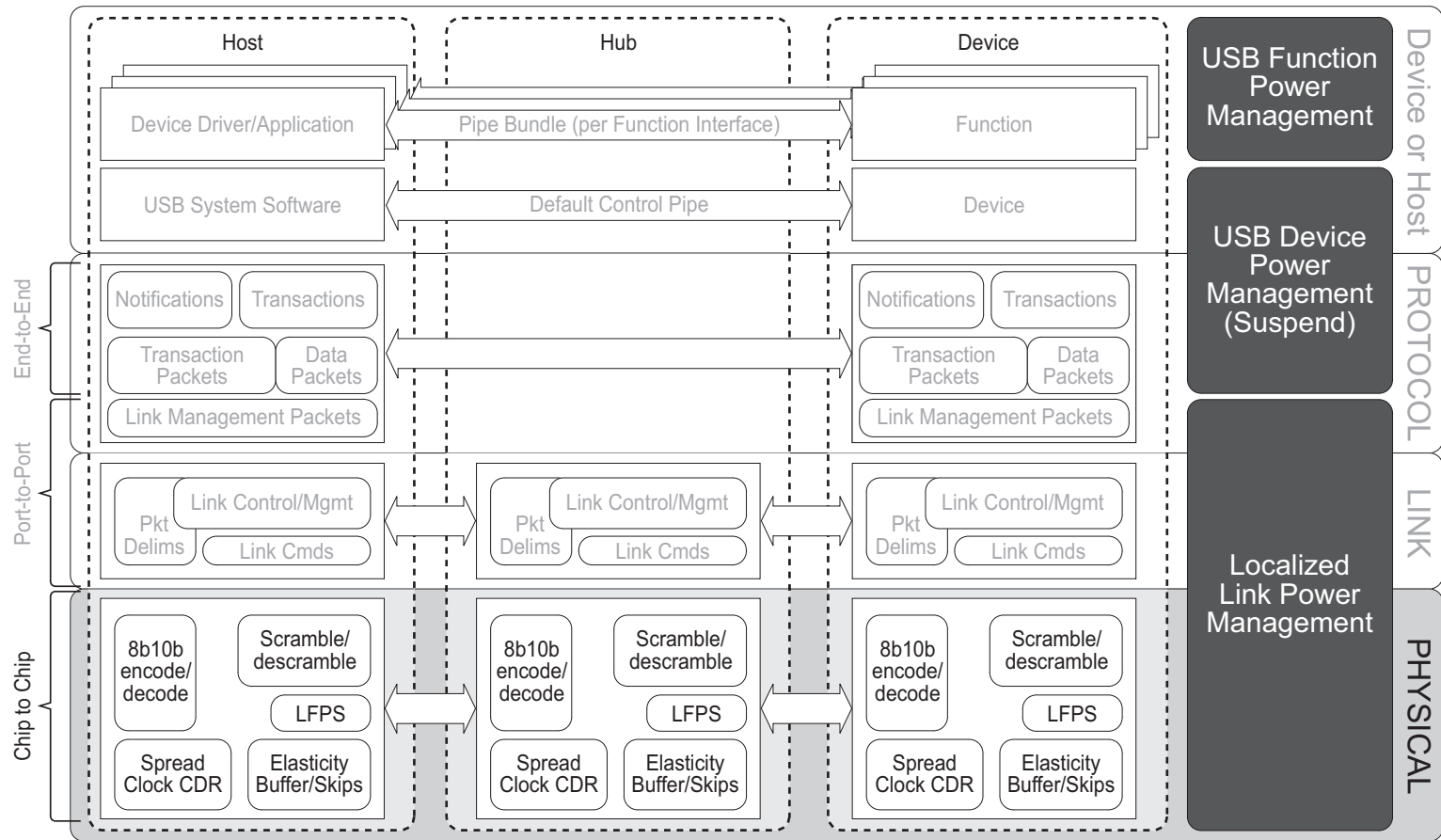
Principal Engineer
Intel Corporation



Agenda

- Challenges & Focus
- Key Features for 5 Gb/s SuperSpeed USB
 - USB 3.0 Cable
 - Equalization
 - Scrambling
 - Compliance Channel & Methodology
 - Low Frequency Periodic Signaling
- Summary

Where Are We?





Challenges & Focus

Challenges:

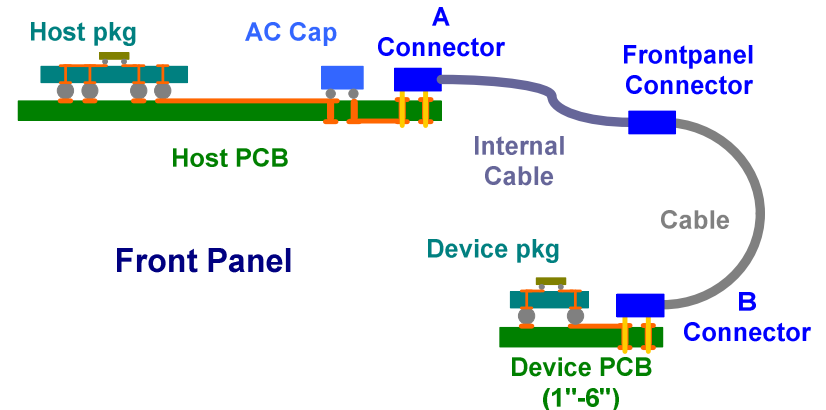
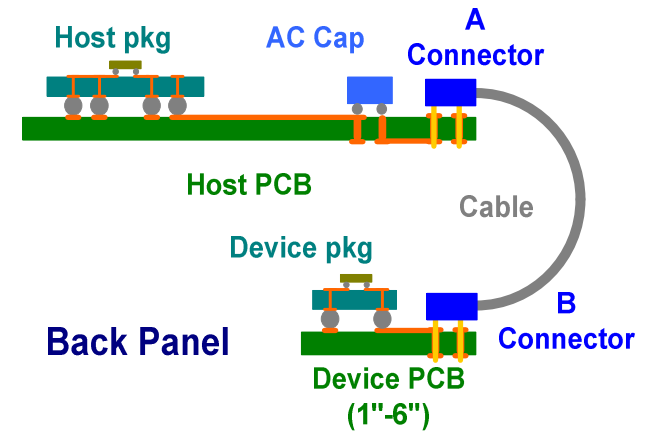
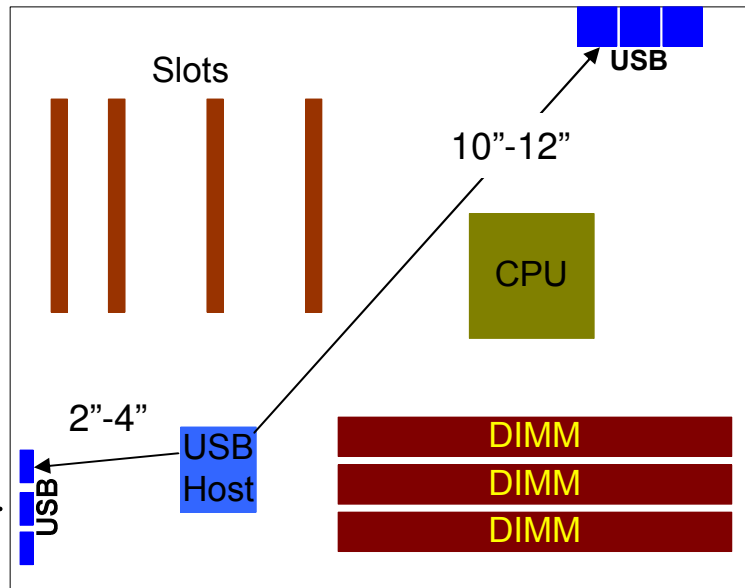
- 5 Gb/s data rate
- Low cost
 - 4 layer PCB, extension of USB cable technology
- Same design & usage flexibility as USB 2.0
 - front panel & back panel connectors, up to 3 m cable
- Robust compliance testing methodology
 - Strong correlation to actual performance
- Transition out of low power states

Our focus: features that get us to 5 Gb/s

PHY Overview



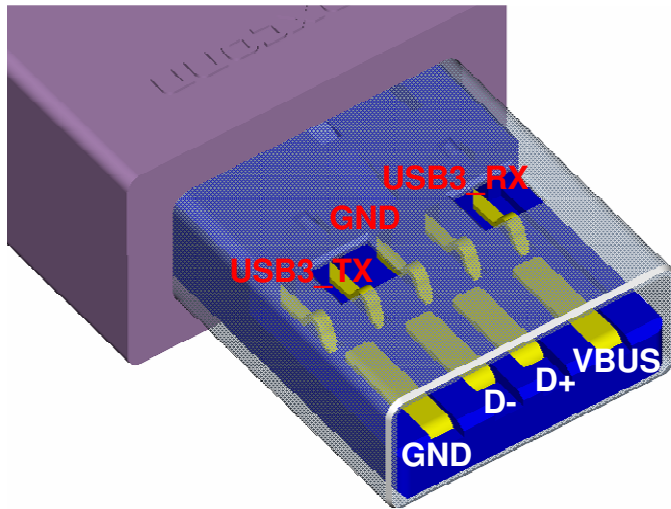
Back Panel



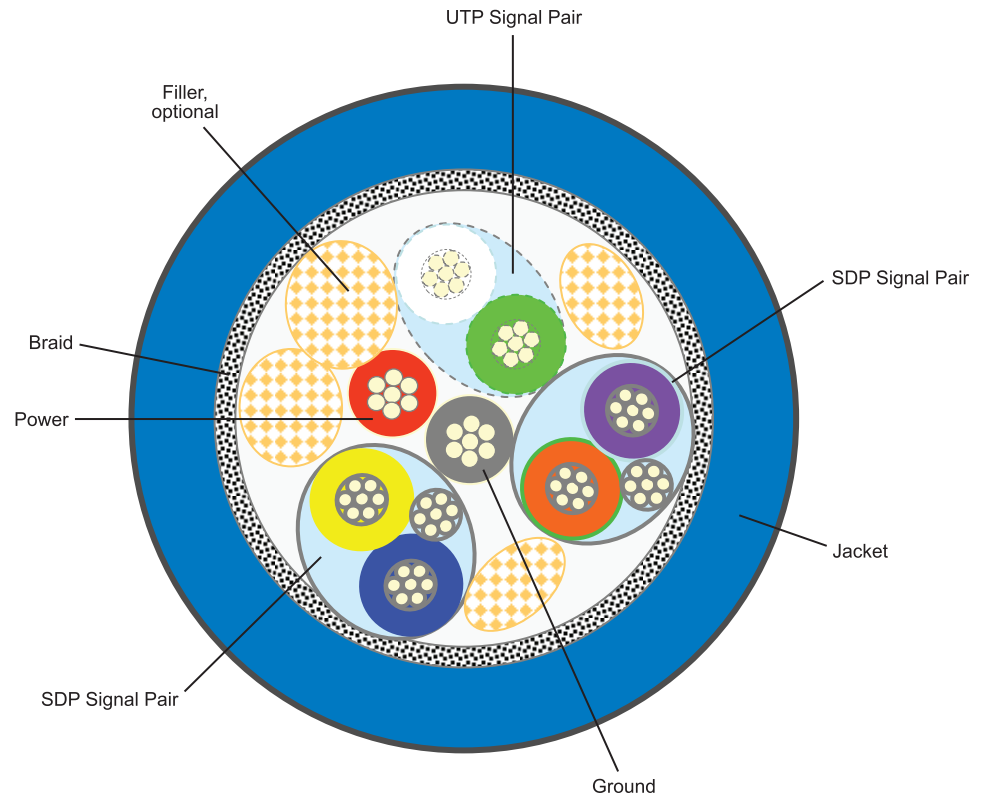
Channel characteristics:

- 2"-12" host PCB length
- 0m to 3m cable
- 1"- 6" device PCB length

USB 3.0 Cable Assembly



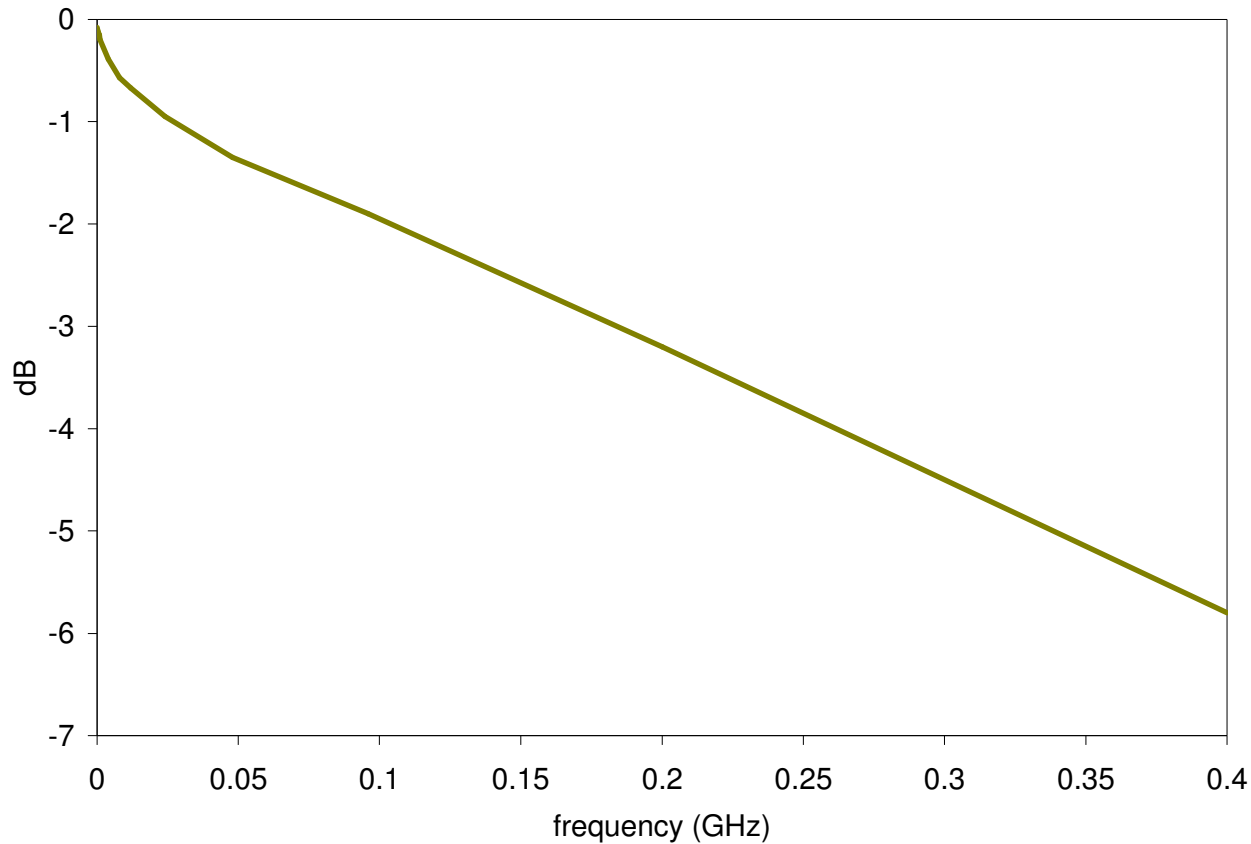
New features added to the cable assembly for SuperSpeed USB operation



USB 3.0 Cable Assembly



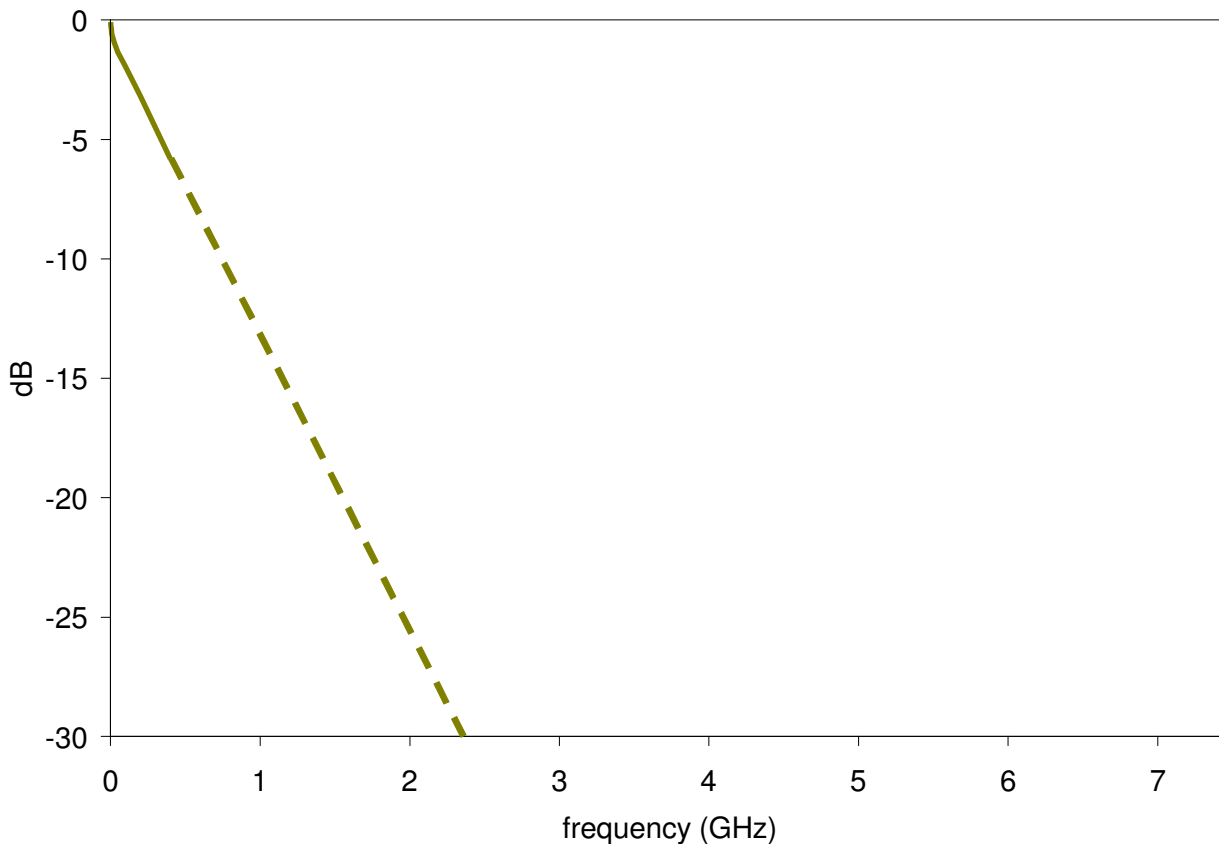
USB 2.0 Cable Attenuation Spec



USB 3.0 Cable Assembly

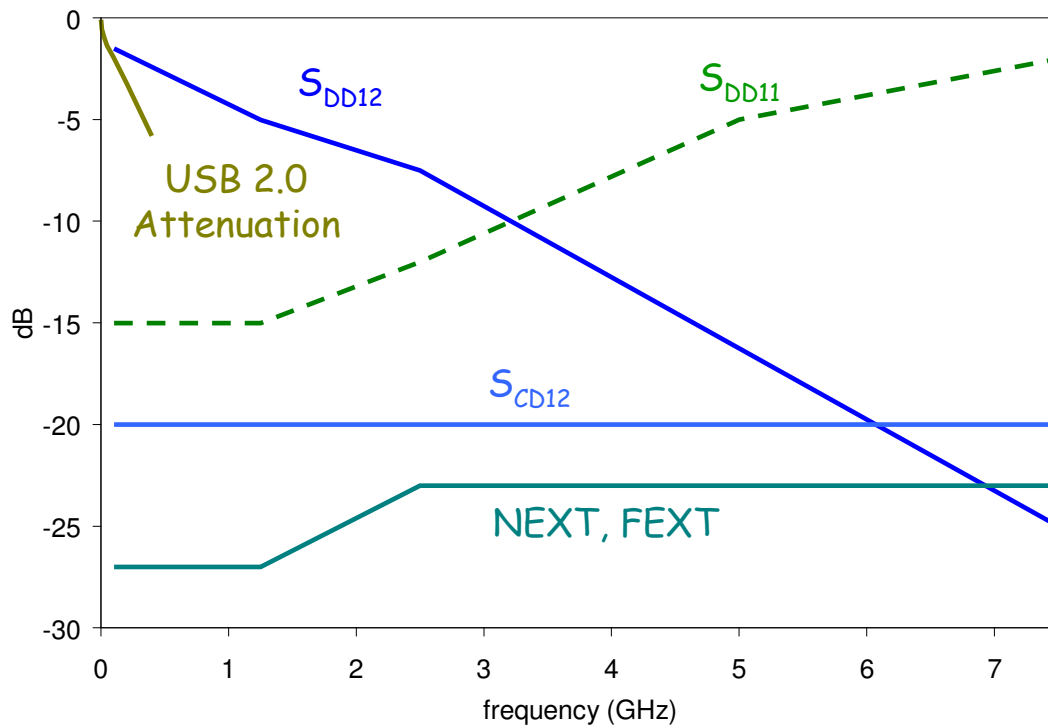


USB 2.0 Cable Attenuation Spec



- 5 Gb/s Requires:
- Extension to 5+ GHz
 - Reduced attenuation

USB 3.0 Cable Assembly

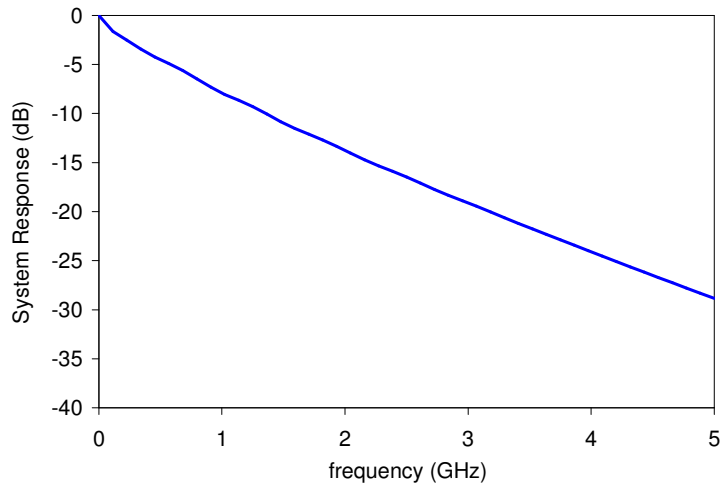


SuperSpeed USB specs:

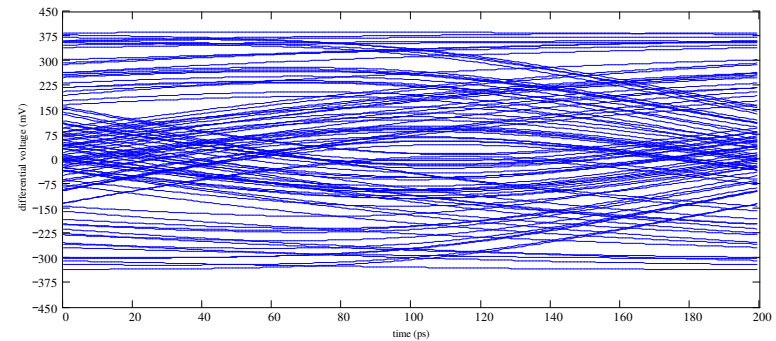
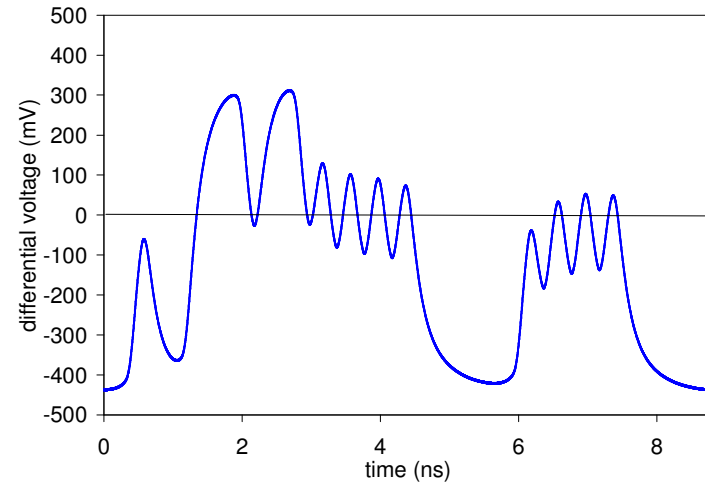
- Attenuation (S_{DD12})
- Crosstalk (NEXT, FEXT)
- Differential-to-Common mode conversion (S_{CD12})
- Return Loss (S_{DD11})
- Characteristic Impedance

USB 3.0 specs make sure cable assemblies support 5 Gb/s transfer rate

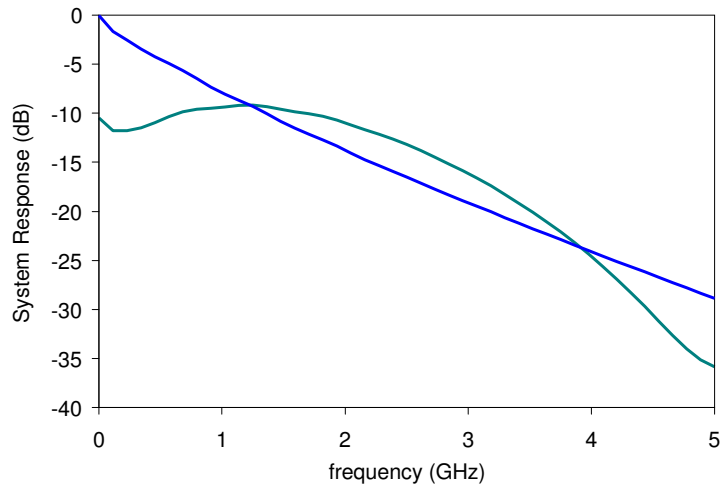
Equalization



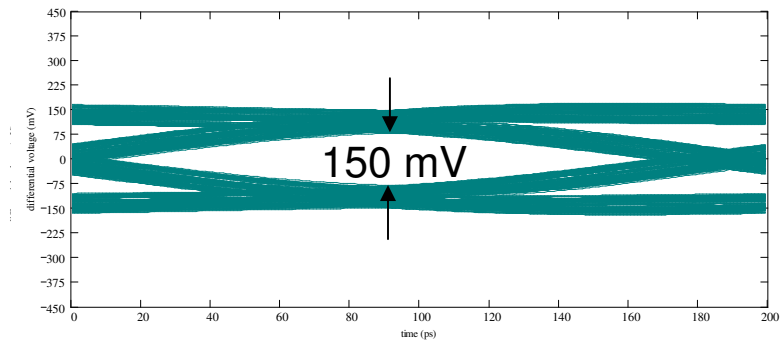
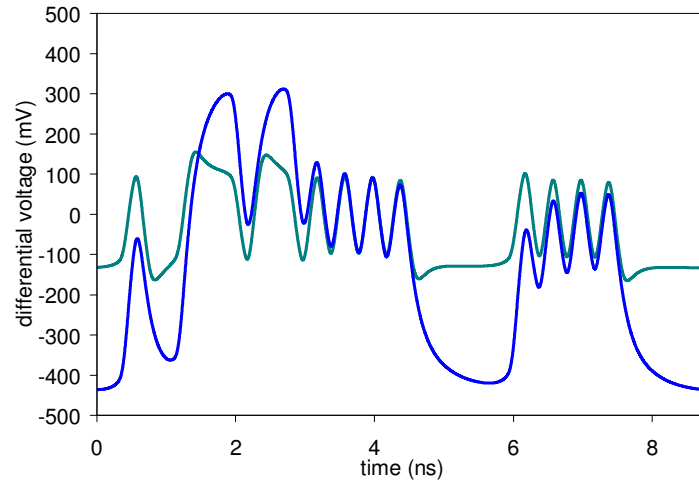
Frequency dependent loss closes the 5 Gb/s eye



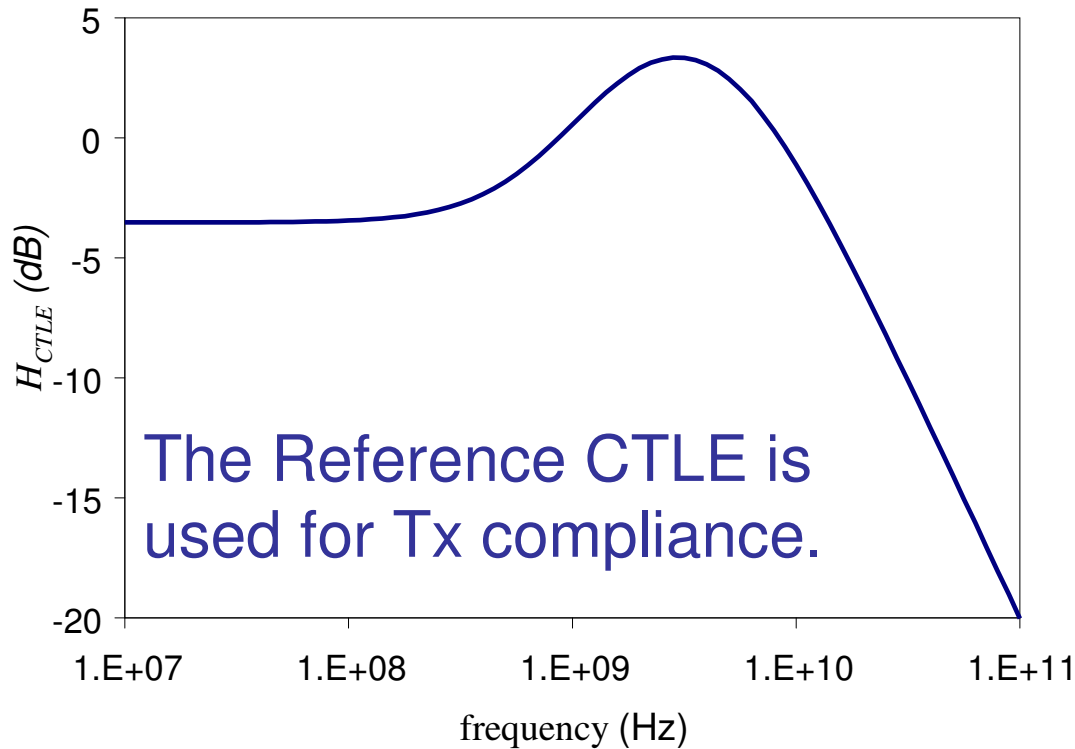
Equalization



Equalization opens up the 5 Gb/s data eye



Receiver CTLE



Ref CTLE Parameters

DC Gain	-3.5dB
AC-DC Gain	6.9dB
Gain BW	10 GHz
f_{zero}	650 MHz
f_{p1}	1.95 GHz
f_{p2}	5 GHz

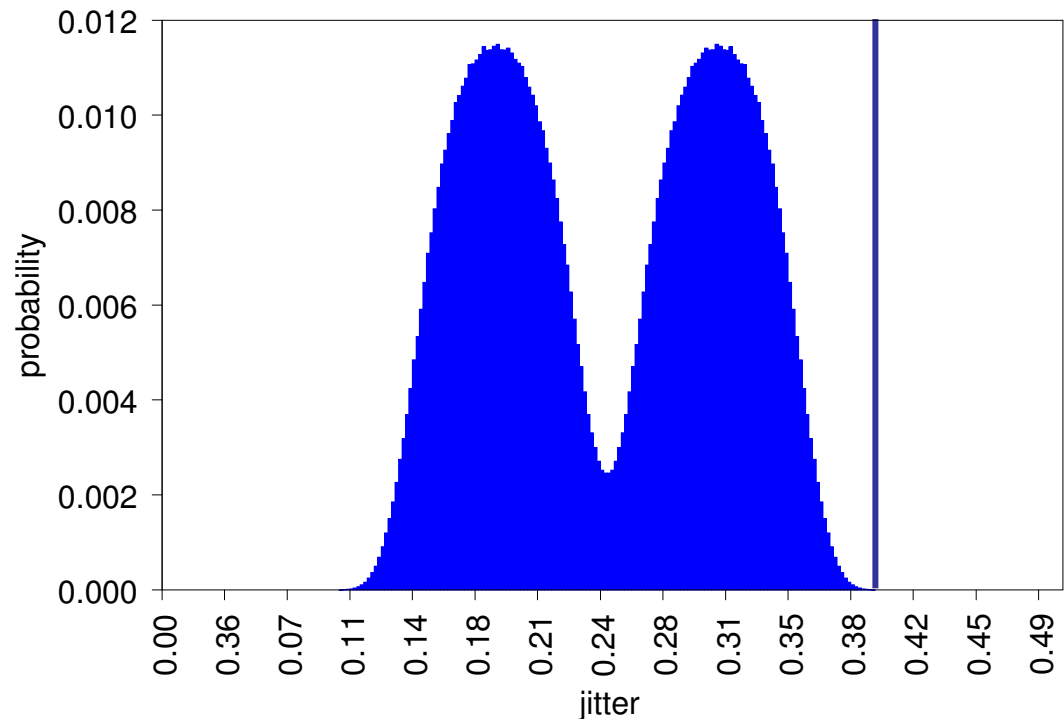
TSEQ is transmitted 2^{16} times at initialization to allow adaptive optimization of the CTLE

Data Scrambling



- Channel jitter spec contains both DJ and RJ terms
- Scrambling randomizes the bit stream
- Channel jitter looks like a truncated Gaussian

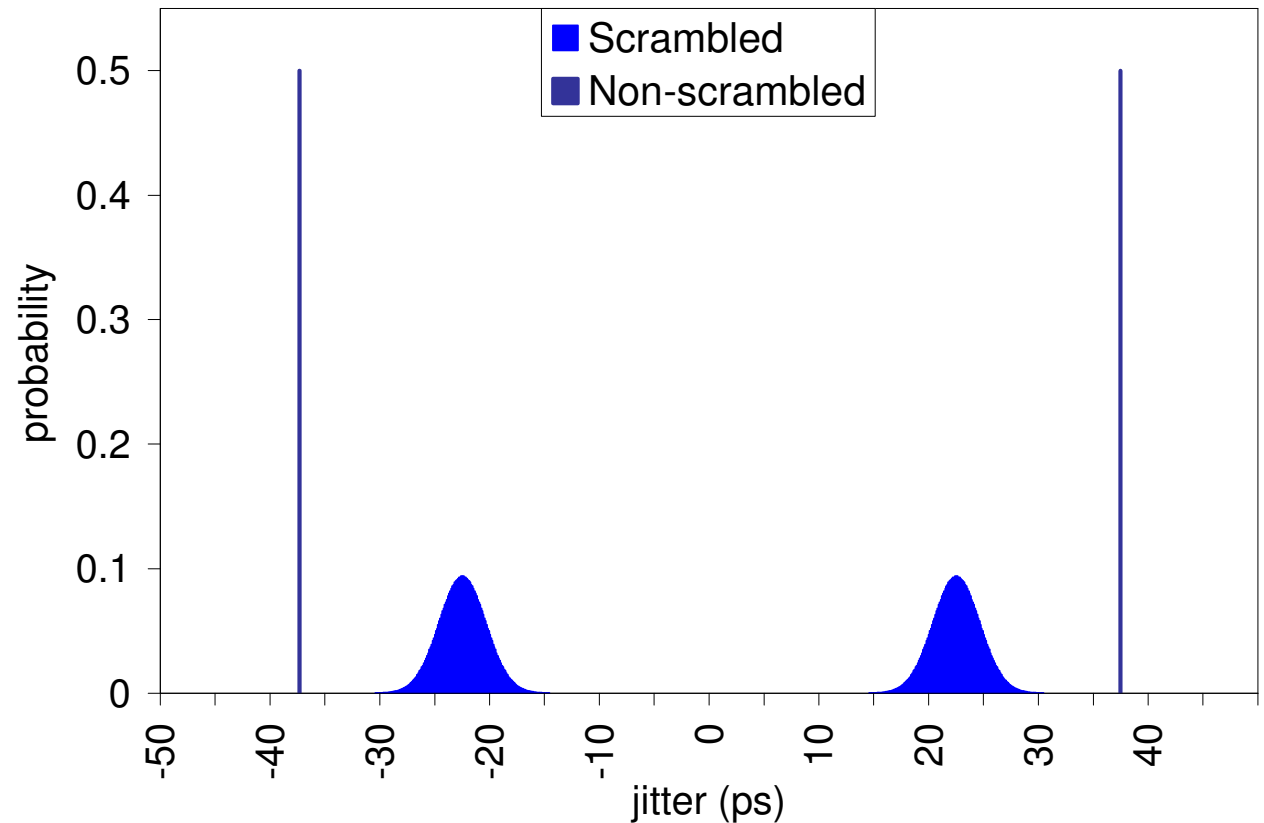
Channel Jitter PDF Example



Data Scrambling



- We can approximate channel jitter with the Dual Dirac model
- Channel jitter is specified by RJ & DJ

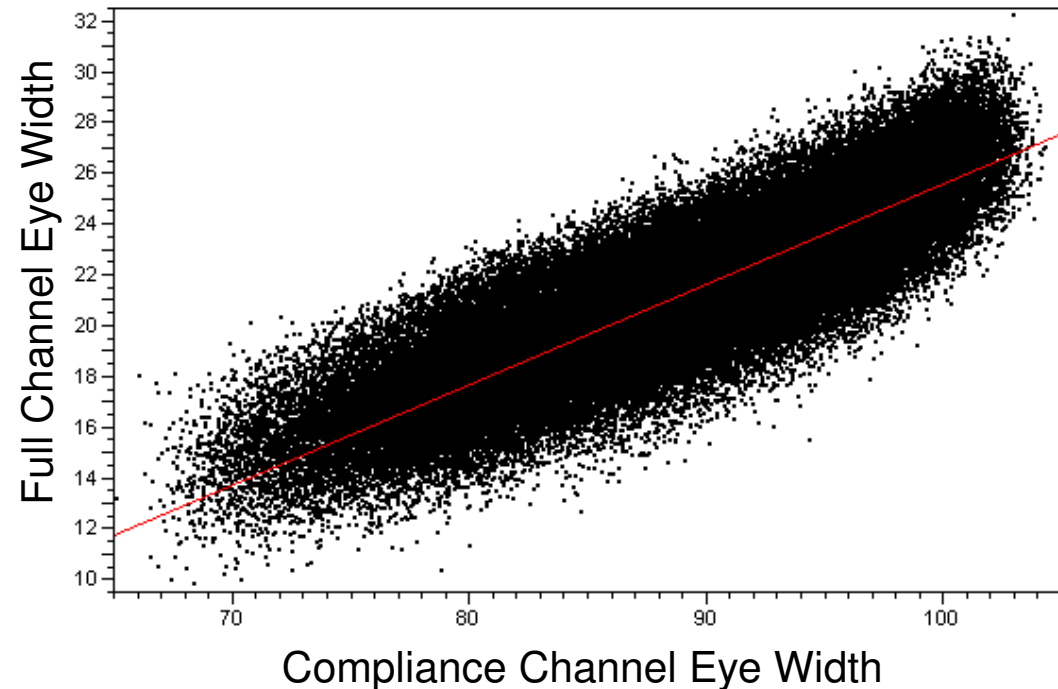


Scrambling allows us to avoid over-spec of jitter

Compliance Testing



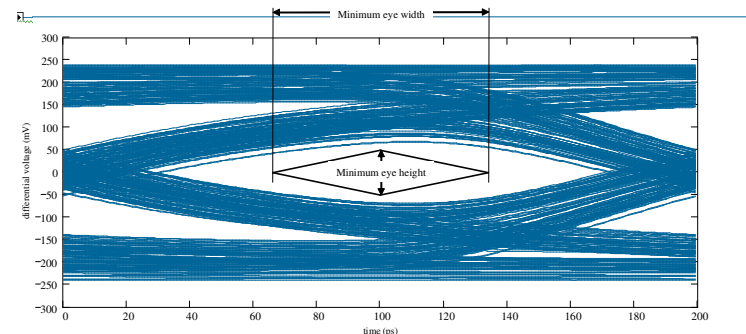
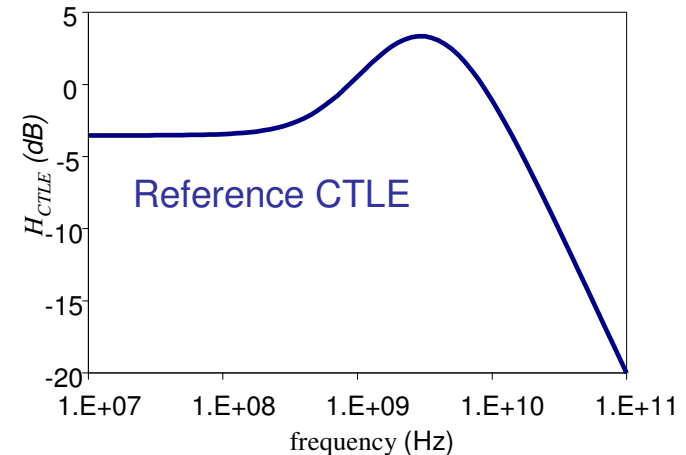
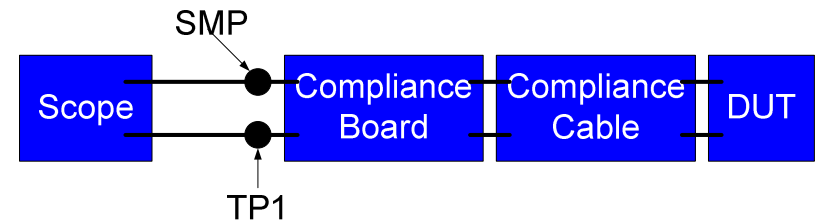
- **Goal:** Compliance test results that accurately predict product performance
- **Constraints:** Observability & Cost
- **Features:**
 - Compliance Fixtures
 - Compliance Patterns
 - Reference CTLE
 - Loopback BERT



Transmitter Jitter Compliance

Method:

- Transmit into compliance channel
- Measure @ TP1
- 10^6 consecutive UI
- Post-process through the reference CTLE
- Extrapolate to 10^{-12} BER



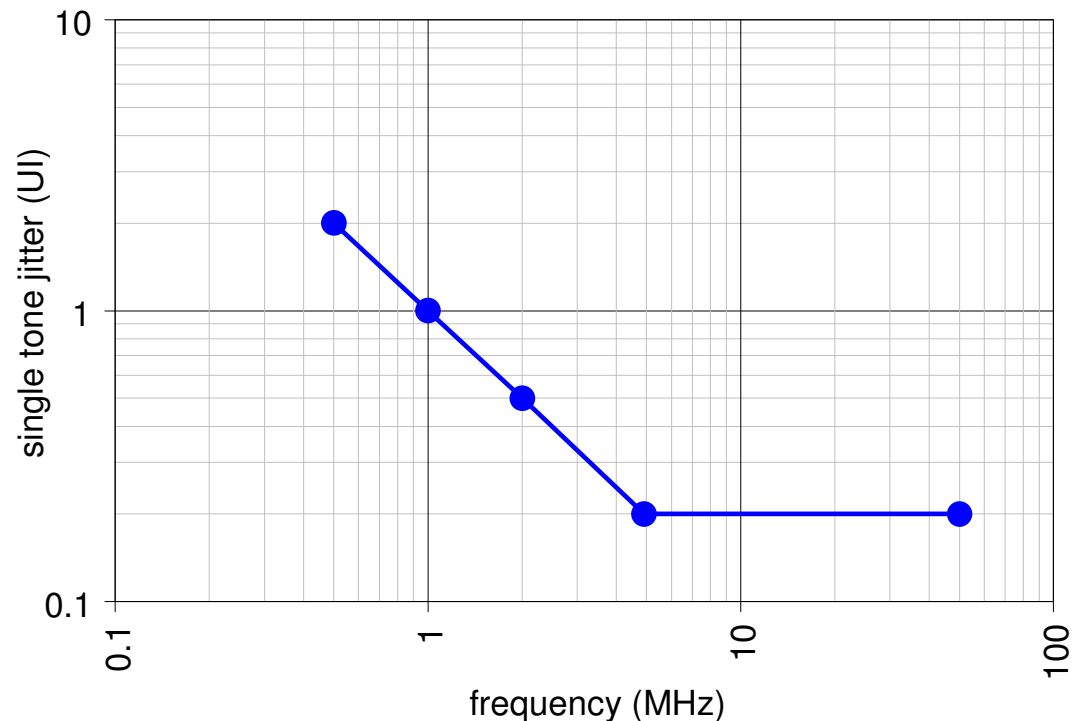
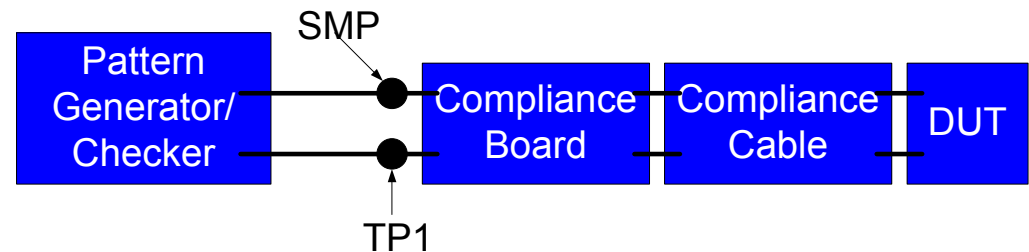
Spec	Min	Max	Units
Eye Height	100	1200	mV
Dj		0.465	UI
Rj		0.30	UI
Tj		0.66	UI

Receiver Jitter Compliance



Method:

- Rx in loopback mode
- Spread spectrum clocking (SSC) turned on
- Transmit scrambled D0.0 into compliance channel
- Inject 0.17UI RJ & the specified amount of sinusoidal jitter
- Use external BERT or Rx BERT



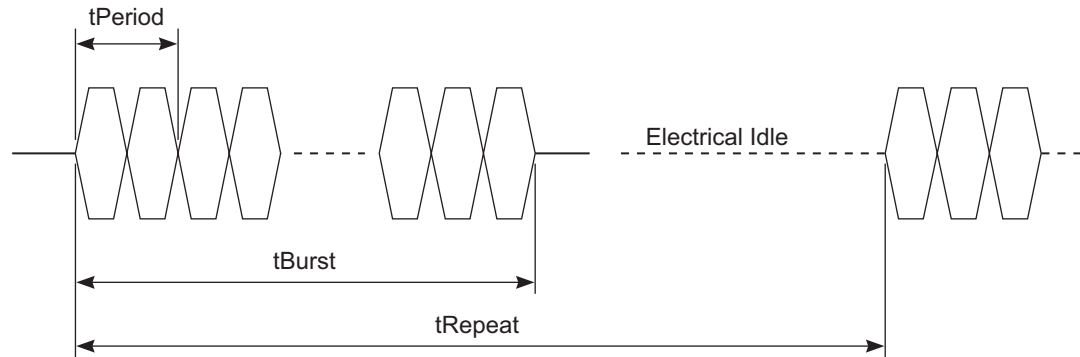
LFPS

Low Frequency Periodic Signaling



- Use:

- Low power state exit
- Polling for link training
- Warm Reset



U-032

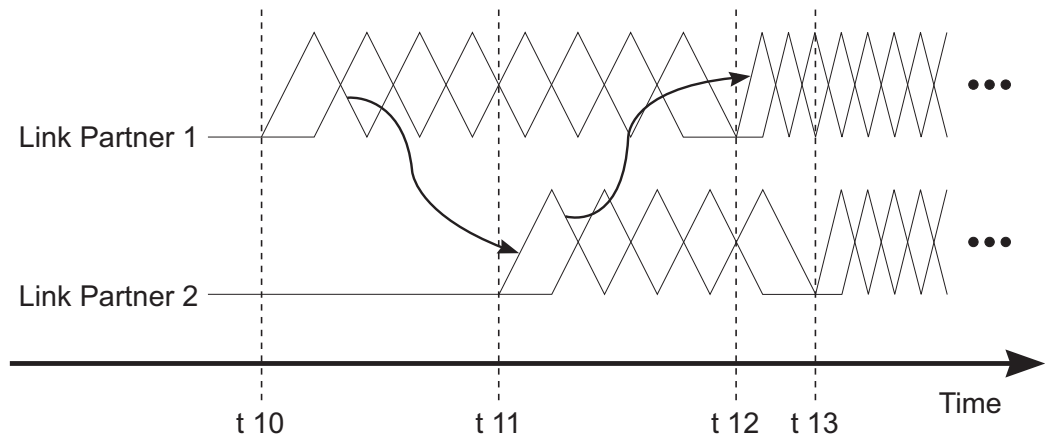
- Messages encoded via t_{Burst} duration

- Single burst for U1/U2 exit, U3 wakeup, Loopback exit, Warm Reset

LFPS Handshake



Examples:
U1/U2 Exit
U3 Wakeup



- LP1 initiates exit with LFPS burst (t_{11})
- LP2 detects & responds with LFPS burst (t_{12})
- LP1 detects & declares success
- LP2 transmits over min interval ($t_{13}-t_{11}$) & declares success
- Valid timing ranges for the events depend upon power state
 - See table 6-22 for specific quantities



Summary

- SuperSpeed USB features create data rate scalability to 5 Gb/s while maintaining compatibility with legacy form factors:
 - high performance cable assembly
 - adaptive equalization
 - data scrambling
 - compliance testing methodology
- LFPS gives a mechanism for
 - recovery from low power states
 - forced link retraining via Warm Reset



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