

Universal Serial Bus 3.0 Link Layer Test Specification

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Contents

1	INTRODUCTION	5
2	TERMS AND ABBREVIATIONS	6
3	TEST ASSERTIONS	7
	Assertion #	7
	Assertion Description	7
	Test #	7
	Chapter 7 Test Assertions: Link Layer	7
	Subsection reference: 7.2 Link Management and Flow Control	7
	Subsection reference: 7.2.1.1 Header Packet Structure	7
	Subsection reference: 7.2.1.1.1 Header Packet Framing	7
	Subsection reference: 7.2.1.1.2 Packet Header	7
	Subsection reference: 7.2.1.1.3 Link Control Word	7
	Subsection reference: 7.2.1.2.1 Data Packet Payload Framing	7
	Subsection reference: 7.2.1.2.2 Data Packet Payload	7
	Subsection reference: 7.2.2.1 Link Command Structure	7
	Subsection reference: 7.2.2.2 Link Command Word Definition	8
	Subsection reference: 7.2.2.3 Link Command Placement	8
	Subsection reference: 7.2.4 Link Command Usage for Flow Control, Error Recovery, and Power Management	8
	Subsection reference: 7.2.4.1 Header Packet Flow Control and Error Recovery	8
	Subsection reference: 7.2.4.1.1 Initialization	8
	Subsection reference: 7.2.4.1.2 General Rules of LGOOD_n and LCRD_x Usage	10
	Subsection reference: 7.2.4.1.3 Transmitting Header Packets	10
	Subsection reference: 7.2.4.1.4 Receiving Header Packets	10
	Subsection reference: 7.2.4.1.6 Receiving Data Packet Payload	10
	Subsection reference: 7.2.4.1.10 Transmitting Timers	11
	Subsection reference: 7.2.4.2.1 Power Management Link Timers	11
	Subsection reference: 7.2.4.2.2 Low Power Link State Initiation	11
	Subsection reference: 7.2.4.2.3 U1/U2 Entry Flow	12
	Subsection reference: 7.2.4.2.4 U3 Entry Flow	13
	Subsection reference: 7.2.4.2.5 Concurrent Low Power Link Management Flow	13
	Subsection reference: 7.2.4.2.6 Concurrent Low Power Link Management and Recovery Flow	14
	Subsection reference: 7.2.4.2.7 Low Power Link State Exit Flow	14
	Subsection reference: 7.3 Link Error Rules/Recovery	14
	Subsection reference: 7.3.4 Link Commands Errors	14
	Subsection reference: 7.3.5 ACK Tx Header Sequence Number Errors	14
	Subsection reference: 7.3.6 Header Sequence Number Advertisement Errors	15
	Subsection reference: 7.3.7 Rx Header Buffer Credit Advertisement Errors	15
	Subsection reference: 7.3.8 Training Sequence Error	15
	Subsection reference: 7.4 PowerOn Reset and Inband Reset	15
	Subsection reference: 7.4.1 Power On Reset	15
	Subsection reference: 7.4.2 Inband Reset	16
	Subsection reference: 7.5 Link Training and Status State Machine (LTSSM)	17

Subsection reference: 7.5.1 SS.Disabled	17
Subsection reference: 7.5.1.1 SS.Disabled Requirements	17
Subsection reference: 7.5.1.2 Exit from SS.Disabled	17
Subsection reference: 7.5.2 SS.Inactive	17
Subsection reference: 7.5.2.3 SS.Inactive.Quiet	17
Subsection reference: 7.5.2.3.1 SS.Inactive.Quiet Requirement	17
Subsection reference: 7.5.2.3.2 Exit from SS.Inactive.Quiet	17
Subsection reference: 7.5.2.4 SS.Inactive.Disconnect.Detect	17
Subsection reference: 7.5.2.4.1 SS.Inactive.Disconnect.Detect Requirements	17
Subsection reference: 7.5.2.4.2 Exit from SS.Inactive.Disconnect.Detect	17
Subsection reference: 7.5.3 Rx.Detect.....	17
Subsection reference: 7.5.3.3 Rx.Detect.Reset	18
Subsection reference: 7.5.3.3.1 Rx.Detect.Reset Requirements	18
Subsection reference: 7.5.3.3.2 Exit from Rx.Detect.Reset.....	18
Subsection reference: 7.5.3.4 Rx.Detect.Active	18
Subsection reference: 7.5.3.5 Rx.Detect.Active Requirement.....	18
Subsection reference: 7.5.3.6 Exit from Rx.Detect.Active	18
Subsection reference: 7.5.3.7 Rx.Detect.Quiet	18
Subsection reference: 7.5.3.7.1 Rx.Detect.Quiet Requirements	19
Subsection reference: 7.5.3.7.2 Exit from Rx.Detect.Quiet.....	19
Subsection reference: 7.5.4 Polling	19
Subsection reference: 7.5.4.3 Polling.LFPS	19
Subsection reference: 7.5.4.3.1 Polling.LFPS Requirements	19
Subsection reference: 7.5.4.3.2 Exit from Polling.LFPS	19
Subsection reference: 7.5.4.4 Polling.RxEQ	19
Subsection reference: 7.5.4.4.1 Polling.RxEQ Requirements	19
Subsection reference: 7.5.4.4.2 Exit from Polling.RxEQ	20
Subsection reference: 7.5.4.5 Polling.Active.....	20
Subsection reference: 7.5.4.5.1 Polling.Active Requirements.....	20
Subsection reference: 7.5.4.5.2 Exit from Polling.Active	20
Subsection reference: 7.5.4.6 Polling.Configuration	20
Subsection reference: 7.5.4.6.1 Polling.Configuration Requirements	20
Subsection reference: 7.5.4.6.2 Exit from Polling.Configuration.....	21
Subsection reference: 7.5.4.7 Polling.Idle	21
Subsection reference: 7.5.4.7.1 Polling.Idle Requirements	21
Subsection reference: 7.5.4.7.2 Exit form Polling.Idle.....	21
Subsection reference: 7.5.5 Compliance Mode	22
Subsection reference: 7.5.5.1 Compliance Mode Requirements	22
Subsection reference: 7.5.5.2 Exit from Compliance Mode	22
Subsection reference: 7.5.6 U0.....	22
Subsection reference: 7.5.6.1 U0 Requirements.....	22
Subsection reference: 7.5.6.2 Exit from U0.....	23
Subsection reference: 7.5.7 U1.....	23
Subsection reference : 7.5.7.1 U1 Requirements.....	23
Subsection reference: 7.5.7.2 Exit from U1.....	23
Subsection reference: 7.5.8 U2.....	24
Subsection reference: 7.5.8.1 U2 Requirements.....	24
Subsection reference: 7.5.8.2 Exit from U2.....	24
Subsection reference: 7.5.9 U3.....	24
Subsection reference: 7.5.9.1 U3 Requirements.....	24
Subsection reference: 7.5.9.2 Exit from U3.....	25
Subsection reference: 7.5.10 Recovery	25
Subsection reference: 7.5.10.3 Recovery.Active	25
Subsection reference: 7.5.10.3.1 Recovery.Active Requirements	25
Subsection reference: 7.5.10.3.2 Exit from Recovery.Active.....	25
Subsection reference: 7.5.10.4 Recovery.Configuration	26

Subsection reference: 7.5.10.4.1 Recovery.Configuration Requirements	26
Subsection reference: 7.5.10.4.2 Exit from Recovery.Configuration	26
Subsection reference: 7.5.10.5 Recovery.Idle	26
Subsection reference: 7.5.10.5.1 Recovery.Idle Requirements	26
Subsection reference: 7.5.10.5.2 Exit from Recovery.Idle	27
Subsection reference: 7.5.11 Loopback.....	27
Subsection reference: 7.5.11.3.1 Loopback.Active Requirements	27
Subsection reference: 7.5.11.3.2 Exit from Loopback.Active	27
Subsection reference: 7.5.11.4 Loopback.Exit	28
Subsection reference: 7.5.11.4.1 Loopback.Exit Requirements	28
Subsection reference: 7.5.11.4.2 Exit from Loopback.Exit	28
Subsection reference: 7.5.12 Hot Reset.....	28
Subsection reference: 7.5.12.2 Hot Reset Requirements	28
Subsection reference: 7.5.12.3 Hot Reset.Active	28
Subsection reference: 7.5.12.3.1 Hot Reset.Active Requirements	28
Subsection reference: 7.5.12.3.2 Exit from Hot Reset.Active	28
Subsection reference: 7.5.12.4 Hot Reset.Exit	29
Subsection reference: 7.5.12.4.1 Hot Reset.Exit Requirements	29
Subsection reference: 7.5.12.4.2 Exit from Hot Reset.Exit	29
Chapter 8 Test Assertions: Protocol Layer	29
Subsection reference: 8.3 Packet Formats	29
Subsection reference: 8.3.1 Fields Common to all Headers	29
Subsection reference: 8.3.1.1 Reserved Values and Reserved Field Handling	29
Subsection reference: 8.4 Link Management Packet (LMP)	29
Subsection reference: 8.4.2 Set Link Function	29
Subsection reference: 8.4.4 Vendor Device Test.....	29
Subsection reference: 8.4.5 Port Capabilities	30
Subsection reference: 8.4.6 Port Configuration.....	30
Subsection reference: 8.4.7 Port Configuration Response.....	30
Subsection reference: 8.6 Data Packet (DP).....	30
Chapter 10 Test Assertions: Hub, Host Downstream Port, and Device Upstream Port Specification ...	30
Subsection reference: 10.2 Hub Power Management	30
Subsection reference: 10.2.2 Hub Downstream Port U1/U2 Timers	31
Subsection reference: 10.3: Hub Downstream Facing Ports	31
Subsection reference: 10.3.1: Hub Downstream Facing Port State Descriptions	31
Subsection reference: 10.3.1.6: DSPORT.Resetting	31
Subsection reference: 10.4 Hub Downstream Facing Port Power Management	31
Subsection reference: 10.4.2 Hub Downstream Facing Port State Descriptions	31
Subsection reference: 10.4.2.1 Enabled U0 States	31
XHCI Specification Chapter 5 Test Assertions: Register Interface	31
Subsection reference: xHCI 5.4 Host Controller Operational Registers.....	31
Subsection reference: xHCI 5.4.8 Port Status and Control Register (PORTSC).....	31
4 TIMING DEFINITIONS.....	32
5 TEST DESCRIPTIONS.....	35
5.1 Link Initialization Sequence	35
5.2 Physical Layer.....	36
TD.6.1 Lane Polarity Inversion Test.....	36

TD.6.2	Skip Test.....	36
TD.6.3	Elasticity Buffer Test.....	37
TD.6.4	LFPS Frequency Test.....	37
TD.6.5	Polling.LFPS Duration Test.....	37
5.3	Link Layer.....	38
TD.7.1	Link Bring-up Test.....	38
TD.7.2	Link Commands Framings Robustness Test.....	39
TD.7.3	Link Commands CRC-5 Robustness Test.....	40
TD.7.4	Invalid Link Commands Test.....	40
TD.7.5	Header Packet Framing Robustness Test.....	41
TD.7.6	Data Payload Packet Framing Robustness Test.....	41
TD.7.7	RX Header Packet Retransmission Test.....	42
TD.7.8	TX Header Packet Retransmission Test.....	43
TD.7.9	PENDING_HP_TIMER Deadline Test.....	44
TD.7.10	CREDIT_HP_TIMER Deadline Test.....	44
TD.7.11	PENDING_HP_TIMER Timeout Test.....	45
TD.7.12	CREDIT_HP_TIMER Timeout Test.....	45
TD.7.13	Wrong Header Sequence Test.....	46
TD.7.14	Wrong LGOOD_N Sequence Test.....	46
TD.7.15	Wrong LCRD_X Sequence Test.....	46
TD.7.16	Link Command Missing Test (Upstream Port Only).....	47
TD.7.17	tPortConfiguration Time Timeout Test.....	47
TD.7.18	Low Power initiation for U1 test (Downstream Port Only).....	48
TD.7.19	Low Power initiation for U2 test (Downstream Port Only).....	49
TD.7.20	PM_LC_TIMER Deadline Test (Downstream Port Only).....	50
TD.7.21	PM_LC_TIMER Timeout Test (Downstream Port Only).....	51
TD.7.22	PM_ENTRY_TIMER Timeout Test (Upstream Port Only).....	51
TD.7.23	Accepted Power Management Transaction for U1 Test (Upstream Port Only).....	51
TD.7.24	Accepted Power Management Transaction for U2 Test (Upstream Port Only).....	52
TD.7.25	Accepted Power Management Transaction for U3 Test (Upstream Port Only).....	53
TD.7.26	Transition to U0 from Recovery Test.....	54
TD.7.27	Hot Reset Detection in Polling Test (Upstream Port Only).....	55
TD.7.28	Hot Reset Detection in U0 Test (Upstream Port Only).....	56
TD.7.29	Hot Reset Initiation in U0 Test (Downstream Port Only).....	57
TD.7.30	Recovery on three consecutive failed RX Header Packets Test.....	58
TD.7.31	Hot Reset Failure Test (Downstream Port Only).....	59
TD.7.32	Warm Reset Rx.Detect Timeout Test (Hub Downstream Port Only).....	59
TD.7.33	Exit Compliance Mode Test (Upstream Port Only).....	60
TD.7.34	Exit Compliance Mode Test (Downstream Port Only).....	60
TD.7.35	Exit U3 by Reset Test (Downstream Port Only).....	61
TD.7.36	Exit U3 Test (Host Downstream Port Only).....	62
TD.7.37	Packet Pending Test (Upstream Port Only).....	63

1 Introduction

This document provides the compliance criteria and test descriptions for SuperSpeed USB 3.0 Link Layer implementations. It is relevant for anyone building a SuperSpeed-compatible host, hub or device. The document is divided into two major sections. The first section lists the compliance criteria and the second section lists the test descriptions used to verify a port's conformance to these criteria.

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB 3.0 specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test description(s) where the assertion is tested.

Each test assertion is formatted as follows:

Assertion #	Assertion Description	Test #
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Assertion#: Unique identifier for each spec requirement. The identifier is in the form USB30_SPEC_SECTION_NUMBER#X, where X is a unique integer for a requirement in that section.

Assertion Description: Specific requirement from the specification

Test #: A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

- NT** This item is not explicitly tested in a test description. Items can be labeled NT for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the compliance test.
- X.X** This item is covered by the test described in test description X.X in this specification.
- IOP** This assertion is verified by the USB 3.0 Interoperability Test Suite.
- BC** This assertion is applied as a background check in all test descriptions.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

Host tests are performed with a Windows 7 machine with all the latest Microsoft updates. The Compliance driver is loaded for most of the Host tests. The Compliance Driver is provided with USB30CV from the usb.org website. One of the Host tests requires the vendor driver for the host controller to be loaded.

For questions about this document, please contact ssusbcompliance@usb.org.

2 Terms and Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification. Terms and Abbreviations specified in the USB 3.0 specifications are not duplicated here.

Term/Abbreviation	Definition
Host Controller Test Driver	The USB30CV driver running on the host controller. This driver has a known behavior in order to run a portion of the tests described in this specification (for host downstream port testing only).
Link Validation System	The hardware aimed at running the tests on an Upstream or a Downstream Port Under Test. The Link Validation System will act as the opposite port.
LVS	See Link Validation System.
Port Under Test	The port connected to the Link Validation System on which the tests are run.
PUT	See Port Under Test.
USB30CV	USB 3.0 Command Verifier software, available for download from usb.org . The same software that runs Ch 9 and MSC tests.

3 Test Assertions

Unless otherwise noted, subsection references point to the USB 3.0 specification.

Assertion #	Assertion Description	Test #
Chapter 7 Test Assertions: Link Layer		
Subsection reference: 7.2 Link Management and Flow Control		
Subsection reference: 7.2.1.1 Header Packet Structure		
7.2.1.1#1	All header packets shall be 20 symbols long. This includes LMPs, TPs, ITPs, and DPHs. A header packet consists of three parts: a header packet framing, a packet header, and a Link Control Word.	BC
Subsection reference: 7.2.1.1.1 Header Packet Framing		
7.2.1.1.1#1	A header packet shall always begin with HPSTART ordered set.	BC
Subsection reference: 7.2.1.1.2 Packet Header		
7.2.1.1.2#1	A packet header shall consist of 12 bytes of header information and a 2-byte CRC-16.	BC
7.2.1.1.2#2	The CRC-16 shall be calculated as specified when transmitted.	BC
Subsection reference: 7.2.1.1.3 Link Control Word		
7.2.1.1.3#1	The CRC-5 shall be calculated as specified when transmitted.	BC
Subsection reference: 7.2.1.2.1 Data Packet Payload Framing		
7.2.1.2.1#1	A data payload packet shall always begin with DPPSTART ordered set.	IOP
7.2.1.2.1#2	A data payload packet shall always end with DPPEND ordered set to indicate normal ending.	IOP
7.2.1.2.1#3	A data payload packet shall always end with DPPABORT ordered set to indicate an abnormal ending.	NT
Subsection reference: 7.2.1.2.2 Data Packet Payload		
7.2.1.2.2#1	The DPP section shall consist of 0 to 1024 data bytes followed by the 4-byte CRC-32.	IOP
7.2.1.2.2#2	The CRC-32 shall be calculated as specified when transmitted.	IOP
7.2.1.2.2#3	The CRC-32 for a 0 bytes payload shall be 0x00000000.	NT
7.2.1.2.2#4	A DPP shall immediately follow its corresponding DPH with no spacing in between.	IOP
Subsection reference: 7.2.2.1 Link Command Structure		

Assertion #	Assertion Description	Test #
7.2.2.1#1	A link command shall always begin with LCSTART ordered set.	BC
7.2.2.1#2	A link command shall consist of two identical consecutive Link Command Words.	BC
Subsection reference: 7.2.2.2 Link Command Word Definition		
7.2.2.2#1	A link command word shall be 16 bits long, with the 11-bit link command information protected by a 5-bit CRC-5.	BC
7.2.2.2#2	The CRC-5 shall be computed as specified when transmitted.	BC
7.2.2.2#3	Any transmitted link command shall match one of the link commands presented in table 7-4 of USB 3.0 spec.	BC
Subsection reference: 7.2.2.3 Link Command Placement		
7.2.2.3#1	Link commands shall not be placed inside header packet structures.	BC
7.2.2.3#2	Link commands shall not be placed within the DPP of a DP structure.	NT
7.2.2.3#3	Link commands shall not be placed between the DPH and the DPP.	IOP
7.2.2.3#4	Link commands may be placed before and after a header packet with the exception that they shall not be placed in between a DPH and its DPP.	BC IOP
7.2.2.3#5	Link commands shall not be sent until all scheduled SKP ordered sets have been transmitted.	NT
Subsection reference: 7.2.4 Link Command Usage for Flow Control, Error Recovery, and Power Management		
Subsection reference: 7.2.4.1 Header Packet Flow Control and Error Recovery		
Subsection reference: 7.2.4.1.1 Initialization		
7.2.4.1.1#1	A port shall have enough Tx Header Buffers in its transmitter to hold up to four unacknowledged header packets.	BC
7.2.4.1.1#2	A port shall have enough Rx Header Buffers in its receiver to receive up to four header packets.	
7.2.4.1.1#3	Upon entry to U0, a port shall immediately start the PENDING_HP_TIMER in expectation of the Header Sequence Number and the Rx Header Buffer Credit Advertisement.	7.26
7.2.4.1.1#3.1	Upon entry to U0, a port shall immediately start the CREDIT_HP_TIMER in expectation of the Header Sequence Number and the Rx Header Butter Credit Advertisement	NT
7.2.4.1.1#4	Upon entry to U0, after starting the PENDING_HP_TIMER and CREDIT_HP_TIMER timers, a port shall initiate the Header Sequence Number Advertisement.	7.26 BC
7.2.4.1.1#5	Upon entry to U0, after the Header Sequence Number Advertisement, a port shall initiate the Rx Header Buffer Credit Advertisement.	4.1 7.26
7.2.4.1.1#6	A port shall set its initial Rx Header Sequence Number to 0	4.1

Assertion #	Assertion Description	Test #
	when it enters U0 from Polling or Hot Reset.	7.27 - 29
7.2.4.1.1#7	A port shall set its initial Rx Header Sequence Number to the Header Sequence Number of the next expected header packet when a it enters U0 from Recovery.	4.1 7.30
7.2.4.1.1#8	A port shall set its initial Tx Header Sequence Number to 0 when it enters U0 from Polling or Hot Reset.	4.1 7.27 – 7.29
7.2.4.1.1#9	A port shall set its initial Tx Header Sequence Number to the same as the Tx Header Sequence Number before Recovery when it enters U0 from Recovery.	7.26 7.30
7.2.4.1.1#10	A port shall initiate the Header Sequence Number Advertisement by transmitting LGOOD_n with “n” equal to the Rx Header Sequence Number minus one.	4.1
7.2.4.1.1#11	A port shall set its initial ACK Tx Header Sequence Number to the Sequence Number received during the Rx Header Sequence Number Advertisement plus one.	4.1
7.2.4.1.1#12	A port shall not send any header packets until the Header Sequence Number Advertisement has been received and a Remote Rx Header Buffer Credit is available.	4.1
7.2.4.1.1#13	A port shall initialize its Tx Header Buffer Credit index to A before sending the Rx Header Buffer Credit.	4.1
7.2.4.1.1#14	A port shall initialize its Rx Header Buffer Credit index to A before sending the Rx Header Buffer Credit.	4.1
7.2.4.1.1#15	A port shall initialize its Remote Rx Header Buffer Credit Count to 0 before sending the Rx Header Buffer Credit.	4.1
7.2.4.1.1#16	A port shall continue to process header packets in its Rx Header Buffers before sending the Rx Header Buffer Credit.	4.1
7.2.4.1.1#17	When a port enters U0 from Polling or Hot Reset, a port shall set its Local Rx Header Buffer Credit Count to 4.	4.1 7.27 - 29
7.2.4.1.1#18	When a port enters U0 from Recovery, a port shall set its Local Rx Header Buffer Credit Count to the number of Rx Header Buffers available for incoming header packets.	NT
7.2.4.1.1#19	A port shall transmit LCRD_A when the Local Rx Header Buffer Credit Count is one based on its Local Rx Header Buffer Credit Count.	NT
7.2.4.1.1#20	A port shall transmit LCRD_A and LCRD_B when the Local Rx Header Buffer Credit Count is two.	NT
7.2.4.1.1#21	A port shall transmit LCRD_A, LCRD_B and LCRD_C when the Local Rx Header Buffer Credit Count is three.	NT
7.2.4.1.1#22	A port shall transmit LCRD_A, LCRD_B, LCRD_C, LCRD_D, when the Local Rx Header Buffer Credit Count is four.	4.1 7.27 - 29
7.2.4.1.1#23	A port receiving LCRD_x shall increment its Remote Rx Header Buffer Credit Count by one each time an LCRD_x is received up to four.	NT
7.2.4.1.1#24	A port shall not transmit any header packet when its Remote Rx Header Buffer Credit Count is zero.	NT
7.2.4.1.1#25	A port sending LBAD before Recovery shall not expect to	NT

Assertion #	Assertion Description	Test #
	receive LRTY before a retried header packet from its link partner upon entry to U0, when a port enters U0 from Recovery.	
7.2.4.1.1#26	A port receiving LBAD before Recovery shall not send LRTY before a retried header packet to its link partner upon entry to U0, when a port enters U0 from Recovery.	NT
Subsection reference: 7.2.4.1.2 General Rules of LGOOD_n and LCRD_x Usage		
7.2.4.1.2#1	A hub shall set the DL bit in the Link Control Word when a header packet transmission is delayed.	NT
Subsection reference: 7.2.4.1.3 Transmitting Header Packets		
7.2.4.1.3#1	Upon receiving LBAD, a port shall send LRTY followed by resending all header packets that have not been acknowledged with LGOOD_n, except for Recovery.	7.8
7.2.4.1.3#2	Prior to resending a header packet, a port shall set the Delay bit within the Link Control word and re-calculate the CRC-5.	7.8
Subsection reference: 7.2.4.1.4 Receiving Header Packets		
7.2.4.1.4#1	A port shall detect a header packet when receiving an HPSTART framing with at least three valid symbols out of four, and ignore the packet otherwise.	BC 7.5
7.2.4.1.4#2	A port receiving a header packet shall send a LGOOD_n when a valid HPSTART is detected, the CRC-5 is valid, the CRC-16 is valid, no K-symbol occurrence is detected and no 8b/10b error is detected.	BC
7.2.4.1.4#3	A port receiving a header packet shall send an LBAD when a valid HPSTART is detected and either CRC-5 or CRC-16 checks fail.	7.7
7.2.4.1.4#4	A port receiving a header packet shall send an LBAD when a valid HPSTART is detected and any K-symbol occurrence is detected or any 8b/10b error is detected.	7,7
7.2.4.1.4#5	A port shall transition directly to Recovery if it fails to receive a header packet three consecutive times. A port shall not issue the third LBAD upon the third error.	7.30
Subsection reference: 7.2.4.1.6 Receiving Data Packet Payload		
7.2.4.1.6#1	A port shall detect a DPP packet when receiving a DPPSTART framing with at least three valid symbols out of four, and ignore the packet otherwise.	7.6
7.2.4.1.6#2	A port shall accept a DPP when a valid DPPSTART is detected, a valid DPPEND is detected, there are four to 1028 symbols, the CRC-32 is valid, no K-symbol occurrence is detected, no 8b/10b error is detected and it is received immediately after its DPH.	7.6
7.2.4.1.6#3	A port shall ignore a DPP when valid DPPSTART and DPPEND are detected and the CRC-32 check fails, there are less than four symbols, there are more than 1028 symbols, any K-symbol occurrence is detected, any 8b/10b error is detected or it is not preceded immediately by its DPH.	NT
7.2.4.1.6#4	The DPP shall be aborted when a valid DPPABORT ordered set is detected	NT

Assertion #	Assertion Description	Test #
Subsection reference: 7.2.4.1.10 Transmitting Timers		
7.2.4.1.10#1	A port transmitting a header packet shall transition to Recovery upon its PENDING_HP_TIMER timeout.	7.11
7.2.4.1.10#2	The PENDING_HP_TIMER shall be reset and restarted when a header packet is acknowledged with LGOOD_n.	7.9
7.2.4.1.10#3	The PENDING_HP_TIMER shall be reset and stopped when a Header Sequence Number Advertisement is received.	BC
7.2.4.1.10#4	The PENDING_HP_TIMER shall be reset and stopped when a header packet acknowledgement of LGOOD_n is received and all transmitted header packets in the Tx Header Buffers are acknowledged.	BC
7.2.4.1.10#5	The PENDING_HP_TIMER shall be reset and stopped when a header packet acknowledgement of LBAD is received.	7.30
7.2.4.1.10#6	A port transmitting a header packet shall transition to Recovery upon its CREDIT_HP_TIMER timeout.	7.12
7.2.4.1.10#7	The CREDIT_HP_TIMER shall be reset when a valid LCRD_x is received.	7.10
7.2.4.1.10#8	The CREDIT_HP_TIMER shall be restarted when a valid LCRD_x is received and the Remote Rx Header Buffer Credit Count is less than four.	NT
Subsection reference: 7.2.4.2.1 Power Management Link Timers		
7.2.4.2.1#1	A port shall start the PM_LC_TIMER after the last symbol of the LGO_Ux link command is sent.	7.21
7.2.4.2.1#2	A port shall disable and reset the PM_LC_TIMER upon receipt of the LAU or LXU.	7.20
7.2.4.2.1#3	A port shall start the PM_ENTRY_TIMER after the last symbol of the LAU is sent.	7.22
7.2.4.2.1#4	A port shall disable and reset the PM_ENTRY_TIMER upon receipt of an LPMA or a TS1 ordered set.	7.23-25
7.2.4.2.1#5	A port shall start the Ux_EXIT_TIMER when it starts to send the LFPS Exit handshake signal.	NT
7.2.4.2.1#6	A port shall disable and reset the Ux_EXIT_TIMER upon entry to U0.	6.6-7
Subsection reference: 7.2.4.2.2 Low Power Link State Initiation		
7.2.4.2.2#1	A port shall not send an LGO_U1, LGO_U2 or LGO_U3 unless it meets all of the following: <ul style="list-style-type: none"> ▪ It has transmitted LGOOD_n and LCRD_x for all header packets received. ▪ It has received LGOOD_n and LCRD_x for all header packets transmitted. ▪ It has no pending packets for transmission. ▪ It has completed the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement upon entry to U0. ▪ It is directed by a higher layer to initiate entry. ▪ It has met higher layer conditions for initiating entry. 	7.18-19
7.2.4.2.2#2	An upstream port shall send an LAU in response to an LGO_U1	7.23-24

Assertion #	Assertion Description	Test #
	or LGO_U2, when the Force Link PM Accept field is asserted due to having received a Set Link Functionality LMP.	
7.2.4.2.2#3	A port shall send an LAU in response to an LGO_U1 or LGO_U2, when all of the following conditions are met: <ul style="list-style-type: none"> ▪ It has transmitted an LGOOD_n, LCRD_x sequence for all packets received. ▪ It has received an LGOOD_n, LCRD_x sequence for all packets transmitted. ▪ It has no pending packets for transmission. ▪ It is not directed by a higher layer to reject entry. 	7.23-24
7.2.4.2.2#4	A port shall send an LXU, when any of the above conditions are not met.	NT
7.2.4.2.2#5	A port shall send an LXU in response to an LGO_U1 or LGO_U2, when it has not yet transmitted an LGOOD_n, LCRD_x sequence for all packets received.	NT
7.2.4.2.2#6	A port shall send an LXU in response to an LGO_U1 or LGO_U2, when it has not received an LGOOD_n, LCRD_x sequence for all packets transmitted.	NT
7.2.4.2.2#7	A port shall send an LXU in response to an LGO_U1 or LGO_U2, when it has pending packets for transmission.	NT
7.2.4.2.2#8	A port shall send an LXU in response to an LGO_U1 or LGO_U2, when it is directed by a higher layer to reject entry.	NT
Subsection reference: 7.2.4.2.3 U1/U2 Entry Flow		
7.2.4.2.3#1	A port shall send a signal LGO_U1 or LGO_U2 to request a transition to a low power link state.	7.18-19
7.2.4.2.3#2	A port shall either accept LGO_Ux with a single LAU or shall reject LGO_U1 or LGO_U2 with a single LXU and remain in U0.	7.23-24
7.2.4.2.3#3	Upon sending LGO_U1 or LGO_U2, a port shall not send any packets until it has received LXU or re-entered U0.	7.18-19
7.2.4.2.3#4	Upon sending LGO_U1 or LGO_U2, a port shall continue receiving and processing packets and link commands.	7.18-19
7.2.4.2.3#5	Upon receiving LXU, a port shall remain in U0.	NT
7.2.4.2.3#6	A port shall initiate transition to Recovery when a single LAU or LXU is not received upon PM_LC_TIMER timeout.	7.21
7.2.4.2.3#7	Upon receiving LAU, a port shall send a single LMPA and then the requested low power link state.	7.18-19
7.2.4.2.3#8	Upon issuing LAU, or LPMA, a port shall not send any packets or link commands.	7.18-19 7.22 7.23-24
7.2.4.2.3#9	A port that sends LAU shall enter the corresponding low power link state upon receipt of LPMA before PM_ENTRY_TIMER timeout.	7.23-24
7.2.4.2.3#10	A port that sends LAU shall enter the low power link state upon PM_ENTRY_TIMER timeout and all of the following conditions are met: <ul style="list-style-type: none"> ▪ LPMA is not received. ▪ No TS1 ordered set is received. 	7.22

Assertion #	Assertion Description	Test #
7.2.4.2.3#11	A port that sent LAU shall enter Recovery before PM_ENTRY_TIMER timeout when a TS1 ordered set is received.	NT
7.2.4.2.3#12	A port that has sent LAU shall not respond with Ux_LFPS exit handshake before PM_ENTRY_TIMER timeout.	7.22
7.2.4.2.3#13	A port in U1 shall enter U2 directly when the following two conditions are met: <ul style="list-style-type: none"> ▪ The port's U2 inactivity timer is enabled. ▪ The U2 inactivity timer times out and no U1 LFPS exit signal is received. 	NT
Subsection reference: 7.2.4.2.4 U3 Entry Flow		
7.2.4.2.4#1	When directed, a downstream port shall initiate U3 entry process by sending LGO_U3.	7.35 7.36
7.2.4.2.4#2	An upstream port shall send LAU in response to LGO_U3.	7.25
7.2.4.2.4#3	An upstream port shall not send any packets or link commands subsequent to sending an LAU.	7.25
7.2.4.2.4#4	Upon issuing LGO_U3, a downstream port shall ignore any packets sent by an upstream port.	7.35 7.36
7.2.4.2.4#5	A downstream port shall send a single LPMA and then transition to U3 when LAU is received.	7.35 7.36
7.2.4.2.4#6	A downstream port shall transition to Recovery and reinitiate U3 entry after re-entry to U0 when all of the following three conditions are met: <ul style="list-style-type: none"> ▪ PM_LC_TIMER timeout ▪ LAU is not received. ▪ The number of consecutive U3 entry attempts is less than three. 	NT
7.2.4.2.4#7	An upstream port shall transition to U3 when LPMA is received.	7.25
7.2.4.2.4#8	An upstream port shall transition to U3 when PM_ENTRY_TIMER times out and LPMA is not received.	NT
7.2.4.2.4#9	A downstream port shall transition to SS.Inactive when it fails U3 entry on three consecutive attempts.	NT
Subsection reference: 7.2.4.2.5 Concurrent Low Power Link Management Flow		
7.2.4.2.5#1	When a downstream port has sent an LGO_U1, LGO_U2, LGO_U3 and also received an LGO_U1 or LGO_U2, it shall send an LXU.	NT
7.2.4.2.5#2	When an upstream port has sent an LGO_U1 or LGO_U2 and also received an LGO_U1, LGO_U2, it shall wait until receipt of an LXU and then send either an LAU or LXU.	NT
7.2.4.2.5#3	When an upstream port has sent an LGO_U1 or LGO_U2 and also received an LGO_U3, it shall wait until receipt of an LXU and then send an LAU.	NT
7.2.4.2.5#4	When a downstream port is directed by a higher layer to initiate a transition to U3, and a transition to U1 or U2 has been initiated but not yet completed, the port shall first complete the in-process transition to U1 or U2, then return to U0 and request entry to U3.	NT

Assertion #	Assertion Description	Test #
Subsection reference: 7.2.4.2.6 Concurrent Low Power Link Management and Recovery Flow		
7.2.4.2.6#1	Upon issuing LGO_Ux, the port shall transition to Recovery when a TS1 ordered set is received.	NT
Subsection reference: 7.2.4.2.7 Low Power Link State Exit Flow		
7.2.4.2.7#1	When a port is initiating U3 wakeup, it shall start sending U3 LFPS wakeup handshake signal.	7.36
7.2.4.2.7#2	A port upon receiving U1/U2 EXIT or U3 wakeup LFPS handshake signal shall start U1/U2 exit or U3 wakeup by responding with U1/U2 Exit or U3 wakeup LFPS signal.	7.18-19 7.23-25
7.2.4.2.7#3	Upon a successful LFPS handshake before tNoLFPSResponse Timeout, a port shall transition to Recovery.	7.18-19 7.23-25
7.2.4.2.7#4	A port initiating U1 or U2 Exit shall transition to SS.Inactive upon tNoLFPSResponse timeout and the condition of a successful LFPS handshake is not met.	NT
7.2.4.2.7#5	A port initiating U1 or U2 Exit shall not transition to U0 upon Ux_EXIT_TIMER timeout.	NT
7.2.4.2.7#6	A port initiating U3 wakeup shall remain in U3 when the condition of a successful LFPS handshake is not met upon tNoLFPSResponse Timeout.	NT
Subsection reference: 7.3 Link Error Rules/Recovery		
Subsection reference: 7.3.4 Link Commands Errors		
7.3.4#1	A port shall detect a link command when receiving a LCSTART framing with at least three valid symbols out of four, and ignore the link command otherwise.	7.2
7.3.4#2	A valid link command is declared if both link command words are the same, they both contain valid link command information as defined in Table 7-4 and they both pass CRC-5 check.	4.1 7.2 7.3 7.4
7.3.4#4	A port shall transition to Recovery upon detection of an LGOOD_n ordering error.	7.14
7.3.4#5	A port shall transition to Recovery upon detection of an LCRD_x ordering error.	7.15
7.3.4#6	A port shall transition to Recovery upon its PM_LC_TIMER timeout.	7.21
7.3.4#7	A downstream port shall transition to Recovery upon detection of a missing LUP.	7.16
7.3.4#8	An upstream port shall transition to Recovery upon detection of a missing LDN	7.16
Subsection reference: 7.3.5 ACK Tx Header Sequence Number Errors		
7.3.5#1	An ACK Tx Header Sequence Number error shall be declared when the Header Sequence Number in the received LGOOD_n does not match the ACK Tx Header Sequence Number.	7.13

Assertion #	Assertion Description	Test #
Subsection reference: 7.3.6 Header Sequence Number Advertisement Errors		
7.3.6#1	A port shall transition to Recovery upon its PENDING_HP_TIMER timeout before the Header Sequence Number Advertisement is received.	7.26
7.3.6#2	A port shall transition to Recovery when a header packet is received before sending the Header Sequence Number Advertisement.	NT
7.3.6#3	A port shall transition to Recovery when an LCRD_x or LGO_Ux is received before receiving the Header Sequence Number Advertisement.	NT
Subsection reference: 7.3.7 Rx Header Buffer Credit Advertisement Errors		
7.3.7#1	A port shall transition to Recovery upon its CREDIT_HP_TIMER timeout before the Header Buffer Credit Advertisement is received.	NT
7.3.7#2	A port shall transition to Recovery when a header packet is received before sending the Header Buffer Credit Advertisement.	NT
7.3.7#3	A port shall transition to Recovery when a LGO_Ux is received before receiving the Header Buffer Credit Advertisement.	NT
Subsection reference: 7.3.8 Training Sequence Error		
7.3.8#1	A downstream port shall transition to Rx.Detect when a Training Sequence error occurs during Polling.	NT
7.3.8#2	An upstream port of a hub shall transition to Rx.Detect when a Training Sequence error occurs during Polling.	NT
7.3.8#3	An upstream port of a peripheral device shall transition to SS.Disabled when a Training Sequence error occurs during Polling.	NT
7.3.8#4	A downstream port shall transition to SS.Inactive when a Training Sequence error occurs during Recovery and the transition to Recovery is not an attempt for Hot Reset.	NT
7.3.8#5	A downstream port shall transition to Rx.Detect when a Training Sequence error occurs during Recovery.Active and Recovery.Configuration and the transition to Recovery is not an attempt for Hot Reset.	NT
7.3.8#6	An upstream port shall transition to SS.Inactive when a Training Sequence error occurs during Recovery.	NT
Subsection reference: 7.4 PowerOn Reset and Inband Reset		
Subsection reference: 7.4.1 Power On Reset		
7.4.1#1	Receiver termination shall meet the $Z_{RX-HIGH-IMP-DC-POS}$ when PowerOn Reset is asserted or while VBUS is OFF.	NT
7.4.1#2	Transmitters shall hold a constant DC common mode voltage ($V_{TX-DC-CM}$) when PowerOnReset is asserted or while VBUS is OFF.	NT
7.4.1#3	The LTSSM of a port shall be initialized to Rx.Detect, when PowerOnReset is completed and VBUS is valid.	NT
7.4.1#4	The LTSSM and the PHY level variables shall be reset to their default values, when PowerOnReset is completed and VBUS is	NT

Assertion #	Assertion Description	Test #
	valid	
7.4.1#5	The receiver termination of a port shall meet R _{RX-DC} , when PowerOnReset is completed and VBUS is valid.	NT
Subsection reference: 7.4.2 Inband Reset		
7.4.2#1	Upon completion of Hot Reset, a downstream port shall reset its Link Error Count.	NT
7.4.2#2	Upon completion of Hot Reset, the port configuration information of an upstream port shall remain unchanged.	7.28 7.29
7.4.2#3	Upon completion of Hot Reset, the PHY level variables shall remain unchanged.	NT
7.4.2#4	Upon completion of Hot Reset, the LTSSM of a port shall transition to U0.	7.27-29
7.4.2#5	Upon a completion of a Warm Reset, a downstream port shall reset its Link Error Count.	NT
7.4.2#6	Upon a completion of a Warm Reset, Port Configuration information of an upstream port shall be reset to default values.	7.31
7.4.2#7	Upon a completion of a Warm Reset, the PHY level variables shall be reinitialized or retrained.	NT
7.4.2#8	Upon a completion of a Warm Reset, the LTSSM of a port shall transition to U0.	7.31
7.4.2#9	When a PORT_RESET is directed, when the downstream port is in U3, or Loopback, or Compliance Mode, or SS.Inactive, it shall use Warm Reset.	7.34
7.4.2#10	When a PORT_RESET is directed, when the downstream port is in U0, it shall use Hot Reset.	7.29
7.4.2#11	When a PORT_RESET is directed, when the downstream port is in U1 or U2, it shall exit U1 or U2 using the LFPS exit handshake, transition to Recovery and then transition to Hot Reset.	NT
7.4.2#12	When a PORT_RESET is directed, when a downstream port is in a transitory state of Polling or Recovery, it shall use Hot Reset.	NT
7.4.2#13	When a PORT_RESET is directed, when a Hot Reset fails due to a LFPS handshake timeout, a downstream port shall transition to SS.Inactive.	NT
7.4.2#14	When a PORT_RESET is directed, when a Hot Reset fails due to a TS1/TS2 handshake timeout, a downstream port shall transition to Rx.Detect and attempt a Warm Reset.	7.31
7.4.2#15	When a PORT_RESET is directed, when the downstream port is in SS.Disabled, an Inband Reset is prohibited.	NT
7.4.2#16	When BH_PORT_RESET is directed, a downstream port shall initiate a Warm Reset in all the link states except SS.Disabled and transition to Rx.Detect.	NT
7.4.2#17	When BH_PORT_RESET is directed, an upstream port shall enable its LFPS receiver and Warm Reset detector in all the link states except SS.Disabled.	NT
7.4.2#18	When BH_PORT_RESET is directed, an upstream port receiving Warm Reset shall transition to Rx.Detect.	NT

Assertion #	Assertion Description	Test #
Subsection reference: 7.5 Link Training and Status State Machine (LTSSM)		
Subsection reference: 7.5.1 SS.Disabled		
7.5.1#1	A downstream port shall transition to SS.Disabled from any other state when directed.	NT
7.5.1#2	An upstream port shall transition to SS.Disabled when VBUS is not valid.	NT
Subsection reference: 7.5.1.1 SS.Disabled Requirements		
7.5.1.1#1	The port's receiver termination shall present high impedance to ground of $Z_{RX-HIGH-IMP-DC-POS}$ when in SS.Disabled.	NT
7.5.1.1#2	The port shall be disabled from transmitting and receiving LFPS and SuperSpeed signals when in SS.Disabled.	NT
Subsection reference: 7.5.1.2 Exit from SS.Disabled		
7.5.1.2#1	A downstream port shall transition to Rx.Detect when directed.	NT
7.5.1.2#2	An upstream port shall transition to Rx.Detect only when VBUS transition to valid or a USB2.0 bus reset is detected.	NT
Subsection reference: 7.5.2 SS.Inactive		
Subsection reference: 7.5.2.3 SS.Inactive.Quiet		
Subsection reference: 7.5.2.3.1 SS.Inactive.Quiet Requirement		
7.5.2.3.1#1	The function of the far-end receiver termination detection shall be disabled.	NT
Subsection reference: 7.5.2.3.2 Exit from SS.Inactive.Quiet		
7.5.2.3.2#1	The port shall transition to SS.Inactive.Disconnect.Detect upon the 12-ms timer timeout.	NT
7.5.2.3.2#2	A downstream port shall transition to Rx.Detect when Warm Reset is issued.	NT
7.5.2.3.2#3	An upstream port shall transition to Rx.Detect upon detection of Warm Reset.	NT
Subsection reference: 7.5.2.4 SS.Inactive.Disconnect.Detect		
Subsection reference: 7.5.2.4.1 SS.Inactive.Disconnect.Detect Requirements		
7.5.2.4.1#1	The transmitter shall perform the far-end receiver termination detection when in SS.Inactive.Disconnect.Detect.	NT
Subsection reference: 7.5.2.4.2 Exit from SS.Inactive.Disconnect.Detect		
7.5.2.4.2#1	The port shall transition to Rx.Detect when a far-end low-impedance receiver termination (R_{RX-DC}) is not detected.	NT
7.5.2.4.2#2	The port shall transition to SS.Inactive.Quiet when a far-end low-impedance receiver termination (R_{RX-DC}) is detected.	NT
Subsection reference: 7.5.3 Rx.Detect		

Assertion #	Assertion Description	Test #
Subsection reference: 7.5.3.3 Rx.Detect.Reset		
Subsection reference: 7.5.3.3.1 Rx.Detect.Reset Requirements		
7.5.3.3.1#1	A downstream port shall transmit Warm Reset for the duration of tReset.	7.31
7.5.3.3.1#2	An upstream port shall remain in this state until it detects the completion of Warm Reset.	NT
Subsection reference: 7.5.3.3.2 Exit from Rx.Detect.Reset		
7.5.3.3.2#1	The port shall transition directly to Rx.Detect.Active when the entry to Rx.Detect is not due to a Warm Reset.	NT
7.5.3.3.2#2	A downstream port shall transition to Rx.Detect.Active after it transmits Warm Reset for the duration of tReset.	NT
7.5.3.3.2#3	An upstream port shall transition to Rx.Detect.Active when it receives no more LFPS Warm Reset signaling.	NT
Subsection reference: 7.5.3.4 Rx.Detect.Active		
Subsection reference: 7.5.3.5 Rx.Detect.Active Requirement		
7.5.3.5#1	The transmitter shall initiate a far-end receiver termination detection when in Rx.Detect.Active.	NT
7.5.3.5#2	The number of far-end receiver termination detection events shall be counted by an upstream port when in Rx.Detect.Active.	NT
Subsection reference: 7.5.3.6 Exit from Rx.Detect.Active		
7.5.3.6#1	The port shall transition from Rx.Detect.Active to Polling upon detection of a far-end low-impedance receiver termination (R_{RX-DC}).	NT
7.5.3.6#2	A downstream port shall transition from Rx.Detect.Active to Rx.Detect.Quiet when a far-end low-impedance receiver termination (R_{RX-DC}) is not detected.	NT
7.5.3.6#3	An upstream port of a hub shall transition from Rx.Detect.Active to Rx.Detect.Quiet when a far-end low-impedance receiver termination (R_{RX-DC}) is not detected.	NT
7.5.3.6#4	An upstream port of a peripheral device shall transition from Rx.Detect.Active to Rx.Detect.Quiet when the following two conditions are met: <ul style="list-style-type: none"> ▪ A far-end low-impedance receiver termination (R_{RX-DC}) is not detected. ▪ The number of far-end receiver termination detection events is less than eight. 	NT
7.5.3.6#5	An upstream port of a peripheral device shall transition from Rx.Detect.Active to SS.Disabled when the following two conditions are met: <ul style="list-style-type: none"> ▪ A far-end low-impedance receiver termination (R_{RX-DC}) is not detected. ▪ The number of far-end receiver termination (R_{RX-DC}) detection events has reached eight. 	NT
Subsection reference: 7.5.3.7 Rx.Detect.Quiet		

Assertion #	Assertion Description	Test #
Subsection reference: 7.5.3.7.1 Rx.Detect.Quiet Requirements		
7.5.3.7.1#1	The far-end receiver termination detection shall be disabled when in Rx.Detect.Quiet.	NT
Subsection reference: 7.5.3.7.2 Exit from Rx.Detect.Quiet		
7.5.3.7.2#1	The port shall transition from Rx.Detect.Quiet to Rx.Detect.Active upon the 12-ms timer timeout.	NT
Subsection reference: 7.5.4 Polling		
Subsection reference: 7.5.4.3 Polling.LFPS		
Subsection reference: 7.5.4.3.1 Polling.LFPS Requirements		
7.5.4.3.1#1	Upon entry to Polling.LFPS, an LFPS receiver shall be enabled.	BC
7.5.4.3.1#2	Upon entry to Polling.LFPS, a port shall establish its LFPS operating condition within 80 μ s.	NT
Subsection reference: 7.5.4.3.2 Exit from Polling.LFPS		
7.5.4.3.2#1	The port shall transition from Polling.LFPS to Polling.RxEQ when the following three conditions are met: <ul style="list-style-type: none"> ▪ At least 16 consecutive Polling.LFPS bursts are sent. ▪ Two consecutive Polling.LFPS bursts are received. ▪ Four consecutive Polling.LFPS bursts are sent after receiving one Polling.LFPS burst. 	BC
7.5.4.3.2#2	The port shall transition to from Polling.LFPS to Compliance Mode upon 360-ms timer timeout if the following two conditions are met: <ul style="list-style-type: none"> ▪ The port has never successfully completed Polling.LFPS after PowerOn Reset. ▪ The condition to transition to Polling.RxEQ is not met. 	7.33 7.34
7.5.4.3.2#3	A downstream port shall transition from Polling.LFPS to Rx.Detect upon the 360-ms timer timeout after having trained once since PowerOn Reset and the conditions to transition to Polling.RxEQ are not met.	NT
7.5.4.3.2#4	An upstream port of a hub shall transition from Polling.LFPS to Rx.Detect upon the 360-ms timer timeout after having trained once since PowerOn Reset if the conditions to transition to Polling.RxEQ are not met.	NT
7.5.4.3.2#5	A peripheral device shall transition from Polling.LFPS to SS.Disabled upon the 360-ms timeout after having trained once since PowerOn Reset if the conditions to transition to Polling.ExEQ are not met.	NT
7.5.4.3.2#6	A downstream port shall transition from Polling.LFPS to Rx.Detect when directed to issue Warm Reset.	NT
7.5.4.3.2#7	An upstream port shall transition from Polling.LFPS to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.4.4 Polling.RxEQ		
Subsection reference: 7.5.4.4.1 Polling.RxEQ Requirements		

Assertion #	Assertion Description	Test #
7.5.4.4.1#1	The detection and correction of the lane polarity inversion shall be enabled in Polling.RxEQ.	6.1
7.5.4.4.1#2	The port shall transmit the TSEQ ordered sets in Polling.RxEQ.	BC
7.5.4.4.1#3	The port shall complete receiver equalizer training upon exit from Polling.RxEQ .	BC
Subsection reference: 7.5.4.4.2 Exit from Polling.RxEQ		
7.5.4.4.2#1	The port shall transition from Polling.RxEQ to Polling.Active after 65,536 consecutive TSEQ ordered sets are transmitted.	BC
7.5.4.4.2#2	A downstream port shall transition from Polling.RxEQ to Rx.Detect when directed to issue Warm Reset.	NT
7.5.4.4.2#3	An upstream port shall transition from Polling.RxEQ to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.4.5 Polling.Active		
Subsection reference: 7.5.4.5.1 Polling.Active Requirements		
7.5.4.5.1#1	The port shall transmit TS1 ordered sets in Polling.Active.	BC
7.5.4.5.1#2	The receiver is training using TS1 or TS2 ordered sets in Polling.Active.	BC
Subsection reference: 7.5.4.5.2 Exit from Polling.Active		
7.5.4.5.2#1	The port shall transition from Polling.Active to Polling.Configuration upon receiving eight consecutive and identical TS1 or TS2 ordered sets.	BC
7.5.4.5.2#2	A downstream port shall transition from Polling.Active to Rx.Detect upon the 12-ms timer timeout if the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.5.2#3	An upstream port of a hub shall transition from Polling.Active to Rx.Detect upon the 12-ms timer timeout if the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.5.2#4	An upstream port of a peripheral device shall transition from Polling.Active to SS.Disabled upon the 12-ms timer timeout if the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.5.2#5	A downstream port shall transition to from Polling.Active to Rx.Detect when directed to issue Warm Reset.	NT
7.5.4.5.2#6	An upstream port shall transition to from Polling.Active to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.4.6 Polling.Configuration		
Subsection reference: 7.5.4.6.1 Polling.Configuration Requirements		
7.5.4.6.1#1	The downstream port shall transmit identical TS2 ordered sets upon entry to Polling.Configuration and set the Reset bit, when directed.	BC 7.29
7.5.4.6.1#2	A port that has Loopback Master capability and has been directed to enter Loopback shall transmit identical TS2 ordered sets with the Loopback bit set upon entry to Polling.Configuration.	NT

Assertion #	Assertion Description	Test #
7.5.4.6.1#3	A port that has Disabling Scrambling capability and has been directed to disable scrambling shall transmit identical TS2 ordered sets with the Disabling Scrambling bit set upon entry to Polling.Configuration.	NT
Subsection reference: 7.5.4.6.2 Exit from Polling.Configuration		
7.5.4.6.2#1	The port shall transition from Polling.Configuration to Polling.Idle when the following two conditions are met: <ul style="list-style-type: none"> ▪ Eight consecutive and identical TS2 ordered sets are received. ▪ Sixteen TS2 ordered sets are sent after receiving the first of the eight consecutive and identical TS2 ordered sets. 	BC
7.5.4.6.2#2	A downstream port shall transition from Polling.Configuration to Rx.Detect upon the 12-ms timer timeout if the conditions to transition to Polling.Idle are not met.	NT
7.5.4.6.2#3	An upstream port of a hub shall transition from Polling.Configuration to Rx.Detect upon the 12-ms timer timeout if the conditions to transitions to Polling.Idle are not met.	NT
7.5.4.6.2#4	An upstream port of a peripheral device shall transition from Polling.Configuration to SS.Disabled upon the 12-ms timer timeout if the conditions to transition to Polling.Idle are not met.	NT
7.5.4.6.2#5	A downstream port shall transition from Polling.Configuration to Rx.Detect when directed to issue Warm Reset.	NT
7.5.4.6.2#6	An upstream port shall transition from Polling.Configuration to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.4.7 Polling.Idle		
Subsection reference: 7.5.4.7.1 Polling.Idle Requirements		
7.5.4.7.1#1	A downstream port shall reset its Link Error Count when it enters Polling.Idle.	NT
7.5.4.7.1#2	An upstream port shall reset its port configuration information to default values when it enters Polling.Idle.	NT
7.5.4.7.1#3	In Polling.Idle the port shall enable scrambling if the Disabling Scrambling bit is not asserted in the TS2 ordered set received in Polling.Configuration.	NT
7.5.4.7.1#4	In Polling.Idle the port shall disable the scrambling when directed, or when the Disabling Scrambling bit is asserted in the TS2 ordered set received in Polling.Configuration.	NT
7.5.4.7.1#5	The port shall transmit Idle Symbols in Polling.Idle.	NT
7.5.4.7.1#6	The port shall be able to receive the Header Sequence Number Advertisement from its link partner in Polling.Idle.	NT
Subsection reference: 7.5.4.7.2 Exit form Polling.Idle		
7.5.4.7.2#1	A port having Loopback Master capability shall transition to Loopback when directed.	NT
7.5.4.7.2#2	A port shall transition to Loopback as a loopback slave when the Loopback bit is asserted in the TS2 ordered set received in Polling.Configuration.	NT

Assertion #	Assertion Description	Test #
7.5.4.7.2#3	A downstream port shall transition to Hot Reset when directed.	7.29
7.5.4.7.2#4	An upstream port shall transition to Hot Reset when the Reset bit is asserted in the TS2 ordered set received in Polling.Configuration.	7.27
7.5.4.7.2#5	The port shall transition from Polling.Idle to U0 when the following two conditions are met: <ul style="list-style-type: none"> ▪ Eight consecutive Idle Symbols are received. ▪ Sixteen Idle Symbols are sent after receiving one Idle Symbol. 	NT
7.5.4.7.2#6	A downstream port shall transition from Polling.Idle to Rx.Detect upon the 2-ms timer timeout if the conditions to transition to U0 are not met.	NT
7.5.4.7.2#7	An upstream port of a hub shall transition from Polling.Idle to Rx.Detect upon the 2-ms timer timeout if the conditions to transition to U0 are not met.	NT
7.5.4.7.2#8	An upstream port of a peripheral device shall transition from Polling.Idle to SS.Disabled upon the 2-ms timer timeout if the conditions to transition to U0 are not met.	NT
7.5.4.7.2#9	A downstream port shall transition from Polling.Idle to Rx.Detect when Reset is directed.	NT
7.5.4.7.2#10	An upstream port shall transition from Polling.Idle to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.5 Compliance Mode		
Subsection reference: 7.5.5.1 Compliance Mode Requirements		
7.5.5.1#1	The port shall maintain the low-impedance receiver termination (R _{RX-DC}) when it is in Compliance Mode.	NT
7.5.5.1#2	The port shall transmit the compliance test pattern continuously upon detection of a Ping.LFPS when in Compliance Mode.	7.33 7.34
Subsection reference: 7.5.5.2 Exit from Compliance Mode		
7.5.5.2#1	A downstream port shall transition from Compliance Mode to Rx.Detect when directed to issue Warm Reset.	7.34
7.5.5.2#2	An upstream port shall transition from Compliance Mode to Rx.Detect upon detection of Warm Reset.	7.33
Subsection reference: 7.5.6 U0		
Subsection reference: 7.5.6.1 U0 Requirements		
7.5.6.1#1	The port shall maintain the low-impedance receiver termination (R _{RX-DC}) in U0.	NT
7.5.6.1#2	The LFPS receiver shall be enabled in U0.	IOP
7.5.6.1#3	A downstream port shall enable a 1-ms timer to measure the time interval between two consecutive link commands in U0.	7.16
7.5.6.1#4	An upstream port shall enable a 10-ms timer in U0. It shall be reset when the first symbol of any link command or packet is sent and restarted after the last symbol of any link command or packet is sent. This timer shall be active when the link is in	NT

Assertion #	Assertion Description	Test #
	logical idle.	
7.5.6.1#5	An upstream port shall transmit a single LUP when the 10- μ s timer expires in U0.	4.1
7.5.6.1#6	A downstream port shall transmit a single LDN when the 10- μ s timer expires in U0.	4.1
Subsection reference: 7.5.6.2 Exit from U0		
7.5.6.2#1	The port shall transition from U0 to Recovery upon detection of a TS1 ordered set.	NT
7.5.6.2#2	The port shall transition from U0 to Recovery when directed.	NT
7.5.6.2#3	The port shall transition from U0 to SS.Inactive when PENDING_HP_TIMER times out for the fourth consecutive time.	NT
7.5.6.2#4	A downstream port shall transition from U0 to SS.Inactive when directed.	NT
7.5.6.2#5	An upstream port shall transition from U0 to SS.Disabled when directed.	NT
7.5.6.2#6	A downstream port shall transition from U0 to Recovery upon not receiving any link commands within 1 ms.	7.16
7.5.6.2#7	A downstream port shall transition from U0 to Rx.Detect when directed to issue Warm Reset.	NT
7.5.6.2#8	An upstream port shall transition from U0 to Rx.Detect when Warm Reset is detected.	NT
7.5.6.2#9	An upstream port shall transition from U0 to SS.Disabled upon detection of VBUS off.	NT
7.5.6.2#10	A downstream port shall transition from U0 to SS.Inactive upon tPortConfiguration timeout	7.17
7.5.6.2#11	An upstream port shall transition from U0 to SS.Disabled upon tPortConfiguration timeout	7.17
Subsection reference: 7.5.7 U1		
Subsection reference : 7.5.7.1 U1 Requirements		
7.5.7.1#1	The port shall maintain its low-impedance receiver termination (R _{RX-DC}) in U1.	NT
7.5.7.1#2	The port shall enable U1 exit detect functionality in U1.	7.18 7.23
7.5.7.1#3	The port shall enable LFPS transmitter when it initiates the exit from U1.	IOP
7.5.7.1#4	The port shall enable its U2 inactivity timer upon entry to U1 when the U2 inactivity timer has a non-zero timeout value.	NT
7.5.7.1#5	A downstream port shall enable its Ping.LFPS detection in U1.	NT
7.5.7.1#6	A downstream port shall enable a 300-ms timer in U1. This timer will be reset and restarted when a Ping.LFPS is received.	NT
7.5.7.1#7	An upstream port shall transmit Ping.LFPS in U1.	NT
Subsection reference: 7.5.7.2 Exit from U1		

Assertion #	Assertion Description	Test #
7.5.7.2#1	A downstream port shall transition from U1 to Rx.Detect when the 300-ms timer expires.	NT
7.5.7.2#2	A downstream port shall transition from U1 to RxDetect when directed to issue Warm Reset.	NT
7.5.7.2#3	An upstream port shall transition from U1 to Rx.Detect when Warm Reset is detected.	NT
7.5.7.2#4	A self-powered upstream port shall transition from U1 to SS.Disabled upon not detecting valid VBUS.	NT
7.5.7.2#5	A port shall transition from U1 to U2 upon the timeout of the U2 inactivity timer.	NT
7.5.7.2#6	A port shall transition from U1 to Recovery upon completion of an LFPS handshake (U1 LFPS exit).	7.18 7.23
7.5.7.2#7	A port shall transition from U1 to SS.Inactive upon the 2-ms LFPS handshake timer timeout if a successful LFPS handshake is not achieved.	NT
Subsection reference: 7.5.8 U2		
Subsection reference: 7.5.8.1 U2 Requirements		
7.5.8.1#1	A port shall maintain its low-impedance receiver termination (R_{RX-DC}) in U2.	NT
7.5.8.1#2	A port shall enable its U2 exit detect functionality when in U2.	7.19 7.24
7.5.8.1#3	A port shall enable its LFPS transmitter when it initiates the exit from U2.	NT
7.5.8.1#4	A downstream port shall perform a far-end receiver termination detection every 100 ms in U2.	NT
Subsection reference: 7.5.8.2 Exit from U2		
7.5.8.2#1	A downstream port shall transition from U2 to Rx.Detect upon detection of a far-end high-impedance receiver termination ($Z_{HIGH-IMP-DC-POS}^{RX}$).	NT
7.5.8.2#2	A downstream port shall transition from U2 to Rx.Detect when directed to issue Warm Reset.	NT
7.5.8.2#3	An upstream port shall transition from U2 to Rx.Detect when Warm Reset is detected.	NT
7.5.8.2#4	A self-powered upstream port shall transition from U2 to SS.Disabled upon not detecting valid VBUS.	NT
7.5.8.2#5	A port shall transition from U2 to Recovery upon successful completion of a LFPS handshake (U2 LFPS exit).	7.19 7.24
7.5.8.2#6	The port shall transition from U2 to SS.Inactive upon the 2-ms LFPS handshake timer timeout if a successful LFPS handshake is not achieved.	NT
Subsection reference: 7.5.9 U3		
Subsection reference: 7.5.9.1 U3 Requirements		
7.5.9.1#1	The port shall maintain its low-impedance receiver termination	NT

Assertion #	Assertion Description	Test #
	(R _{RX-DC}) in U3.	
7.5.9.1#2	LFPS Ping detection shall be disabled in U3. (Downstream port Only.)	NT
7.5.9.1#3	The port shall enable its U3 wakeup detect functionality in U3.	7.25
7.5.9.1#4	The port shall enable its LFPS transmitter when it initiates the exit from U3.	7.36
7.5.9.1#5	A downstream port shall perform a far-end receiver termination detection every 100 ms in U3.	NT
Subsection reference: 7.5.9.2 Exit from U3		
7.5.9.2#1	A downstream port shall transition from U3 to Rx.Detect upon detection of a far-end high-impedance receiver termination (Z _{RX-HIGH-IMP-DC-POS}).	NT
7.5.9.2#2	A downstream port shall transition from U3 to Rx.Detect when directed to issue Warm Reset.	7.35
7.5.9.2#3	An upstream port shall transition from U3 to Rx.Detect when Warm Reset is detected.	NT
7.5.9.2#4	A self-powered upstream port shall transition from U3 to SS.Disabled upon not detecting valid VBUS.	NT
7.5.9.2#5	A port shall transition from U3 to Recovery upon successful completion of a LFPS handshake (U3 wakeup).	7.36 7.25
7.5.9.2#6	A port shall remain in U3 when the 10-ms LFPS handshake timer times out if a successful LFPS handshake is not achieved.	NT
Subsection reference: 7.5.10 Recovery		
Subsection reference: 7.5.10.3 Recovery.Active		
Subsection reference: 7.5.10.3.1 Recovery.Active Requirements		
7.5.10.3.1#1	A port shall transmit the TS1 ordered sets upon entry to Recovery.Active.	7.26 7.30
7.5.10.3.1#2	A port shall train its receiver with TS1 or TS2 ordered sets in Recover.Active.	7.26 7.30
Subsection reference: 7.5.10.3.2 Exit from Recovery.Active		
7.5.10.3.2#1	A port shall transition from Recovery.Active to Recovery.Configuration after eight consecutive and identical TS1 or TS2 ordered sets are received.	7.26 7.30
7.5.10.3.2#2	A port shall transition from Recovery.Active to SS.Inactive when either the U _x _EXIT_TIMER or the 12-ms timer times out.	NT
7.5.10.3.2#3	A downstream port shall transition from Recovery.Active to SS.Inactive when the transition to Recovery is not to attempt a Hot Reset AND the 12ms timer or U _x _EXIT_TIMER times out.	NT
7.5.10.3.2#5	A downstream port shall transition from Recovery.Active to Rx.Detect when the transition to Recovery is to attempt a Hot Reset AND the 12ms timer or the U _x _EXIT_TIMER times out.	7.31
7.5.10.3.2#6	A downstream port shall transition from Recovery.Active to	NT

Assertion #	Assertion Description	Test #
	Rx.Detect when directed to issue Warm Reset.	
7.2.10.3.2#7	An upstream port shall transition from Recovery.Active to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.10.4 Recovery.Configuration		
Subsection reference: 7.5.10.4.1 Recovery.Configuration Requirements		
7.5.10.4.1#1	The port shall transmit identical TS2 ordered sets upon entry to Recovery.Configuration and set the Reset bit, when directed.	7.28 7.29
7.5.10.4.1#2	If port that has Loopback Master Capability and is directed to go to Loopback, it shall transmit identical TS2 ordered sets with the Loopback bit set upon entry to Recovery.Configuration.	NT
7.5.10.4.1#3	If directed to disable scrambling, a port shall transmit identical TS2 ordered sets upon entry to this Recovery.Configuration with the Disabling Scrambling bit set.	NT
Subsection reference: 7.5.10.4.2 Exit from Recovery.Configuration		
7.5.10.4.2#1	The port shall transition from Recovery.Configuration to Recovery.Idle after the following two conditions are met; <ul style="list-style-type: none"> ▪ Eight consecutive and identical TS2 ordered sets are received. ▪ Sixteen TS2 ordered sets are sent after receiving the first of the eight consecutive and identical TS2 ordered sets. 	7.26 7.30
7.5.10.4.2#2	The port shall transition from Recovery.Configuration to SS.Inactive when either the Ux_EXIT_TIMER or the 6-ms timer times out. A downstream port cannot transition to Recovery as an attempt to Hot Reset.	NT
7.5.10.4.2#3	A downstream port shall transition from Recovery.Configuration to Rx.Detect when either the Ux_EXIT_TIMER or the 6-ms timer times out, and the transition to Recovery is to attempt a Hot Reset.	NT
7.5.10.4.2#4	A downstream port shall transition from Recovery.Configuration to Rx.Detect when directed to issue Warm Reset.	NT
7.5.10.4.2#5	An upstream port shall transition from Recovery.Configuration to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.10.5 Recovery.Idle		
Subsection reference: 7.5.10.5.1 Recovery.Idle Requirements		
7.5.10.5.1#1	A port shall transmit Idle Symbols in Recovery.Idle.	7.26 7.30
7.5.10.5.1#2	A port shall enable scrambling by default in Recovery.Idle.	7.26 7.30
7.5.10.5.1#3	In Recovery.Idle a port shall disable the scrambling when directed, or when the Disabling Scrambling bit is asserted in the TS2 ordered set received in Recovery.configuration.	NT
7.5.10.5.1#4	A port shall be able to receive the Header Sequence Number Advertisement from its link partner in Recovery.Idle.	NT

Assertion #	Assertion Description	Test #
Subsection reference: 7.5.10.5.2 Exit from Recovery.Idle		
7.5.10.5.2#1	A port shall transition from Recovery.Idle to Loopback when directed as a loopback master if the port is capable of being a loopback master.	NT
7.5.10.5.2#2	A port shall transition from Recovery.Idle to Loopback as a loopback slave when the Loopback bit is asserted in TS2 ordered sets.	NT
7.5.10.5.2#3	A port shall transition from Recovery.Idle to U0 when the following two conditions are met; <ul style="list-style-type: none"> ▪ Eight consecutive Idle Symbols are received. ▪ Sixteen Idle Symbols are sent after receiving one Idle Symbol. 	7.26 7.30
7.5.10.5.2#4	A port shall transition from Recovery.Idle to SS.Inactive when Ux_EXIT_TIMER or the 2-ms timer times out if the conditions to transition to U0 are not met.	NT
7.5.10.5.2#5	A downstream port shall transition from Recovery.Idle to Hot Reset when directed.	NT
7.5.10.5.2#6	A downstream port shall transition from Recovery.Idle to Rx.Detect when directed to issue Warm Reset.	NT
7.5.10.5.2#7	An upstream port shall transition from Recovery.Idle to Rx.Detect when Warm Reset is detected.	NT
7.5.10.5.2#8	An upstream port shall transition from Recovery.Idle to Hot Reset when the Reset bit is asserted in TS2 ordered sets.	NT
Subsection reference: 7.5.11 Loopback		
Subsection reference: 7.5.11.3.1 Loopback.Active Requirements		
7.5.11.3.1#1	A loopback master shall send valid 8b/10b data with SKPs as necessary when in Loopback.Active.	NT
7.5.11.3.1#2	A loopback slave shall retransmit the received 10-bit symbols when in Loopback.Active.	NT
7.5.11.3.1#3	A loopback slave shall not modify the received 10-bit symbols in Loopback.Active. (Other than SKP ordered set, which may be added or dropped.)	NT
7.5.11.3.1#4	The loopback slave shall process the BERT commands in Loopback.Active.	NT
7.5.11.3.1#5	The LFPS receiver shall be enabled in Loopback.Active.	NT
Subsection reference: 7.5.11.3.2 Exit from Loopback.Active		
7.5.11.3.2#1	A downstream port shall transition from Loopback.Active to Rx.Detect when directed to issue Warm Reset.	NT
7.5.11.3.2#2	An upstream port shall transition from Loopback.Active to Rx.Detect when Warm Reset is detected.	NT
7.5.11.3.2#3	When directed, loopback master shall transition from Loopback.Active to Loopback.Exit.	NT
7.5.11.3.2#4	A loopback slave shall transition from Loopback.Active to Loopback.Exit upon detection of Loopback LFPS exit handshake.	NT

Assertion #	Assertion Description	Test #
Subsection reference: 7.5.11.4 Loopback.Exit		
Subsection reference: 7.5.11.4.1 Loopback.Exit Requirements		
7.5.11.4.1#1	A LFPS transmitter and the LFPS receiver shall be enabled in Loopback.Exit.	NT
7.5.11.4.1#2	A port shall transmit and receive Loopback LFPS exit handshake in Loopback.Exit.	NT
Subsection reference: 7.5.11.4.2 Exit from Loopback.Exit		
7.5.11.4.2#1	A port shall transition from Loopback.Exit to Rx.Detect upon a successful Loopback LFPS exit handshake.	NT
7.5.11.4.2#2	A port shall transition from Loopback.Exit to SS.Inactive upon the 2-ms timer timeout if the condition to transition to Rx.Detect is not met	NT
7.5.11.4.2#3	A downstream port shall transition from Loopback.Exit to Rx.Detect when directed to issue Warm Reset.	NT
7.5.11.4.2#4	An upstream port shall transition from Loopback.Exit to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.12 Hot Reset		
Subsection reference: 7.5.12.2 Hot Reset Requirements		
7.5.12.2#1	A downstream port shall reset its PM timers and the U1 and U2 timeout value to zero in Hot Reset.	NT
Subsection reference: 7.5.12.3 Hot Reset.Active		
Subsection reference: 7.5.12.3.1 Hot Reset.Active Requirements		
7.5.12.3.1#1	Upon entry to this Hot Reset.Active, the port shall first transmit at least 16 TS2 ordered sets continuously with the Reset bit asserted.	7.27-29
7.5.12.3.1#2	In Hot Reset.Active a downstream port shall continue to transmit TS2 ordered sets with the Reset bit asserted until the upstream port transitions from sending TS2 ordered sets with the Reset bit asserted to sending the TS2 ordered sets with the Reset bit de-asserted.	7.29
7.5.12.3.1#3	An upstream port shall transmit TS2 ordered sets with the Reset bit asserted while performing the Hot Reset.	7.27-28
7.5.12.3.1#4	An upstream port shall transmit TS2 ordered sets with the Reset bit de-asserted after completing the Hot Reset.	7.27-28
Subsection reference: 7.5.12.3.2 Exit from Hot Reset.Active		
7.5.12.3.2#1	The port shall transition to Hot Reset.Exit when the following three conditions are met: <ul style="list-style-type: none"> ▪ At least 16 TS2 ordered sets with the Reset bit asserted are transmitted. ▪ Two consecutive TS2 ordered sets are received with the Reset bit de-asserted. ▪ Four consecutive TS2 ordered set with the Reset bit de-asserted are sent after receiving one TS2 ordered set with the Reset bit de-asserted. 	7.27-29

Assertion #	Assertion Description	Test #
7.5.12.3.2#2	The port shall transition from Hot Reset.Active to SS.Inactive upon the 12-ms timer timeout if the conditions to transition to Hot Reset.Exit are not met.	NT
7.5.12.3.2#3	A downstream port shall transition from Hot Reset.Active to Rx.Detect when directed to issue Warm Reset.	NT
7.5.12.3.2#4	An upstream port shall transition from Hot Reset.Active to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.12.4 Hot Reset.Exit		
Subsection reference: 7.5.12.4.1 Hot Reset.Exit Requirements		
7.5.12.4.1#1	A port shall transmit idle symbols in Hot Reset.Exit.	7.27-29
7.5.12.4.1#2	The port shall be able to receive the Header Sequence Number Advertisement from its link partner in Hot Reset.Exit.	NT
Subsection reference: 7.5.12.4.2 Exit from Hot Reset.Exit		
7.5.12.4.2#1	The port shall transition from Hot Reset.Exit to U0 when the following two conditions are met: <ul style="list-style-type: none"> ▪ Eight consecutive Idle Symbols are received. ▪ Sixteen Idle Symbols are sent after receiving one Idle Symbol. 	7.27-29
7.5.12.4.2#2	The port shall transition from Hot Reset.Exit to SS.Inactive upon the 2-ms timer timeout if the conditions to transition to U0 are not met.	NT
7.5.12.4.2#3	A downstream port shall transition from Hot Reset.Exit to Rx.Detect when directed to issue Warm Reset.	NT
7.5.12.4.2#4	An upstream port shall transition from Hot Reset.Exit to Rx.Detect when Warm Reset is detected.	NT
Chapter 8 Test Assertions: Protocol Layer		
Subsection reference: 8.3 Packet Formats		
Subsection reference: 8.3.1 Fields Common to all Headers		
Subsection reference: 8.3.1.1 Reserved Values and Reserved Field Handling		
8.3.1.1#1	A receiver shall ignore any Reserved field.	NT
8.3.1.1#2	A receiver shall ignore any packet that has any of its defined fields set to a reserved value, but it shall acknowledge the packet and return credit for the same.	NT
Subsection reference: 8.4 Link Management Packet (LMP)		
Subsection reference: 8.4.2 Set Link Function		
8.4.2#1	Upon receipt of an LMP with the Force_LinkPM_Accept bit is asserted, the upstream port shall accept all LGO_U1 and LGO_U2 Link Commands until the port receives an LMP with Force_LinkPM_Accept bit is de-asserted.	7.23-24
Subsection reference: 8.4.4 Vendor Device Test		

Assertion #	Assertion Description	Test #
8.4.4#1	The Vendor Device Test LMP shall not be used during normal operation of the link.	NT
Subsection reference: 8.4.5 Port Capabilities		
8.4.5#1	The port shall send the Port Capability LMP within tPortConfiguration time after completion of link initialization.	4.1 7.17
8.4.5#2	When the link partner that has downstream capability does not receive the Port Capability LMP within tPortConfiguration time, it shall signal an error.	NT
8.4.5#3	When the link partner that only supports upstream capability does not receive Port Capability LMP within tPortConfiguration time, it shall transition to SS.Disabled and try to connect at the other speeds this device supports.	7.17
8.4.5#4	After exchanging Port Capability LMPs, the link partners shall determine which of the link partners shall be configured as the downstream facing port.	NT
Subsection reference: 8.4.6 Port Configuration		
8.4.6#1	Any port that supports downstream port capability shall be capable of sending the Port Configuration LMP.	4.1
8.4.6#2	When the port that was to be configured in the upstream facing mode does not receive the Port Configuration LMP within tPortConfiguration time after link initialization, the upstream port shall transition to SS.Disabled and try and connect at the other speeds this device supports.	7.17
8.4.6#3	A port configured in the downstream mode shall send the Port Configuration LMP to the upstream port.	4.1
8.4.6#4	The port sending the Port Configuration LMP shall select only one bit for the Link Speed field.	NT
8.4.6#5	When a downstream capable port cannot work with its link partner, it shall signal an error as described in Section 10.14.2.6.	NT
Subsection reference: 8.4.7 Port Configuration Response		
8.4.7#1	A Port that supports upstream port capability shall be capable of sending the Port Configuration Response LMP.	4.1
8.4.7#2	When the downstream port does not receive the Port Configuration Response LMP within tPortConfiguration time, it shall signal an error as described in Section 10.14.2.6.	NT
8.4.7#3	When the Response Code indicates that the Link Speed was rejected by the upstream port, the downstream port shall signal an error as described in Section 10.14.2.6.	NT
Subsection reference: 8.6 Data Packet (DP)		
8.6#1	If no endpoints on this device have packets pending, then the device can use this information to aggressively manage its upstream link, e.g., set the link to a lower power U1 or U2 state.	7.37
Chapter 10 Test Assertions: Hub, Host Downstream Port, and Device Upstream Port Specification		
Subsection reference: 10.2 Hub Power Management		

Assertion #	Assertion Description	Test #
Subsection reference: 10.2.2 Hub Downstream Port U1/U2 Timers		
10.2.2#6	If a hub has received a valid packet on its upstream port that is routed to a downstream port, it shall reject U1 or U2 link entry attempts on the downstream port until the packet has been successfully transmitted.	NT
10.2.2#7	Hub implementation ensures no race condition when a header packet that has not been deferred is queued for transmission on a downstream port with a link that is in U1, U2, or is in the process of entering U1, U2	NT
Subsection reference: 10.3: Hub Downstream Facing Ports		
Subsection reference: 10.3.1: Hub Downstream Facing Port State Descriptions		
Subsection reference: 10.3.1.6: DSPORT.Resetting		
10.3.1.6#6	If the port initiates a hot reset on the link and the hot reset TS1/TS2 handshake fails, a warm reset is automatically tried.	7.31
10.3.1.6#7	When the downstream port link enters Rx.Detect.Active during a warm reset, the hub shall start a timer to count the time it is in Rx.Detect.Active. If this timer exceeds tTimeForResetError while the link remains in Rx.Detect.Active, the port shall transition to the DSPORT.Disconnected state.	7.32
Subsection reference: 10.4 Hub Downstream Facing Port Power Management		
Subsection reference: 10.4.2 Hub Downstream Facing Port State Descriptions		
Subsection reference: 10.4.2.1 Enabled U0 States		
10.4.2.1#14	Hub shall ensure that there is no race condition between a link partner initiating a U1/U2 request and transitioning to U0 based on SetPortFeature(PORT_LINK_STATE) request.	NT
XHCI Specification Chapter 5 Test Assertions: Register Interface		
Subsection reference: xHCI 5.4 Host Controller Operational Registers		
Subsection reference: xHCI 5.4.8 Port Status and Control Register (PORTSC)		
5.4.8	The xHC shall set the PLC bit of the PORTSC register of a USB3 port to '1' when an Error occurs (the link transitions from any state -> Inactive).	NT

4 Timing Definitions

The USB 3.0 Specification defines the timers used in the Link Layer. . To accurately test timer implementations, there are several considerations beyond the simple timer definition that factor into this document's timing scheme. Section 7.5 of the USB 3.0 Specification defines the link layer timers to have an implementation tolerance of +50%. Chapter 6 details an SSC Tolerance of -5300/+300ppm, the lower limit of which could add 0.5% time to any interval. Consideration for Physical Layer and Link Layer processing time (Tx and Rx latency time) is also applied.

The following expression is used for determining each timer's high-end value used in this specification:

$$\text{Spec Defined Timer value} \times \text{Additional50pctTolerance} \times \text{SSCFactor} + \text{tLinkTurnAround}$$

Spec Defined Timer value = the timer value defined in USB 3.0 specification.

Additional50pctTolerance = +50% tolerance defined in the Section 7.5 of the USB 3.0 specification.

SSCFactor = delay induced by SSC influenced clock with a maximum SSC of 5000ppm applied, equating to +0.5%.

tLinkTurnAround = the maximum delay induced by the PHY and Link layers when a link event occurs, until the respective action is made. This is measured from the time a packet is received, until the time a response is generated on the transmit side. This amounts to a maximum of 500ns. This includes tACKResponse (400ns, which closely approximates the link+PHY Tx and Rx latency), Link layer transmit scheduling latency, and potential delay from SKP transmissions.

Using their respective numerical values, the expression is presented again below:

$$\text{Spec Defined Timer value} \times 1.5 \times 1.005 + 500\text{ns}$$

The expression above is applicable for Link Layer timers.

$$\text{Spec Defined Timer value} \times 1.005 + 500\text{ns}$$

The expression above is applicable for PHY and protocol layer timers.

The following table lists the timers used in the Link Layer compliance tests and the window of compliant durations between the initial event that started the timer, and the expected response when the timer expires.

PORT_U2_TIMEOUT is not listed in the table because its value is programmable using the U2 Inactivity Timeout LMP. A calculation is needed as per the value programmed.

tPollingLFPSEstablishedTimeout was created from USB 3.0 Specification section 7.5.4.3.1: A Port shall establish its LFPS operating condition within 80us.

Timer definition	Timer expiration deadline (USB 3.0 specification defined value)	Timer expiration time (Calculated test time)
tLinkTurnAround		500ns
tRxDetectQuietTimeout	12ms	18.0905ms
tPollingLFPSTimeout	360ms	542.7005ms
tPollingLFPSEstablishedTimeout		80us
tPollingActiveTimeout	12ms	18.0905ms
tPollingConfigurationTimeout	12ms	18.0905ms

tRecoveryActiveTimeout	12ms	18.0905ms
tRecoveryConfigurationTimeout	6ms	9.0453ms
tU0RecoveryTimeout	1ms	1.5080ms
tHotResetActiveTimeout	12ms	18.0905ms
CREDIT_HP_TIMER	5ms	7.5380ms
PENDING_HP_TIMER	3 μ s	5.0225 μ s
PM_LC_TIMER	3 μ s	5.0225 μ s
PM_ENTRY_TIMER	6 μ s	9.545 μ s
Ux_EXIT_TIMER	6ms	9.0455ms
tPortConfiguration	20 μ s	20.6 μ s
tNoLFPSResponseTimeout for U1/2	2ms	2.0105ms
tNoLFPSResponseTimeout for U3	10ms	10.0505ms
tU3WakeupRetryDelay	100ms	150.7505ms

Table 4-1

Note +/- 100ns applies to Timer Expiration Times in Table 4-1 above.

5 Test Descriptions

5.1 Link Initialization Sequence

Most of the following test descriptions (TDs) refer to the Link Initialization Sequence, described here. The purpose of the Link Initialization Sequence is to establish the link between the LVS and the PUT and check that link establishment and initialization is followed properly by the PUT.

Some tests are designed to follow the Link Initialization Sequence up to a certain point and then introduce different test steps. This is reflected in each specific TD.

Covered Assertions

7.2.4.1.1#6,8,10-17,22

7.2.4.1.4#2

7.3.4#2

7.5.6.1#5,6

8.4.5#1

8.4.6#1,3 (downstream)

8.4.7#1 (upstream)

Link Initialization Sequence

1. The LVS and the PUT go through the initial steps of the LTSSM (SS.Disabled, Rx.Detect, Polling) to reach U0.
2. Once in U0, the LVS will transmit the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement.
3. The LVS verifies that the Header Sequence Number Advertisement transmitted by the PUT is LGOOD_7 and that the PUT transmits the following Rx Header Buffer Credit Advertisements: LCRD_A, LCRD_B, LCRD_C and LCRD_D.
4. The LVS and the PUT will exchange Port Configuration transactions.
 - If the LVS is configured as a Downstream Port:
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP.
 - d. LVS transmits a valid Port Configuration LMP to the PUT.
 - e. LVS waits for the PUT Port Configuration Response LMP.
 - f. LVS verifies that the Port Configuration Response LMP is valid.
 - If the LVS is configured as an Upstream Port:
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.

- c. LVS transmits its Port Capability LMP.
 - d. LVS waits for the PUT to transmit the Port Configuration LMP.
 - e. LVS verifies that the Port Configuration LMP is valid.
 - f. LVS transmits a Port Configuration Response LMP to the device.
5. The test fails if the Port Configuration transaction is not completed before tPortConfiguration expires.
 6. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.

The Link Initialization Sequence passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.

5.2 Physical Layer

TD.6.1 Lane Polarity Inversion Test

This test verifies that the PUT can successfully handle reception of lane polarity inversion.

Covered Assertions

(No Physical Layer assertions defined)

7.5.4.4.1#1

Overview of Test Steps

1. Invert the LVS TX lane polarity.
2. Bring the link to U0 using the Link Initialization Sequence.
3. The test passes if the Link Initialization Sequence passes.

TD.6.2 Skip Test

This test verifies that the PUT supports all possible skip (SKP) combinations. Combinations to be tested:

- A. Repetition of one skip ordered set followed by 354 symbols (word aligned)
- B. Repetition of one skip ordered set followed by 353 symbols (word misaligned)
- C. Repetition of two skip ordered sets followed by 708 symbols (word aligned)
- D. Repetition of two skip ordered sets followed by 707 symbols (word misaligned)
- E. Repetition of three skip ordered sets followed by 1,062 symbols (word aligned)
- F. Repetition of three skip ordered sets followed by 1,061 symbols (word misaligned)
- G. Repetition of four skip ordered sets followed by 1,416 symbols (word aligned)
- H. Repetition of four skip ordered sets followed by 1,415 symbols (word misaligned)

Covered Assertions

(No Physical Layer assertions defined)

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms. Skips will be generated according to the first pattern described above.

3. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.
4. Repeat the steps with the other skip patterns listed above.

TD.6.3 Elasticity Buffer Test

This test verifies that the PUT's elasticity buffer supports the required frequency range, from -5,300 to 300ppm.

Covered Assertions

(No Physical Layer assertions defined)

Overview of Test Steps

1. Configure the LVS with an SSC clock of -5300ppm.
2. Bring the link to U0 using the Link Initialization Sequence.
3. The test passes if the Link Initialization Sequence passes.
4. Repeat the above steps with an SSC clock of +300ppm.

TD.6.4 LFPS Frequency Test

This test verifies that the PUT's LFPS detector supports the required frequency range. The periods to be tested are:

- A. tPeriod = 10 MHz (min)
- B. tPeriod = 50 MHz (max)

Covered Assertions

(No Physical Layer assertions defined)

Overview of Test Steps

1. The LVS and the PUT go through the initial steps of the LTSSM (SS.Disabled, Rx.Detect) to reach Polling.LFPS.
2. The LVS will start generating a Polling.LFPS signal having durations of tBurst = 1 us and tRepeat = 10 us. The burst period will be set to the first period listed above.
3. The test passes if the PUT moves successfully to Polling.RxEQ according to section 7.5.4.3.2 of the USB 3.0 specification.
4. Repeat the steps with the other period listed above.

TD.6.5 Polling.LFPS Duration Test

This test verifies that the PUT's Polling.LFPS detector supports the required duration range. Here are the durations to be tested:

- A. tBurst = 0.6 us and tRepeat = 6 us
- B. tBurst = 0.6 us and tRepeat = 14 us

- C. tBurst = 1.4 us and tRepeat = 6 us
- D. tBurst = 1.4 us and tRepeat = 14 us

Covered Assertions

(No Physical Layer assertions defined)

Overview of Test Steps

1. The LVS and the PUT go through the initial steps of the LTSSM (SS.Disabled, Rx.Detect) to reach Polling.LFPS.
2. The LVS will start generating a Polling.LFPS signal having the first duration specified in the list above.
3. The test passes if the PUT moves successfully to Polling.RxEQ according to section 7.5.4.3.2, and if the Polling.LFPS tPeriod, tBurst and tRepeat from the PUT are within the ranges specified in section 6.9.1.
4. Repeat the steps with the other durations listed above.

5.3 Link Layer

TD.7.1 Link Bring-up Test

This test verifies that the Link Verification System (LVS) and the Port under Test (PUT) can reach U0 successfully.

Covered Assertions

Refer to the list of covered assertions for the Link Initialization Sequence

Overview of Test Steps

1. The LVS starts the link process.
 - If the LVS is configured as a Downstream Port, the LVS asserts VBUS. The PUT should move from SS.Disabled to Rx.Detect.
 - If the LVS is configured as an Upstream Port, the LVS asserts Terminations. The PUT should already be in Rx.Detect.
2. The test fails if the PUT does not transmit Polling.LFPS bursts before tRxDetectQuietTimeout + tPollingLFPSEstablishedTimeout expires.
3. The LVS transmits Polling.LFPS bursts.
4. The test fails if any of the following occur:
 - a. The PUT does not transmit at least sixteen consecutive Polling.LFPS bursts.
 - b. The PUT does not transmit at least four consecutive Polling.LFPS bursts after receiving one Polling.LFPS bursts.
 - c. The PUT transitions away from Polling.LFPS before the LVS sends at least two consecutive Polling.LFPS bursts.
 - d. The PUT does not transition from Polling.LFPS before tPollingLFPSTimeout expires.
5. The LVS transmits TSEQ ordered sets.
6. The test fails if any of the following occur:
 - a. The PUT does not transmit TSEQ ordered sets.

- b. The PUT transmits SKP Ordered Sets, Idle Symbols, or any other Packet, Symbol or Ordered Set during TSEQ transmission or between TSEQ ordered sets.
7. The LVS transmits TS1 ordered sets and waits to receive eight consecutive and identical TS1 or TS2 ordered sets from the PUT.
8. The test fails if any of the following occur:
 - a. The PUT does not transmit TS1 ordered sets.
 - b. The PUT transmits TS2s before the LVS sends eight consecutive and identical TS1s or TS2s.
 - c. The PUT interrupts a TS1 ordered set to transmit a SKP ordered set (between TS1 ordered sets is OK).
 - d. The PUT transmits Idle Symbols or any other Packet.
 - e. The PUT continues to transmit TS1 ordered sets after tPollingActiveTimeout expires.
9. The LVS transmits TS2 ordered sets and readies to complete the Polling.Configuration handshake.
10. The test fails if any of the following occur:
 - a. The PUT does not transmit at least sixteen consecutive TS2 ordered sets after receiving one TS2 ordered set.
 - b. The PUT sends Idle symbols before the LVS sends at least eight consecutive TS2 ordered sets.
 - c. The PUT interrupts transmission of a TS2 ordered set to transmit a SKP ordered set (between TS2 ordered sets is OK).
 - d. The PUT continues to transmit TS2 ordered sets after tPollingConfigurationTimeout expires.
11. The LVS transmits Idle symbols.
12. The test fails if any of the following occur:
 - a. The PUT does not transmit sixteen Idle Symbols after TS2 ordered sets.
 - b. The PUT transmits the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before the LVS transmits 8 Idle symbols.
 - c. The PUT enters recovery after Idle symbols have been exchanged.
 - d. Upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before their respective timeouts, PENDING_HP_TIMER and CREDIT_HP_TIMER, expire.
13. The LVS and PUT continue the test with the Link Initialization Sequence starting at step two.

TD.7.2 Link Commands Framings Robustness Test

This test verifies that the PUT can tolerate link commands having one symbol error in the LCSTART framing. Here are the combinations to be tested:

- A. ERR SLC SLC EPF
- B. SLC ERR SLC EPF
- C. SLC SLC ERR EPF
- D. SLC SLC SLC ERR

The Port Configuration transaction will be used for this purpose.

Covered Assertions

7.3.4#1,2

Overview of Test Steps

1. Perform the Link Initialization Sequence, but transmit all LCRD_X with an error in the first LCSTART symbol.
2. The test passes if the Link Initialization Sequence passes.
3. Repeat the above steps with an error in the second, third, and fourth LCSTART symbols as shown above.

TD.7.3 Link Commands CRC-5 Robustness Test

This test verifies that the PUT will ignore link commands with a CRC-5 error, even if only one of the Link Command Words has a CRC-5 error. The Port Configuration transaction will be used for this purpose.

The tested CRC-5 error robustness conditions are:

- A. Incorrect CRC-5 in first Link Command Word
- B. Incorrect CRC-5 in second Link Command Word
- C. Both Link Command Words have an incorrect CRC-5.

Covered Assertions

7.3.4#2

Overview of Test Steps

1. Perform the Link Initialization Sequence but transmit all LCRD_X with condition A above.
2. The test passes if the PUT enters recovery when CREDIT_HP_TIMER expires.
3. Repeat the above steps for each condition listed above. .

TD.7.4 Invalid Link Commands Test

This test verifies that the PUT will ignore Link Commands with link command information in the first LCW not the same as link command information in the second LCW, and both pass the CRC5 check.

Covered Assertions

7.3.4#2

Overview of Test Steps

1. Do steps 1 to 5 of the Link Initialization Sequence.
2. The LVS sends a link command with LGO_U1 in the first LCW and LGO_U2 in the second LCW, with good CRC-5 calculations on both.
3. The test fails if the PUT responds with an LAU or LXU.
4. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
5. The test passes if the link command is ignored, all exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received by the PUT, all credits are restored and the link stays in U0 for at least 50ms.

TD.7.5 Header Packet Framing Robustness Test

This test verifies that the PUT does not invalidate header packets having one symbol error in the HPSTART framing. The combinations to be tested:

- A. ERR SHP SHP EPF
- B. SHP ERR SHP EPF
- C. SHP SHP ERR EPF
- D. SHP SHP SHP ERR

The Port Configuration transaction will be used for this purpose.

Covered Assertions

7.2.4.1.4#1

Overview of Test Steps

1. Perform the Link Initialization Sequence, but transmit all Header Packets with an error in the first HPSTART symbol.
2. The test passes if the Link Initialization Sequence passes.
3. Repeat the above steps with an error in the second, third, and fourth HPSTART symbols, as shown above.

TD.7.6 Data Payload Packet Framing Robustness Test

This test verifies that the PUT does not invalidate data payload packets having a single character framing error in DPPSTART and DPPEND. The combinations to be tested:

- A. ERR SDP SDP EPF
- B. SDP ERR SDP EPF
- C. SDP SDP ERR EPF
- D. SDP SDP SDP ERR
- E. ERR END END EPF
- F. END ERR END EPF
- G. END END ERR EPF
- H. END END END ERR

When the LVS is a Downstream Port, it will place framing errors on Setup DP Packets.

When the LVS is an Upstream Port, it will reply to the GetDeviceDescriptor request with a DPP containing framing errors.

Covered Assertions

7.2.4.1.6#1,2

Overview of Test Steps

1. Perform the Link Initialization Sequence.
2. At this stage the Downstream Port is expected to issue a GetDeviceDescriptor request.
 - If the LVS is configured as an Upstream Port:

- a. The LVS prompts the test operator to have the PUT send a GetDeviceDescriptor request through USB30CV and then press “OK”.
 - b. The test fails if no GetDeviceDescriptor request is received and the test operator has pressed “OK”.
 - c. When the LVS receives a GetDeviceDescriptor request, it closes the prompt. The LVS will respond to the request with a DPP containing the Device Descriptor data which includes the first framing error listed above.
 - If the LVS is configured as a Downstream Port, it will issue a GetDeviceDescriptor request, but will send the SETUP DP with the first framing error listed above.
3. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
 4. The test fails if the data exchange fails on the protocol level.
 5. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received by the PUT, all credits are restored and the link stays in U0 for at least 50ms.
 6. Repeat for each condition listed above.

TD.7.7 RX Header Packet Retransmission Test

This test verifies that the PUT will send an LBAD if an invalid header packet is received, and that the retransmission will be correctly handled.

The tested conditions invalidating a header packet are:

- A. Incorrect CRC-16
- B. Incorrect CRC-5
- C. K28.2 SDP symbol in HP data
- D. K28.3 EDB symbol in HP data
- E. K28.4 SUB symbol in HP data
- F. K28.6 Reserved K-symbol in HP data
- G. K27.7 SHP symbol in HP data
- H. K29.7 END symbol in HP data
- I. K30.7 SLC symbol in HP data
- J. K23.7 EPF symbol in HP data

Each of the conditions C – J are tested in the following positions, one case at a time:

1. Position 2: SHP SHP SHP EPF DX.X KX.X DX.X DX.X
2. Position 5: SHP SHP SHP EPF DX.X DX.X DX.X DX.X KX.X

Covered Assertions

7.2.4.1.4#3, 4

Overview of Test Steps

1. Do steps 1 to 3 of the Link Initialization Sequence.
2. The LVS and the PUT will exchange Port Configuration transactions, but the first packet sent by the LVS will be invalid.
 - If the LVS is configured as a Downstream Port:
 - a. The LVS waits for the PUT’s Port Capability LMP.

- b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP with the first invalid condition listed above.
 - d. LVS verifies that the PUT replies with an LBAD.
 - e. LVS transmits a LRTY and then retransmits the packet.
 - f. LVS transmits the Port Configuration LMP.
 - g. LVS waits for the PUT's Port Configuration Response LMP.
 - h. LVS verifies the PUT's Port Configuration Response LMP.
- If the LVS is configured as an Upstream Port:
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP with the first invalid condition listed above.
 - d. LVS verifies the PUT replies with an LBAD.
 - e. LVS transmits a LRTY and then retransmits the packet.
 - f. LVS waits for the PUT's Port Configuration LMP.
 - g. LVS verifies the PUT's Port Configuration LMP.
 - h. LVS transmits its Port Configuration Response LMP.
3. The LVS will keep the link active by sending Link Pollings (LUP when the LVS is configured as Upstream Port, or LDN when the LVS is configured as a Downstream Port) for 50ms.
 4. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, the PUT responds to the invalid packets with an LBAD, all other packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.
 5. Repeat the above steps for each of the invalid conditions listed above.

TD.7.8 TX Header Packet Retransmission Test

This test verifies that the PUT will correctly retransmit a header packet on receipt of an LBAD.

Covered Assertions

7.2.4.1.3#1, 2

Overview of Test Steps

1. Do steps 1 to 3 of the Link Initialization Sequence.
2. The LVS and the PUT will exchange the Port Configuration transaction, but in this case the LVS will respond to the first packet sent by the PUT with an LBAD.
 - If the LVS is configured as a Downstream Port:
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS responds to the PUT with an LBAD.
 - d. LVS waits for the PUT to transmit an LRTY.
 - e. LVS waits for the retransmitted packet.

- f. LVS verifies that the retransmitted packet is the same as the first packet sent by the device.
 - g. LVS transmits its Port Capability LMP and Port Configuration LMP.
 - h. LVS waits for the PUT Port Configuration Response LMP.
 - i. LVS verifies the PUT's Port Configuration Response LMP.
- If the LVS is configured as an Upstream Port:
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP.
 - d. LVS responds to the PUT with an LBAD.
 - e. LVS waits for the PUT to transmit an LRTY.
 - f. LVS waits for the retransmitted packet.
 - g. LVS verifies that the retransmitted packet is the same as the first packet sent by the device.
 - h. LVS waits for the PUT's Port Configuration LMP.
 - i. LVS verifies that the Port Configuration LMP is valid.
 - j. LVS transmits its Port Configuration Response LMP.
3. The LVS will keep the link active by sending Link Pollings (LUP when it was configured as an Upstream Port, LDN when it was configured as a Downstream Port) for 50ms.
 4. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, the packet that the LVS responded to with an LBAD is retransmitted correctly, all other packets are received successfully, all credits are restored and the link stays in U0 for at least 50ms.

TD.7.9 PENDING_HP_TIMER Deadline Test

This test verifies that the PUT will accept an LGOOD_N sent at the PENDING_HP_TIMER deadline. The Port Configuration transaction will be used for this purpose.

Covered Assertions

7.2.4.1.10#2

Overview of Test Steps

1. Perform the Link Initialization Sequence, but transmit all the LGOOD_N responses tLinkTurnAround prior to the PENDING_HP_TIMER deadline.
2. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
3. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.

TD.7.10 CREDIT_HP_TIMER Deadline Test

This test verifies that the PUT will accept an LCRD_X sent at the CREDIT_HP_TIMER deadline. The Port Configuration transaction will be used for this purpose.

Covered Assertions

7.2.4.1.10#7

Overview of Test Steps

1. Perform the Link Initialization Sequence but transmit all LCRD_X responses tLinkTurnAround prior to the CREDIT_HP_TIMER deadline.
2. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
3. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.

TD.7.11 PENDING_HP_TIMER Timeout Test

This test verifies that the PUT will go to recovery when the PENDING_HP_TIMER expires.

Covered Assertions

7.2.4.1.10#1

Overview of Test Steps

1. Do steps 1 to 3 of the Link Initialization Sequence.
2. The LVS and the PUT will exchange the Port Configuration transaction, but the LVS will respond (with an LGOOD) to the first LMP packet sent by the PUT after expiration of the PENDING_HP_TIMER.
 - If the LVS is configured as a Downstream Port:
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS will not respond to the PUT with an LGOOD.
 - d. LVS transmits its Port Capability LMP and Port Configuration LMP.
 - If the LVS is configured as an Upstream Port:
 - a. LVS waits for the PUT to transmit its Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its PUT Port Capability LMP.
 - d. LVS will not respond to the PUT with an LGOOD.
3. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port, LDN when it is configured as a Downstream Port).
4. The test passes if the PUT goes to recovery after the PENDING_HP_TIMER deadline and before the PENDING_HP_TIMER expires.

TD.7.12 CREDIT_HP_TIMER Timeout Test

This test verifies that the PUT will go to recovery when the CREDIT_HP_TIMER expires.

Covered Assertions

7.2.4.1.10#6

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence with the exception that the LVS will not send any LCRD_X.
2. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port, LDN when it is configured as a Downstream Port).
3. The test passes if the PUT goes to recovery after the CREDIT_HP_TIMER deadline and before the CREDIT_HP_TIMER expires.

TD.7.13 Wrong Header Sequence Test

This test verifies that the PUT will go to recovery when it receives a wrong header sequence.

Covered Assertions

7.3.5#1

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence, with the exception that the LVS will send two LMP packets with Header Sequence Numbers that are not sequential.
2. The test passes if the PUT goes to recovery within tLinkTurnAround after reception of the LMP packet with a Header Sequence Number that is not sequential.

TD.7.14 Wrong LGOOD_N Sequence Test

This test verifies that the PUT will go to recovery when it receives an incorrect LGOOD_N sequence.

Covered Assertions

7.3.4#4

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence, with the exception that the LVS will send an LGOOD_0 for the first LMP packet as expected, but will send an LGOOD_n with $n \neq 1$ for the second LMP packet.
2. The test passes if the PUT goes to recovery within tLinkTurnAround after reception of the incorrect LGOOD_n.

TD.7.15 Wrong LCRD_X Sequence Test

This test verifies that the PUT will go to recovery when it receives an incorrect LCRD_X sequence.

Covered Assertions

7.3.4#5

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence, with the exception that the LVS will send an LCRD_A for the first LMP packet as expected, but will send an LCRD_X with $X \neq B$ for the second LMP packet. respond with LCRD_X the invalid condition listed above.
2. The test passes if the PUT goes to recovery within tLinkTurnAround after reception of the incorrect LCRD_X.

TD.7.16 Link Command Missing Test (Upstream Port Only)

This test verifies that the PUT will go to Recovery if no Link Commands are received for more than tU0RecoveryTimeout.

Please note that the downstream LVS port shall disable transmission of ITPs.

Covered Assertions

- 7.3.4#7, 8
- 7.5.6.1#3
- 7.5.6.2#6

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS will not send LDNs or any other link commands.
3. The test fails if the PUT goes to Recovery before the tU0RecoveryTimeout deadline, or if it does not go to Recovery after tU0RecoveryTimeout expires.

TD.7.17 tPortConfiguration Time Timeout Test

This test verifies that a downstream PUT will go to SS.Inactive if tPortConfiguration expires, and an upstream PUT will go to SS.Disabled if tPortConfiguration expires.

Covered Assertions

- 7.5.6.2#10,11
- 8.4.5#1,3
- 8.4.6#2

Overview of Test Steps

1. Do steps 1 to 3 of the Link Initialization Sequence.
2. The LVS does not transmit both the Port Capability LMP and Port Configuration LMP.
3. The test fails if any of the following occur:

- a. The PUT transitions to SS.Inactive (downstream PUT) or SS.Disabled (upstream PUT) before tPortConfiguration deadline.
 - b. The PUT does not transition to SS.Inactive (downstream PUT) or SS.Disabled (upstream PUT) after tPortConfiguration expires.
 - c. The PUT sends any other packets or LFPS signals.
 - d. The PUT enters recovery.
4. Do steps 1 to 3 of the Link Initialization Sequence.
 5. The LVS waits for the Port Capability LMP from the PUT.
 6. LVS verifies that the Port Capability LMP is valid.
 7. The LVS transmits the Port Capability LMP, but does not transmit the Port Configuration LMP (downstream LVS port) or Port Configuration Response LMP (upstream LVS port).
 8. The test fails if any of the following occur:
 - a. The PUT does not transmit the Port Capability LMP.
 - b. The PUT transitions to SS.Inactive (downstream PUT) or SS.Disabled (upstream PUT) before tPortConfiguration deadline.
 - c. The PUT does not transition to SS.Inactive (downstream PUT) or SS.Disabled (upstream PUT) after tPortConfiguration expires.
 - d. The PUT sends any other packets or LFPS signals.
 - e. The PUT enters recovery.
 9. Do steps 1 to 3 of the Link Initialization Sequence
 10. The LVS does not transmit the Port Capability LMP, but does send the Port Configuration LMP (downstream LVS port) or Port Configuration Response LMP (upstream LVS port).
 11. The test fails if any of the following occur:
 - a. The PUT does not transmit the Port Capability LMP.
 - b. The PUT transitions to SS.Inactive (downstream PUT) or SS.Disabled (upstream PUT) before tPortConfiguration deadline.
 - c. The PUT does not transition to SS.Inactive (downstream PUT) or SS.Disabled (upstream PUT) after tPortConfiguration expires.
 - d. The PUT sends any other packets or LFPS signals.
 - e. The PUT enters recovery.

TD.7.18 Low Power initiation for U1 test (Downstream Port Only)

This test verifies that the PUT initiates U1 state.

Covered Assertions

7.2.4.2.2#1

7.2.4.2.3#1,3,4,5,7,8

7.2.4.2.7#2,3

7.5.7.1#2

7.5.7.2#6

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS application prompts the test operator to enable and configure the U1 and U2 inactivity timers through USB30CV. CV will set the U1 Timeout field to 7Fh and the U2 Timeout field to 00h.
3. The LVS waits to receive an LGO_U1 from the PUT. The LVS transmits an LXU, when it receives the LGO_U1.
4. The test fails if the PUT sends an LPMA, or if recovery is entered.
5. The LVS waits to receive an LGO_U1 from the PUT again.
6. The LVS transmits an LAU when it receives the LGO_U1.
7. The test fails if any of the following conditions occur:
 - a. The PUT does not transmit an LPMA before PM_ENTRY_TIMER deadline
 - b. The PUT enters recovery
 - c. The PUT does not transition to U1
8. The LVS transmits the U1 Exit LFPS to transition to U0 and waits to receive U1 Exit LFPS to complete the U1 Exit LFPS handshake.
9. The test fails if the LFPS handshake does not conform to the following specifications from section 6.9.2:
 - a. Between 300ns – 900ns elapses between the start of the LVS U1 Exit LFPS and the start of the PUT U1 Exit LFPS.
 - b. The PUT U1 Exit LFPS duration is within 600ns – 900ns.
 - c. The PUT enters U0 before Ux_EXIT_TIMER deadline.
 - d. The PUT enters Recovery before tNoLFPSResponseTimeout deadline after the start of its U1 exit LFPS.
10. The test passes if all packets are successful, recovery is entered once, no extra packets or LFPS signals are received, and the PUT returns to U0.
11. After the LVS completes this test case, clear the U1/U2 registers through the CV prompt.

TD.7.19 Low Power initiation for U2 test (Downstream Port Only)

This test verifies that the PUT initiates U2 state.

Covered Assertions

- 7.2.4.2.2#1,
- 7.2.4.2.3#1,3,4,5,7,8
- 7.2.4.2.7#2,3
- 7.5.8.1#2
- 7.5.8.2#5

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
 The LVS application prompts the test operator to enable and configure the U1 and U2 inactivity timers through USB30CV. CV will set the U1 Timeout field to 00h and the U2 Timeout field to 7Fh.

2. The LVS waits to receive an LGO_U2 from the PUT.
3. The LVS transmits an LXU when it receives the LGO_U2.
4. The test fails if the PUT sends an LPMA, or if recovery is entered.
5. The LVS waits to receive an LGO_U2 from the PUT again.
6. The LVS transmits an LAU when it receives the LGO_U2.
7. The test fails if any of the following occur:
 - a. The PUT does not transmit an LPMA before PM_ENTRY_TIMER deadline.
 - b. The PUT enters recovery
 - c. The PUT does transition to U2.
8. The test fails if the PUT does not transition to U2.
9. The LVS transmits the U2 Exit LFPS to transition to U0 and waits to receive U2 Exit LFPS to complete the U2 Exit LFPS handshake.
10. The test fails if the LFPS handshake does not conform to the following specifications from section 6.9.2:
 - a. Between 300ns – 2ms elapses between the start of the LVS U2 Exit LFPS and the start of the PUT U2 Exit LFPS.
 - b. The PUT U2 Exit LFPS duration is within 80us – 2ms.
 - c. The PUT enters U0 before Ux_EXIT_TIMER deadline.
 - d. The PUT enters Recovery before tNoLFPSResponseTimeout deadline after the start of its U2 exit LFPS.
11. The test passes if all packets are successful, recovery is entered once, no extra packets or LFPS signals are received, and the PUT returns to U0.
12. After the LVS completes this test case, clear the U1/U2 registers through the CV prompt.

TD.7.20 PM_LC_TIMER Deadline Test (Downstream Port Only)

This test verifies that the PUT accepts an LGO_U1 sent at the PM_LC_TIMER deadline.

Covered Assertions

7.2.4.2.1#1, 2

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS application prompts the test operator to enable and configure the U1 and U2 inactivity timers through USB30CV. CV will set the U1 Timeout field to 7Fh and the U2 Timeout field to 00h.
3. The LVS waits to receive an LGO_U1 from the PUT.
4. The LVS transmits an LAU tLinkTurnAround before the PM_LC_TIMER deadline.
5. The test fails if the PUT does not transmit an LPMA after receiving the LAU.
6. After the LVS completes this test case, clear the U1/U2 registers through the CV prompt.

TD.7.21 PM_LC_TIMER Timeout Test (Downstream Port Only)

This test verifies that the PUT transitions to Recovery when the PM_LC_TIMER expires.

Covered Assertions

7.2.4.2.1#1
7.2.4.2.3#6
7.3.4#6

Overview of Test Steps

1. Do steps 1 to 3 of TD.7.18.
2. The LVS does not transmit LAU when it receives the LGO_U1.
3. The test fails if the PUT does not transition to Recovery when the PM_LC_TIMER expires.
4. After the LVS completes this test case, clear the U1/U2 registers through the CV prompt.

TD.7.22 PM_ENTRY_TIMER Timeout Test (Upstream Port Only)

This test verifies that the PUT transitions to a low power state when the PM_ENTRY_TIMER expires.

Covered Assertions

7.2.4.2.1#3,7,2.4.2.3#8,10,12

Overview of Test Steps

1. Do steps 1 to 4 of TD.7.23.
2. The LVS does not transmit LPMA when it receives LAU.
3. The test fails if the PUT does not transition to U1 when the PM_ENTRY_TIMER expires, the PUT does not transmit LAU, or if the PUT sends any packet or LFPS.

TD.7.23 Accepted Power Management Transaction for U1 Test (Upstream Port Only)

This test verifies that the PUT transitions to U1 if it receives LGO_U1.

Covered Assertions

7.2.4.1.1#7,9
7.2.4.2.1#4
7.2.4.2.2#2,3
7.2.4.2.3#2,8,9
7.2.4.2.7#2,3
7.5.5.1#2
7.5.5.2#2
7.5.7.1#2
7.5.7.2#2

8.4.2#1

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS transmits the Set Link Function LMP with the Force_LinkPM_Accept bit asserted.
3. The LVS transmits an LGO_U1 and waits to receive an LAU from the PUT.
4. The test fails if the PUT does not transmit an LAU before PM_LC_TIMER deadline, or recovery is entered.
5. The LVS transmits an LPMA and then transition to U1.
6. The test fails if the PUT does not transition to U1 when the PM_ENTRY_TIMER expires, if recovery is entered, or if the PUT sends any packet.
7. The LVS transmits a U1 Exit LFPS to transition to U0 and waits to receive U1 Exit LFPS to complete the U1 Exit LFPS handshake.
8. The test fails if the LFPS handshake does not conform to the following specifications from section 6.9.2:
 - a. Between 300ns – 900ns elapses between the start of the LVS U1 Exit LFPS and the start of the PUT U1 Exit LFPS.
 - b. The PUT U1 Exit LFPS duration is within 600ns – 900ns.
 - c. The PUT enters Recovery before tNoLFPSResponseTimeout deadline after the start of its U1 exit LFPS.
 - d. The PUT enters U0 before Ux_EXIT_TIMER deadline.
9. The test passes if all packets are successful, recovery is entered once, no extra packets or LFPS signals are received, and the PUT returns to U0.

TD.7.24 Accepted Power Management Transaction for U2 Test (Upstream Port Only)

This test verifies that the PUT transitions to U2 if it receives an LGO_U2.

Covered Assertions

7.2.4.1.1#7,9
 7.2.4.2.1#4
 7.2.4.2.2#2,3
 7.2.4.2.3#2,8,9
 7.2.4.2.7#2, 3
 7.5.8.1#2
 7.5.8.2#5
 8.4.2#1

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS transmits the Set Link Function LMP with the Force_LinkPM_Accept bit asserted.
3. The LVS transmits an LGO_U2 and waits to receive an LAU from the PUT.
4. The test fails if the PUT does not transmit an LAU before PM_LC_TIMER deadline, or if recovery is entered.

5. The LVS transmits an LPMA and then transitions to U2.
6. The test fails if the PUT does not transition to U2 when the PM_ENTRY_TIMER expires, recovery is entered, or if the PUT sends any packet.
7. The LVS transmits the U2 Exit LFPS to transition to U0 and waits to receive U2 Exit LFPS to complete the U2 Exit LFPS handshake.
8. The test fails if the LFPS handshake does not conform to the following specifications from section 6.9.2:
 - a. Between 300ns – 2ms elapses between the start of the LVS U2 Exit LFPS and the start of the PUT U2 Exit LFPS.
 - b. The PUT U2 Exit LFPS duration is within 80us – 2ms.
 - c. The PUT enters Recovery before tNoLFPSResponseTimeout deadline after the start of its U2 exit LFPS.
 - d. The PUT enters U0 before Ux_EXIT_TIMER deadline
9. The test passes if all packets are successful, recovery is entered once, no extra packets or LFPS signals are received, and the PUT enters Recovery.

TD.7.25 Accepted Power Management Transaction for U3 Test (Upstream Port Only)

This test verifies that the PUT transitions to U3 if it receives an LGO_U3.

Covered Assertions

7.2.4.1.1#7,97.2.4.2.1#4

7.2.4.2.4#2,3,7

7.2.4.2.7#2,3

7.5.9.1#3

7.5.9.2#5

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS transmits an LGO_U3 and waits to receive an LAU from PUT.
3. The test fails if the PUT does not transmit an LAU before PM_LC_TIMER deadline, or if recovery is entered..
4. The LVS transmits an LPMA and then transitions to U3.
5. The test fails if the PUT does not transition to U3 when the PM_ENTRY_TIMER expires, if recovery is entered, or if the PUT sends any packet.
6. The LVS transmits the U3 Exit LFPS to transition to U0 and waits to receive U3 Exit LFPS to complete the U3 Exit LFPS handshake.
7. The test fails if the LFPS handshake does not conform to the following specifications from section 6.9.2:
 - a. Between 300ns – 10ms elapses between the start of the LVS U3 Exit LFPS and the start of the PUT U3 Exit LFPS.
 - b. The PUT U3 exit LFPS duration is within 80us – 10ms.
 - c. The PUT enters Recovery before tNoLFPSResponseTimeout deadline after the start of its U3 exit LFPS.

8. The test passes if all packets are successful, recovery is entered once, no extra packets or LFPS signals are received, and the PUT enters Recovery.

TD.7.26 Transition to U0 from Recovery Test

This test verifies that the PUT transitions to U0 when it is in Recovery.

Covered Assertions

- 7.2.4.1.1#3,4,7,9
- 7.3.6#17.5.10.3.1#1
- 7.5.10.3.2#1
- 7.5.10.4.2#1
- 7.5.10.5.1#1
- 7.5.10.5.2#1

Overview of Test Steps

1. Both the LVS and the PUT go through the initial steps of the LTSSM to reach U0.
2. The LVS does not transmit the Header Sequence Advertisement and the Rx Header Buffer Credit Advertisement. The PUT will then transition to Recovery because the PENDING_HP_TIMER will time out.
3. The test fails if the PUT transitions to Recovery before PENDING_HP_TIMER deadline or it does not transition to Recovery when the PENDING_HP_TIMER expires.
4. The test fails if any of the following occur:
 - a. The PUT does not transmit TS1 ordered sets.
 - b. The PUT transmits TS2s before the LVS sends eight consecutive and identical TS1s or TS2s.
 - c. The PUT interrupts a TS1 ordered set to transmit a SKP ordered set (between TS1 ordered sets is OK).
 - d. The PUT transmits Idle Symbols or any other Packet.
 - e. The PUT continues to transmit TS1 ordered sets after tRecoveryActiveTimeout expires.
5. The LVS transmits TS2 ordered sets and readies to complete the Recovery.Configuration handshake.
6. The test fails if any of the following occur:
 - a. The PUT does not transmit at least sixteen consecutive TS2 ordered sets after receiving one TS2 ordered set.
 - b. The PUT sends Idle symbols before the LVS sends at least eight consecutive TS2 ordered sets.
 - c. The PUT interrupts transmission of a TS2 ordered set to transmit a SKP ordered set (between TS2 ordered sets is OK).
 - d. The PUT continues to transmit TS2 ordered sets after tRecoveryConfigurationTimeout expires.
7. The LVS transmits Idle symbols.
8. The test fails if any of the following occur:
 - a. The PUT does not transmit at least sixteen Idle Symbols after the LVS transmits one Idle symbol.

- b. The PUT transmits the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before the LVS transmits 8 Idle symbols.
 - c. The PUT enters recovery after idle symbols have been exchanged.
 - d. Upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before their respective timeouts, PENDING_HP_TIMER and CREDIT_HP_TIMER, expire.
9. The LVS and PUT continue the test with the Link Initialization Sequence starting at step two.

TD.7.27 Hot Reset Detection in Polling Test (Upstream Port Only)

This test verifies that the PUT detects the Hot Reset in Polling.

Covered Assertions

- 7.2.4.1.1#6,8,17,22
- 7.4.2#4
- 7.5.4.7.2#4
- 7.5.12.3.1#1,3,4
- 7.5.12.3.2#1
- 7.5.12.4.1#1
- 7.5.12.4.2#1

Overview of Test Steps

1. Both LVS and PUT detect each other and then transition to Polling.LFPS and Polling.RxEQ.
2. Both LVS and PUT transmit the TS1 ordered sets during Polling.Active.
3. The LVS waits to receive TS2 ordered sets.
4. The test fails if the PUT does not transmit TS1s before tU0RecoveryTimeout expires.
5. The LVS initiates a Hot Reset and transmits TS2 ordered sets with the Reset bit asserted.
6. The test fails if the PUT does not transmit at least sixteen TS2 ordered sets with the Reset bit asserted followed by two consecutive TS2 ordered sets with the Reset bit de-asserted.
7. The LVS transmits four consecutive TS2 ordered sets with the Reset bit de-asserted, and then transmits Idle Symbols.
8. The test fails if any of the following occur:
 - a. The PUT does not transmit at least sixteen Idle Symbols after the LVS transmits one Idle symbol.
 - b. The PUT transmits the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before the LVS transmits 8 Idle symbols.
 - c. The PUT enters recovery after idle symbols have been exchanged.
 - d. Upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before their respective timeouts, PENDING_HP_TIMER and CREDIT_HP_TIMER, expire.
9. The LVS and PUT exchange Port Configuration transactions.

10. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
11. The test fails if the Port Configuration exchange sequences are not successful or the link does not stay in U0 for at least 50ms.

TD.7.28 Hot Reset Detection in U0 Test (Upstream Port Only)

This test verifies that the PUT detects the Hot Reset in U0 and does not start the Port Configuration Sequences.

Covered Assertions

- 7.2.4.1.1#6,8,17,22
- 7.4.2#2,4
- 7.5.10.4.1#1
- 7.5.12.3.1#1,2
- 7.5.12.3.2#1
- 7.5.12.4.1#1
- 7.5.12.4.2#1

Overview of Test Steps

1. Do steps 1 to 5 of the Link Initialization Sequence.
2. The LVS transmits TS1 ordered set to transition to Recovery.
3. The LVS waits to receive TS1 ordered sets.
4. The test fails if the PUT does not transmit TS1s before tU0RecoveryTimeout expires.
5. The LVS initiates a Hot Reset by transmitting TS2 ordered sets with the Reset bit asserted.
6. The test fails if the PUT does not transmit at least sixteen TS2 ordered sets with the Reset bit asserted followed by two consecutive TS2 ordered sets with the Reset bit de-asserted.
7. The LVS transmits four consecutive TS2 ordered sets with the Reset bit de-asserted, and then transmits Idle Symbols.
8. The test fails if any of the following occur:
 - a. The PUT does not transmit at least sixteen Idle Symbols after the LVS transmits one Idle symbol.
 - b. The PUT transmits the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before the LVS transmits 8 Idle symbols.
 - c. The PUT enters recovery after idle symbols have been exchanged.
 - d. Upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before their respective timeouts, PENDING_HP_TIMER and CREDIT_HP_TIMER, expire.
9. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
10. The test fails if the PUT retransmits Port Capability or Port Configuration LMPs.
11. The test fails if the Port Configuration exchange sequences are not successful and the link does not stay in U0 for at least 50ms.

TD.7.29 Hot Reset Initiation in U0 Test (Downstream Port Only)

This test verifies that the PUT initiates Hot Reset in U0.

Covered Assertions

7.2.4.1.1#6,8,17,22

7.4.2#2,4,10

7.5.4.6.1#1

7.5.4.7.2#3

7.5.10.4.1#1

7.5.12.3.1#1,2

7.5.12.3.2#1

7.5.12.4.1#1

7.5.12.4.2#1

Overview of Test Steps

1. Do steps 1 to 5 of the Link Initialization Sequence.
2. The LVS prompts the test operator to initiate a Hot Reset on the PUT through USB30CV.
3. The LVS waits for the PUT to send TS1s.
4. The test fails if the PUT does not transmit TS1s before tU0RecoveryTimeout expires.
5. The LVS transmits TS1 ordered sets and waits to receive TS2 ordered sets with the Reset bit asserted.
6. The test fails if the PUT does not transmit at least sixteen TS2 ordered sets with Reset bit asserted.
7. The LVS transmits at least sixteen TS2 ordered sets with the Reset bit asserted, and then transmits two consecutive TS2 ordered sets with the Reset bit de-asserted.
8. The test fails if any of the following occur:
 - a. After LVS transmitted TS2 ordered sets with Reset bit de-asserted, the PUT does not transmit four consecutive TS2 ordered sets with the Reset bit de-asserted, when tHotResetActiveTimeout expires
 - b. The PUT transmits anything other than TS2 ordered sets, before the LVS transmits TS2 ordered sets with the Reset bit de-asserted.
9. The LVS transmits Idle Symbols.
10. The test fails if any of the following occur:
 - a. The PUT does not transmit at least sixteen Idle Symbols after the LVS transmits one Idle symbol.
 - b. The PUT transmits the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before the LVS transmits 8 Idle symbols.
 - c. The PUT enters recovery after idle symbols have been exchanged.
 - d. Upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before their respective timeouts, PENDING_HP_TIMER and CREDIT_HP_TIMER, expire.
11. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.

12. The test fails if the PUT retransmits Port Capability or Port Configuration LMPs.
13. The test fails if the Port Configuration exchange sequences are not successful and the link does not stay in U0 for at least 50ms.

TD.7.30 Recovery on three consecutive failed RX Header Packets Test

This test verifies that the PUT will enter Recovery if it fails to receive a header packet three consecutive times.

Covered Assertions

- 7.2.4.1.1#7,9
- 7.2.4.1.4#5
- 7.5.10.3.1#1
- 7.5.10.3.2#1
- 7.5.10.4.2#1
- 7.5.10.5.1#1
- 7.5.10.5.2#1

Overview of Test Steps

1. Do steps 1 to 3 of the Link Initialization Sequence.
2. The LVS and the PUT will exchange Port Configuration transactions, but the first packet sent by the LVS will have an invalid CRC-5.
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP with an invalid CRC-5.
 - d. LVS verifies that the PUT replies with an LBAD.
 - e. LVS transmits an LRTY and then retransmits the packet with an invalid CRC-5.
 - f. LVS verifies that the PUT replies with an LBAD.
 - g. LVS transmits an LRTY and then retransmits the packet with an invalid CRC-5.
 - h. LVS verifies that the PUT initiates Recovery.
3. The test fails if any of the following occur:
 - a. The PUT does not reply with LBAD to the first two packets (which have invalid CRC-5s)
 - b. The PUT does not initiate Recovery in step g within tLinkTurnAround.
 - c. The PUT initiates Recovery before the third invalid packet is received.
4. The LVS and PUT transition through Recovery to U0.
5. The LVS and the PUT perform the Link Initialization Sequence and exchange all remaining Port Configuration transactions.
6. The test fails if the PUT retransmits its Port Capability LMP.
7. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.

8. The test passes if the exchanges are successful, no timeout is detected, recovery is entered once, all packets are successfully received by the PUT except for the packet with invalid CRC-5, all credits are restored and the link stays in U0 for at least 50ms.

TD.7.31 Hot Reset Failure Test (Downstream Port Only)

This test verifies that the PUT initiates a Warm Reset when Hot Reset training fails. NOTE: This test is not aligned with USB 3.0 Specification but it is anticipated that the issue will be resolved in favor of the test implementation in an Errata.

Covered Assertions

- 7.4.2#6,8,14
- 7.5.3.3.1#1
- 7.5.10.3.2#5
- 10.3.1.6#6

Overview of Test Steps

1. Perform the Link Initialization Sequence to bring the LVS and PUT link to U0.
2. The LVS software prompts the test operator to initiate a Hot Reset on the PUT through USB30CV.
3. The LVS waits for the PUT to send TS1s.
4. The test fails if the PUT does not transmit TS1s before tU0RecoveryTimeout expires.
5. The LVS does not transmit anything in response to the PUT.
6. The test fails if the PUT does not transmit a Warm Reset LFPS after tHotResetActiveTimeout expires.
7. The LVS responds to the Warm Reset LFPS by entering Rx.Detect.
8. The LVS and PUT perform the Link Initialization Sequence to bring the link to U0.
9. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
10. The test passes if the exchanges are successful, the PUT initiates a Warm Reset LFPS after tRecoveryActiveTimeout in Recovery.Active and the link reaches U0 with a correct Port Configuration Transaction and stays there for at least 50ms.

TD.7.32 Warm Reset Rx.Detect Timeout Test (Hub Downstream Port Only)

This test verifies that a hub port transitions to DSPORT.Disconnected when a Warm Reset is initiated and no far end terminations are found.

Covered Assertions

- 10.3.1.6#7

Overview of Test Steps

1. Perform the Link Initialization Sequence to bring the LVS and PUT link to U0.
2. The LVS software prompts the test operator to initiate a Warm Reset on the hub PUT through USB30CV.
3. The LVS waits for the PUT to send a Warm Reset LFPS.

4. The test fails if PUT does not transmit a Warm Reset by the time the test operator presses “OK” on the prompt.
5. The LVS removes terminations and starts a timer when it sees a Warm Reset LFPS by the PUT. The LVS does not present terminations.
6. After the timer reaches max tTimeForResetError time, the LVS software prompts the test operator to check the state of the PUT through USB30CV. The prompt asks “Is the port in DSPORT.Disconnected” with YES and NO options available.
7. The test passes if the exchanges are successful and the test operator determines that the PUT was in DSPORT.Disconnected.

TD.7.33 Exit Compliance Mode Test (Upstream Port Only)

This test verifies that a device exits Compliance Mode when it receives a Warm Reset LFPS.

Covered Assertions

7.4.2#9

7.5.4.3.2#1

7.5.5.1#2

7.5.5.2#2

Overview of Test Steps

1. The LVS makes sure VBUS is off to assure a PowerOn Reset.
2. The LVS prompts the test operator to power cycle a self-powered device.
3. The LVS turns on VBUS, bringing the link to Rx.Detect.
4. The LVS presents Terminations and waits for the PUT to present Terminations.
5. When the LVS detects Terminations from the PUT, the LVS starts a timer for tPollingLFPSTimeout and does not transmit an LFPS.
6. When the timer expires, the LVS verifies that the device is in Compliance Mode by sending Ping.LFPS until it can verify that the LVS is receiving a Compliance Pattern, (at most by the COMs in the 4th Compliance Pattern).
7. The test fails if the LVS cannot verify a Compliance Pattern coming from the PUT.
8. The LVS transmits a Reset.LFPS and enters Rx.Detect.
9. The LVS and PUT perform the Link Initialization Sequence to bring the LVS and PUT link to U0.
10. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
11. The test passes if all exchanges are successful and the PUT stays in U0 for 50ms.

TD.7.34 Exit Compliance Mode Test (Downstream Port Only)

This test verifies that a downstream port instructed to Reset while in Compliance Mode initiates a Warm Reset.

Covered Assertions

- 7.4.2#9
- 7.5.4.3.2#2
- 7.5.5.1#2
- 7.5.5.2#1

Overview of Test Steps

1. The LVS prompts the test operator to power cycle the PUT computer to toggle VBUS.
2. The LVS waits for VBUS and Terminations from the PUT.
3. When the LVS detects VBUS and Terminations from the PUT, the LVS starts a timer for tPollingLFPSTimeout and does not transmit an LFPS.
4. When the timer expires, the LVS verifies that the device is in Compliance Mode by sending Ping.LFPS until it can verify that the LVS is receiving a Compliance Pattern, (at most by the COMs in the 4th Compliance Pattern).
5. The test fails if the LVS cannot verify a Compliance Pattern coming from the PUT.
6. The LVS prompts the test operator to Reset the PUT through USB30CV and then hit “OK”.
7. The LVS waits to receive a Warm Reset LFPS from PUT.
8. The test fails if the LVS does not receive a Warm Reset LFPS before the test operator hits “OK”
9. The LVS closes the prompt automatically when it receives a Warm Reset LFPS.
10. The LVS transitions to Rx.Detect.Reset for the duration of the Warm Reset LFPS.
11. The LVS transitions to Rx.Detect and the LVS and PUT transition through Polling to U0.
12. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
13. The test passes after the Port Configuration exchange is successful and the link stays in U0 for 50ms.

TD.7.35 Exit U3 by Reset Test (Downstream Port Only)

This test verifies that a downstream port instructed to Reset during U3 initiates a Warm Reset.

Covered Assertions

- 7.2.4.2.4#1,4,5
- 7.5.9.2#2

Overview of Test Steps

1. Perform the Link Initialization Sequence to bring the LVS and PUT link to U0.
2. The LVS software prompts the test operator to Suspend the PUT to U3 through USB30CV.
3. The LVS waits to receive an LGO_U3 from the PUT.
4. The LVS sends an LAU when it receives an LGO_U3 from the PUT.
5. The LVS waits to receive an LPMA from the PUT.
6. The test fails if any of the following occur:
 - a. The LVS does not receive an LGO_U3

- b. The LVS does not receive an LPMA before PM_ENTRY_TIMER deadline.
 - c. The PUT fails to transition to U3 after PM_ENTRY_TIMER expires.
7. The LVS prompts the test operator to Reset the PUT through USB30CV and then hit “OK” on the prompt.
 8. The LVS waits to receive a Warm Reset LFPS from PUT.
 9. The test fails if no Warm Reset LFPS is received by the LVS before the test operator hits “OK”.
 10. When the LVS receives a Warm Reset LFPS the prompt is closed automatically.
 11. The LVS transitions to Rx.Detect.Reset for the duration of the Warm Reset LFPS.
 12. The LVS transitions to Rx.Detect and the LVS and PUT transition through Polling to U0.
 13. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
 14. The test passes after the Port Configuration exchange is successful and the link stays in U0 for 50ms.

TD.7.36 Exit U3 Test (Host Downstream Port Only)

This test verifies that a downstream port initiates U3 exit with a U3 exit LFPS.

Note: This test is performed on host silicon only. This test is not performed on end products. The operator must install the Product-Specific host controller driver to perform this test. It cannot be tested with the Compliance driver. The LVS is configured to appear to the host controller as a device.

The tested conditions are:

- A. LVS responds to the first U3 Exit LFPS from host downstream port 5ms after detecting
- B. LVS responds to the second U3 Exit LFPS from host downstream port 5ms after detecting. No response is made to the first one.
- C. LVS responds to the third U3 Exit LFPS from host downstream port 5ms after detecting. No response is made to the first two.
- D. LVS responds to fourth U3 Exit LFPS from host downstream port 30ms after detecting. No response is made to the first three.

Covered Assertions

7.2.4.2.4#1,4,5

7.2.4.2.7#1

7.5.9.1#4

7.5.9.2#5

Overview of Test Steps

1. Perform the Link Initialization Sequence to bring the LVS and PUT link to U0. The PUT host controller machine enumerates the LVS.
2. The LVS software prompts the test operator to put the PUT host controller machine to sleep.
3. The LVS waits to receive an LGO_U3 from the PUT.
4. The LVS sends an LAU when it receives an LGO_U3 from the PUT.
5. The LVS waits to receive an LPMA from the PUT.
6. The test fails if any of the following occur:

- a. The LVS does not receive an LGO_U3
 - b. The LVS does not receive an LPMA before PM_ENTRY_TIMER deadline.
7. The LVS prompts the test operator to verify that the host controller machine is in a sleep state.
 8. The LVS prompts the test operator to wake the host controller machine.
 9. The LVS waits to receive a U3 Exit LFPS from PUT.
 10. The test fails if no U3 Exit LFPS is received.
 11. The LVS sends a U3 Exit LFPS complying with first condition listed above.
 12. The test fails if duration of tU3WakeupRetryDelay deadline is not observed between unsuccessful LFPS handshake.
 13. The LVS and PUT transition through Recovery to U0.
 14. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
 15. The test passes after the Port Configuration exchange is successful and the link stays in U0 for 50ms.
 16. Repeat the steps using each of the other conditions listed above.

TD.7.37 Packet Pending Test (Upstream Port Only)

This test verifies that the PUT releases its Packet Pending flag at the end of a Control Transfer.

Covered Assertions

8.6#1

Overview of Test Steps

1. Perform the Link Initialization Sequence to bring the LVS and PUT link to U0.
2. The LVS software issues a GetDescriptor request SETUP packet, with the PP bit set to 1.
3. After receiving LGOOD and LCRD for the SETUP packet, the LVS issues an LGO_U1.
4. The test fails if the PUT does not respond with LXU, or sends any packet before LXU.
5. The LVS sends an ACK TP to start the IN stage of the GetDescriptor request.
6. The LVS waits to receive IN data from the PUT.
7. The LVS software issues a GetDescriptor STATUS packet, with a PP bit set to 0.
8. The LVS waits to receive ACK TP from the PUT, concluding the GetDescriptor request.
9. The test fails if the GetDescriptor request is not completed.
10. The LVS sends an LGO_U1 and waits to receive LAU from the PUT.
11. The test fails if the PUT does not send an LAU.
12. The LVS transmits an LPMA and then transitions to U1.
13. The test fails if the PUT does not transition to U1, or if the PUT sends any packet.