



Larry Taylor

System Architect

Staccato Communications

Allan Bjerke

Sr. Hardware Engineer

Intel Corporation

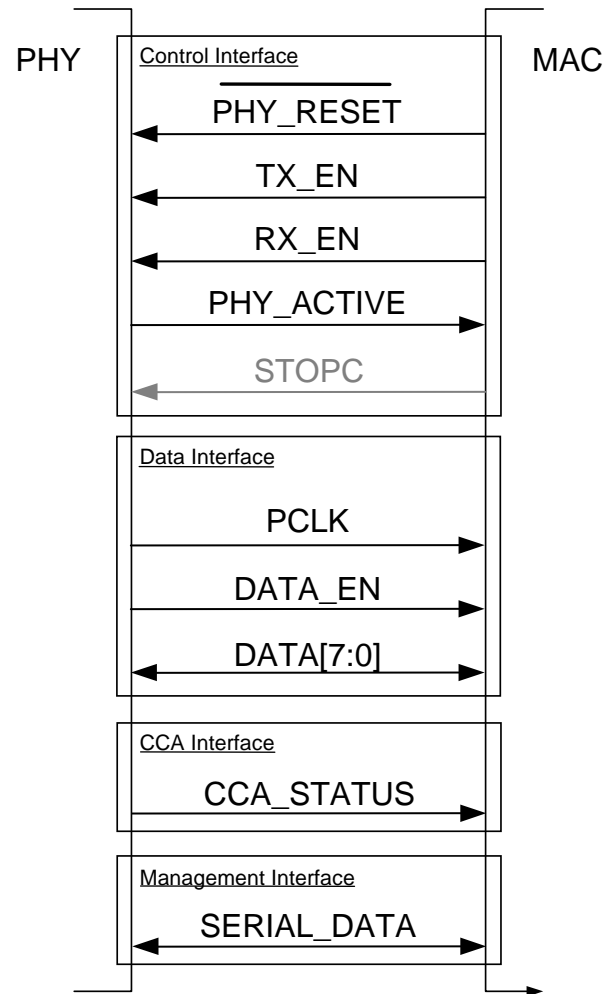


MAC-PHY Interface

- Simple State Machine Model
- Synchronous Interface
- Minimum Number of Signal Lines
- Sleep & Active States
- Flexible Expression of Frame Exchange and IFS Control

Interface Signals

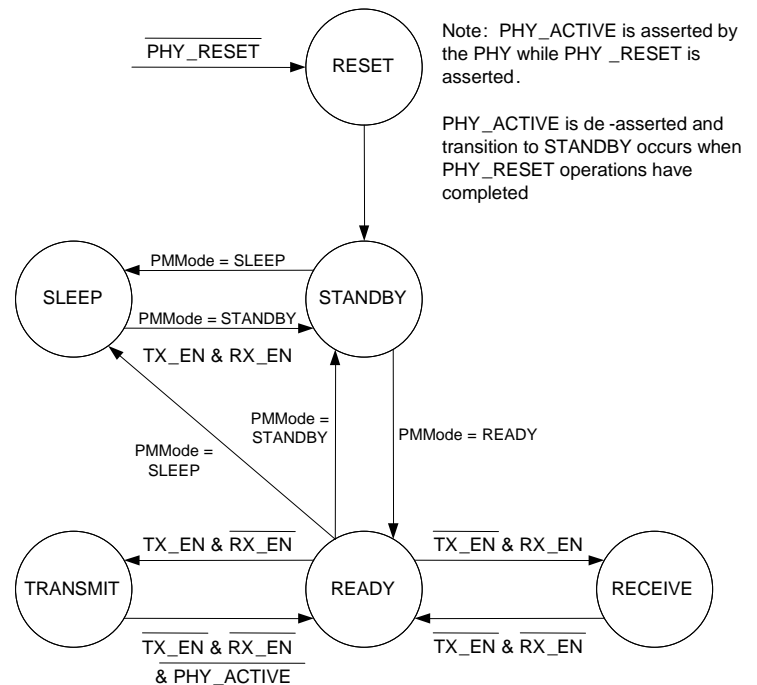
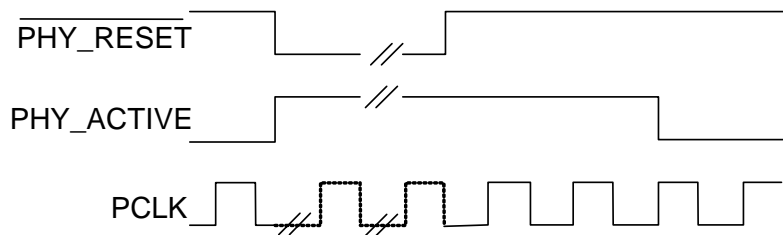
- Four Signal Groups
 - Control Interface
 - Data Interface
 - CCA Interface
 - Management Interface



PHY Reset

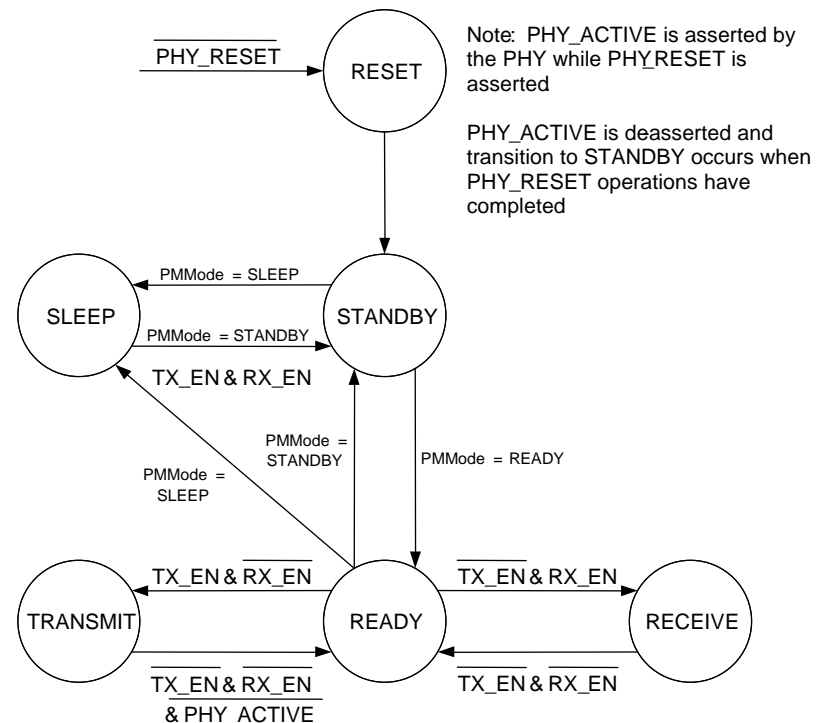
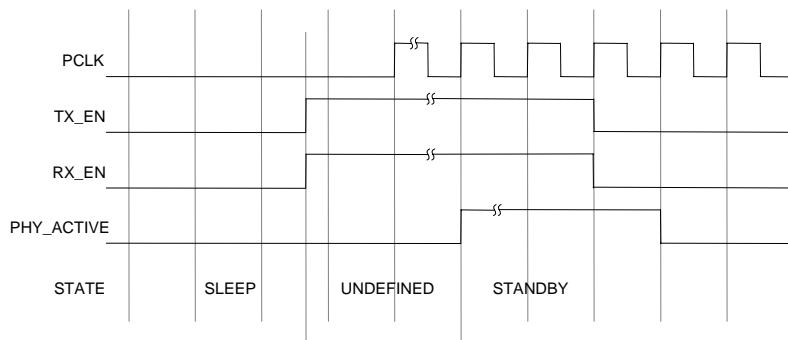


- PHY can be reset at any time and from any state
- $\overline{\text{PHY_RESET}}$ asserted for PHY specific duration
- PHY_ACTIVE asserted by PHY
- PCLK may be off or undefined
- PHY_ACTIVE de-asserted to signal stable PCLK and STANDBY state
- Check RDY register in CONTROL



Exit From Sleep

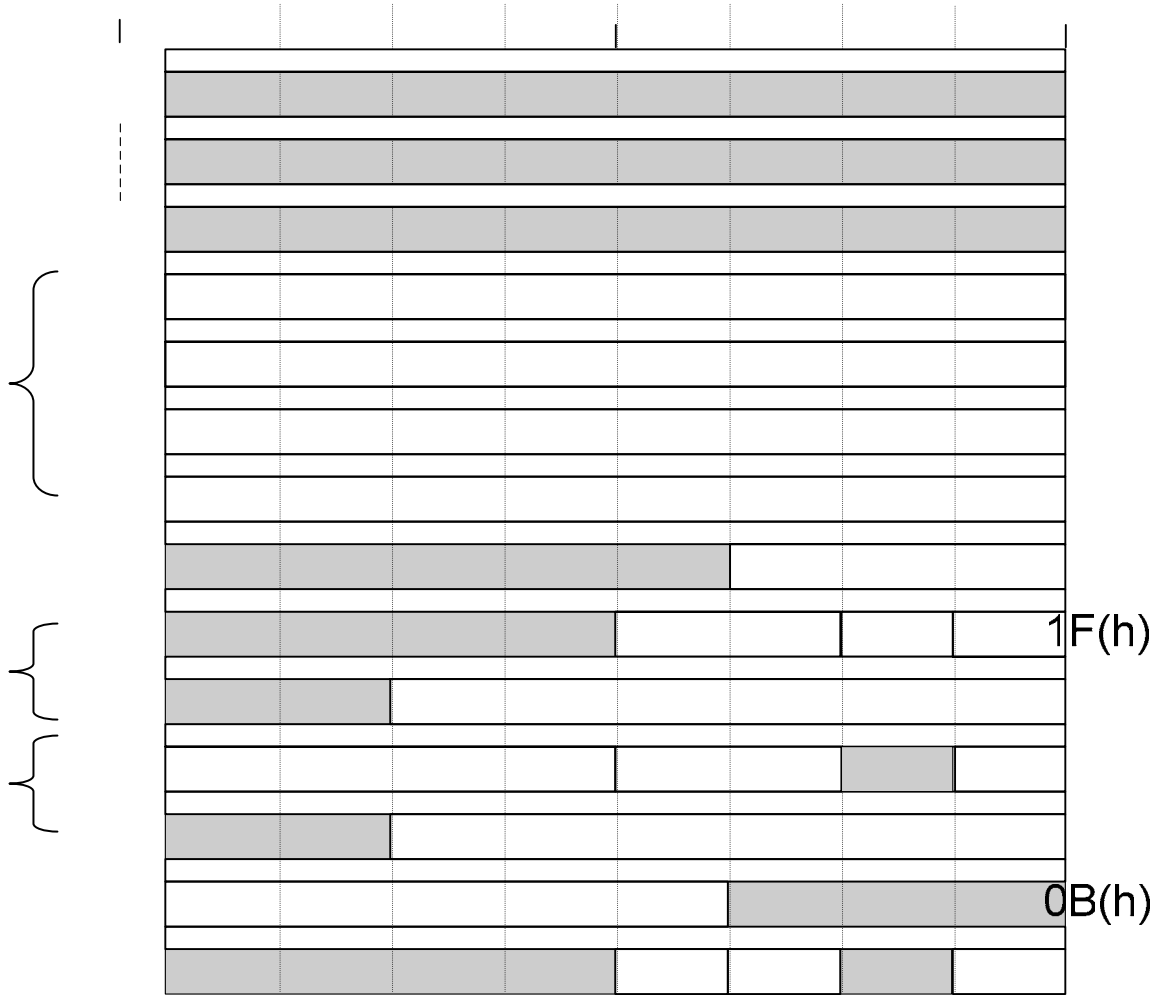
- PCLK is off
- Wake action via TX_EN & RX_EN
- PHY_ACTIVE asserted when in STANDBY state
- MAC Handshake Completion by de-asserting TX_EN & RX_EN



Register Set

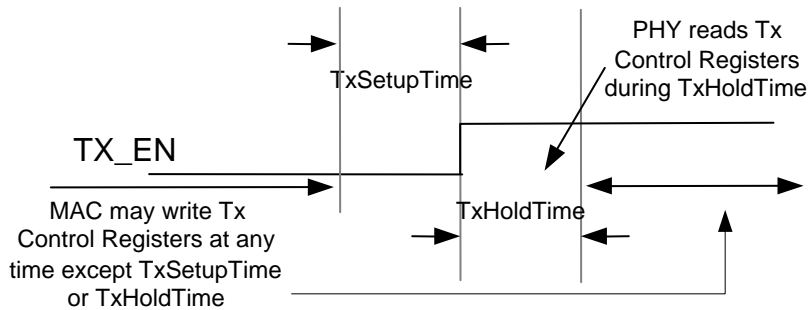


- Ranging Timer
- PHY State
- Receive Control
- Transmit Control
- Regulatory
- Control

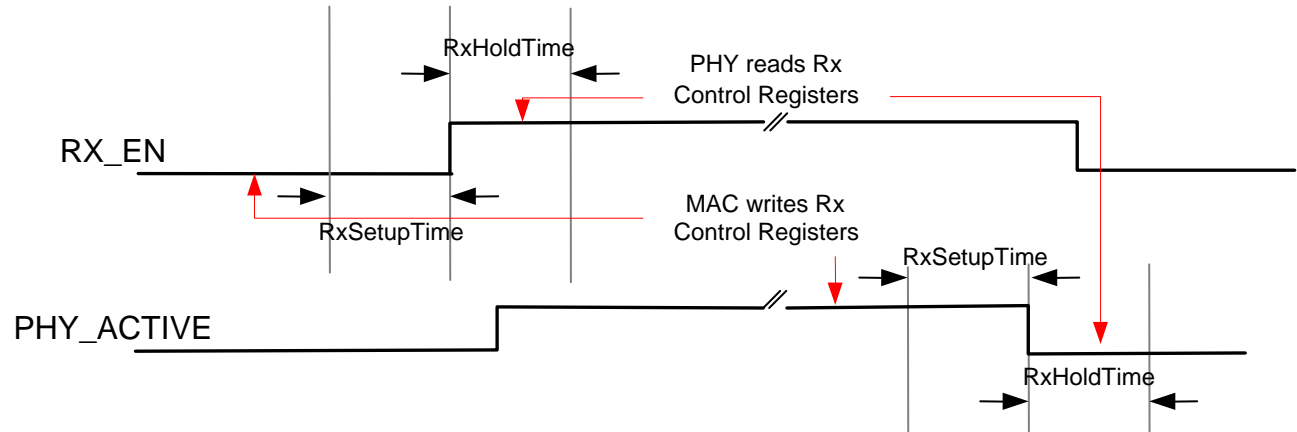


Register Access Timing

- Transmit



- Receive



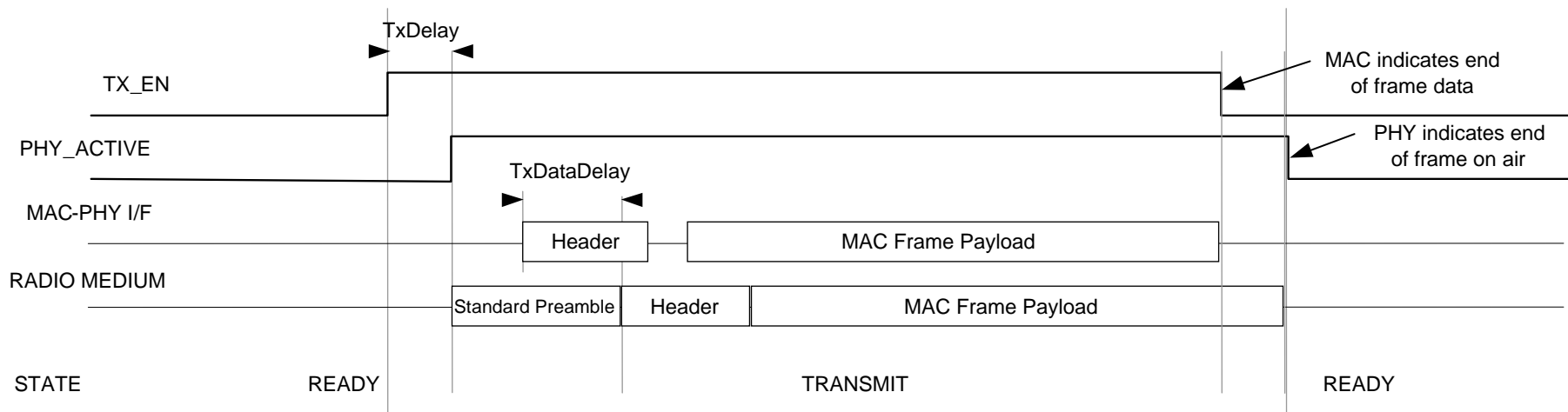


Theory of Operation

- TX_EN, RX_EN & PHY_ACTIVE encode all interface semantics
- All signals are synchronous to rising edge of PCLK
- DATA[7:0] is qualified by DATA_EN
- PHY_ACTIVE provides accurate on-air beginning of frame and end of frame timing from PHY to MAC
 - Tx and Rx offsets to compensate for PHY processing delays
- No 'handshake' between PHY and MAC to indicate when status bytes are being passed
 - MAC counts bytes to determine when the status bytes have arrived (mostly)

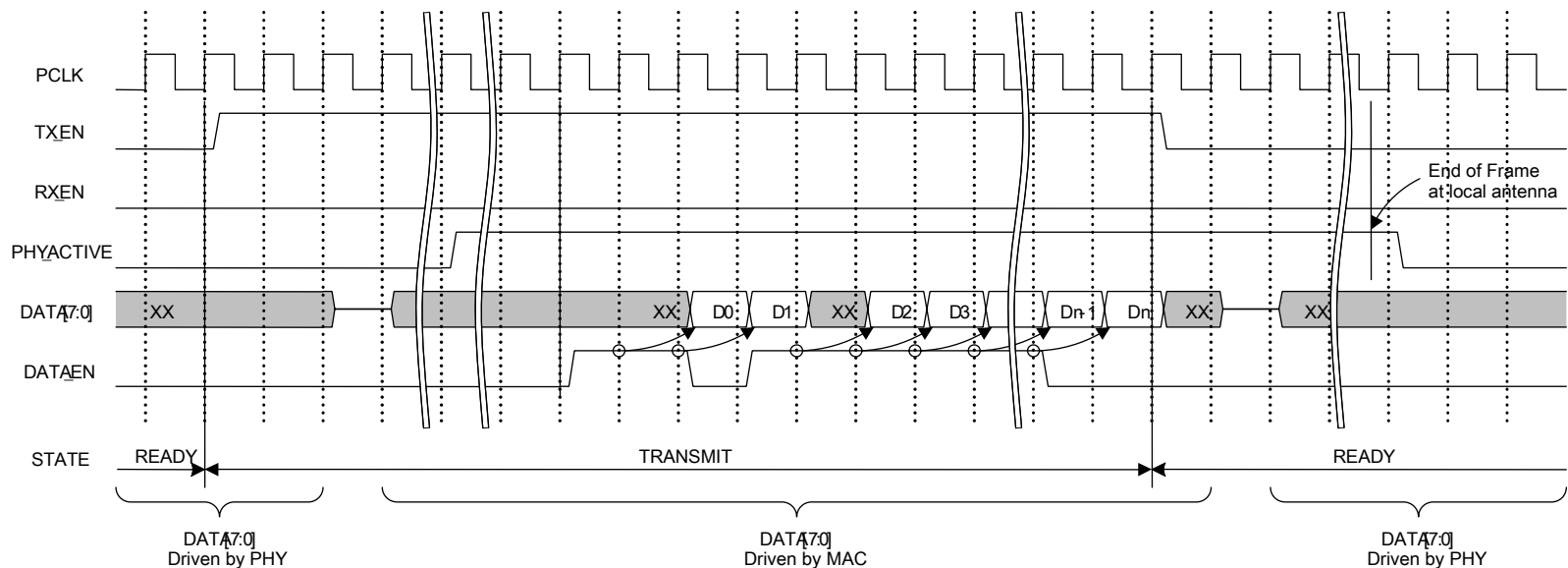
Transmit Delay Intervals

- TxDelay transmit delay path constant
- TxDataDelay for extra MAC processing time
- Explicit end of frame timing



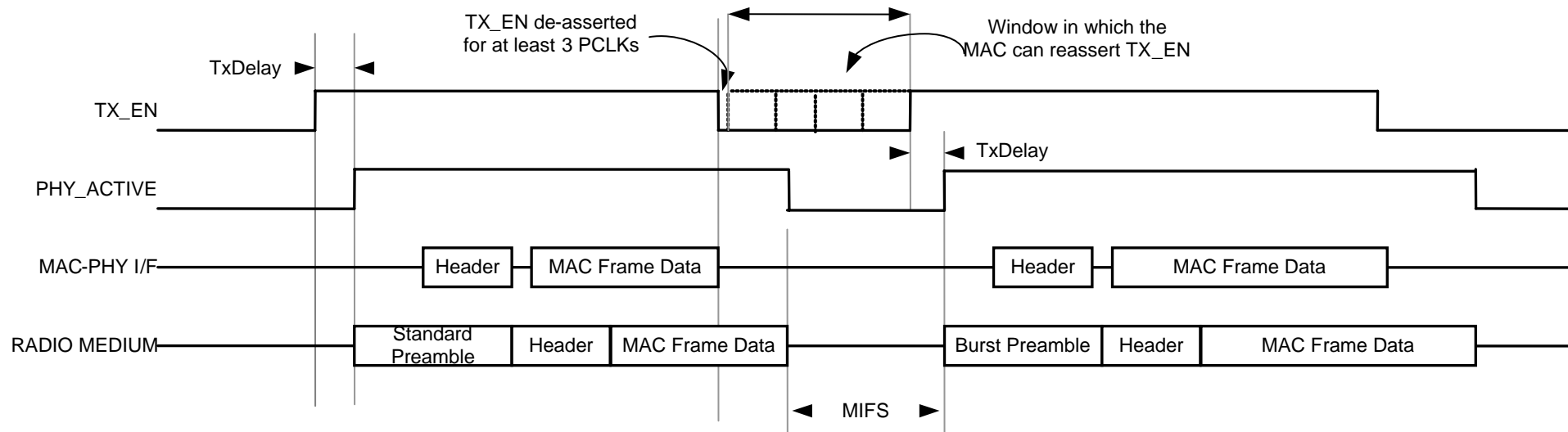
Single Frame Transmit

- TX_EN assertion + TxDelay defines start of frame on air
- Explicit end of frame timing
- TX_EN de-assertion signals end of MAC data



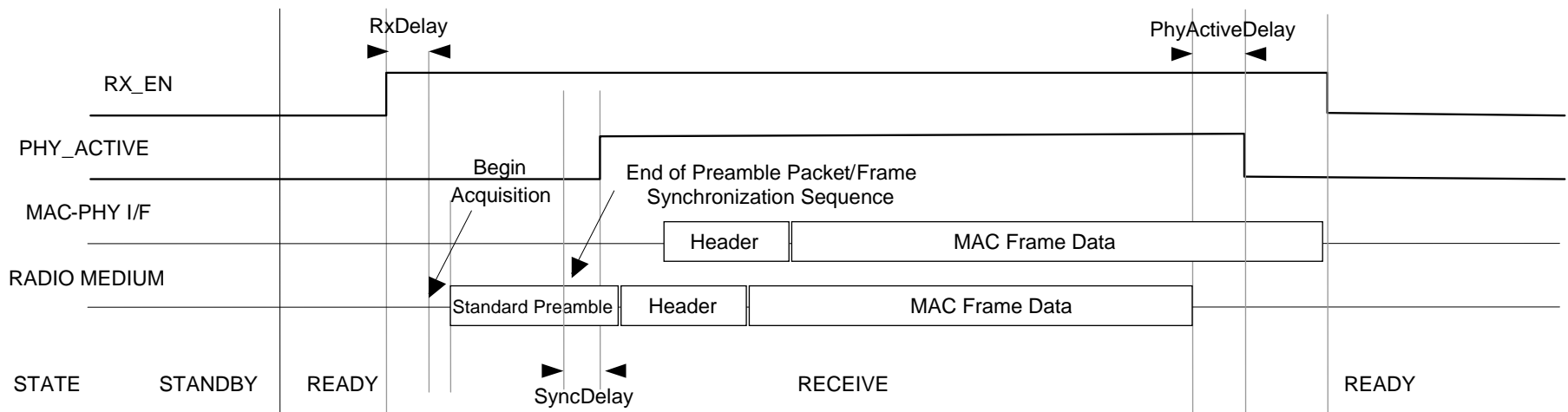
Burst Mode Transmit

- TX_EN re-assertion at least TxDelay before MIFS expires
- Minimum 3 PCLK cycles off time
- PHY enforced 6 symbol IFS



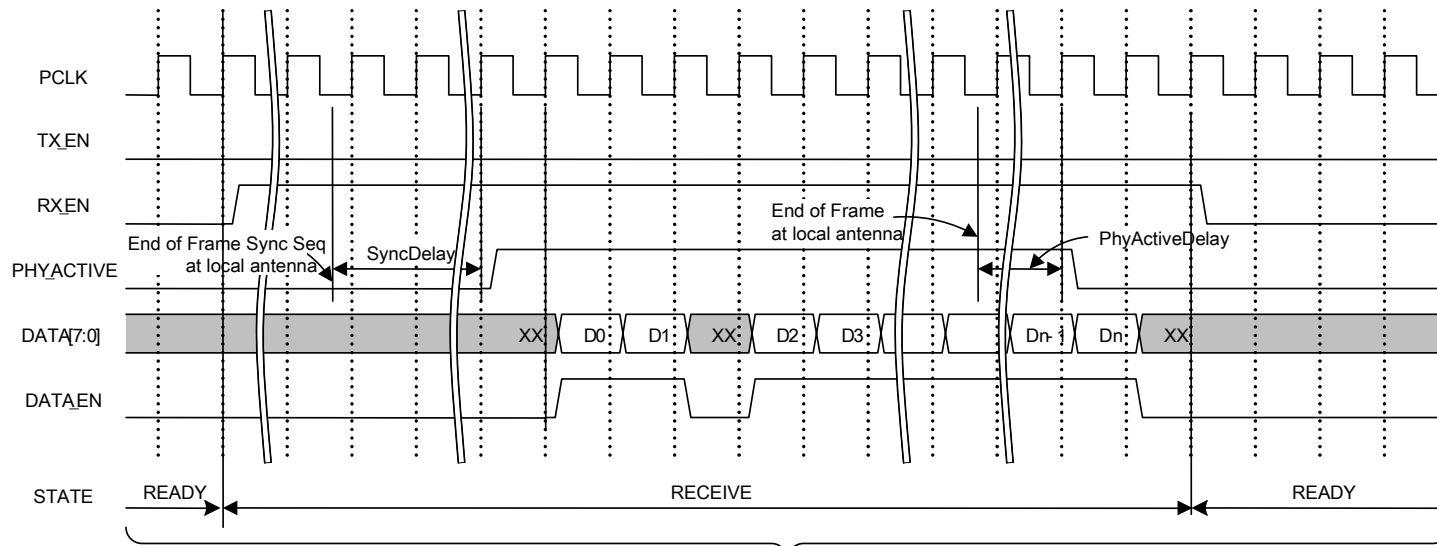
Receive Delay Intervals

- RxDelay receive path delay constant
- PHY_ACTIVE assertion provides Rx Timestamp
 - SyncDelay receive timing reference
- PHY_ACTIVE de-assertion provides end of frame timing
 - PhyActiveDelay decode path constant



Single Frame Receive

- RxDelay receive path delay constant
- PHY_ACTIVE assertion provides Rx Timestamp
 - SyncDelay receive timing reference
- PHY_ACTIVE de-assertion provides end of frame timing
 - PhyActiveDelay decode path constant

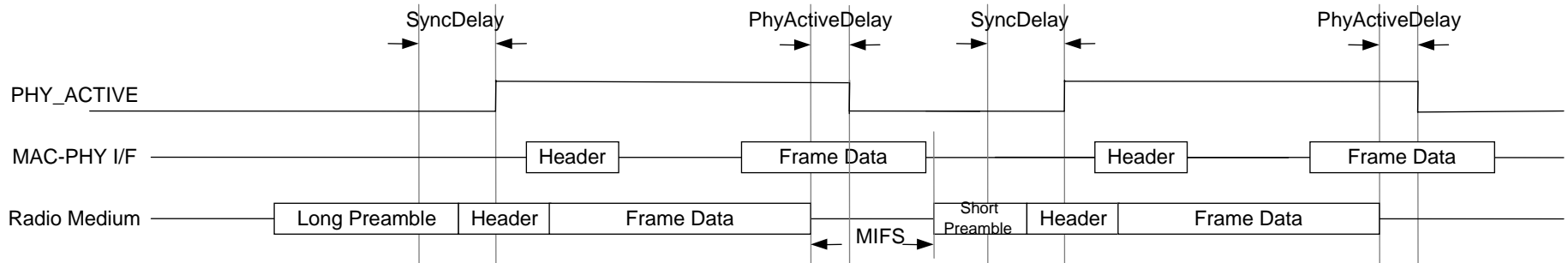


Note SyncDelay & PHYActiveDelay wrt PHY timing

DATA[7:0]
Driven by PHY

Burst Mode Receive

- RX_EN maintained asserted during Burst Mode Receive
- PLCP Header signals subsequent frame preamble and burst continuation
- Usual start and end of frame timing via PHY_ACTIVE, SyncDelay and PHYActiveDelay



Preamble Control

- PT & BM

- PT & BM in PLCP Header
- Burst Mode only
- Long or short preamble

- PTON

- Receive override PT processing

Previous Burst or Single Frame Transmission

Frame (m-1)	BM=0	PT=0	
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Burst Transmission

Frame (m)	BM=1	PT=0 or PT=1	
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Frame (m+1)	BM=1	PT=0 or PT=1	
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Frame (n-1)	BM=1	PT=0 or PT=1	
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Frame (n)	BM=0	PT=0	
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Next Burst or Single Frame Transmission

Frame (n+1)	xx	xx	
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Zero Length Frame Rx

- PHYActiveDelay allows accurate end-of-frame-on-air timing
- Frame status bytes follow header status byte on data lines
 - Flow-controlled by DATA_EN
 - MAC knows to expect them because length was zero

