



WiMedia MAC/PHY Interface

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MAC-PHY Interface

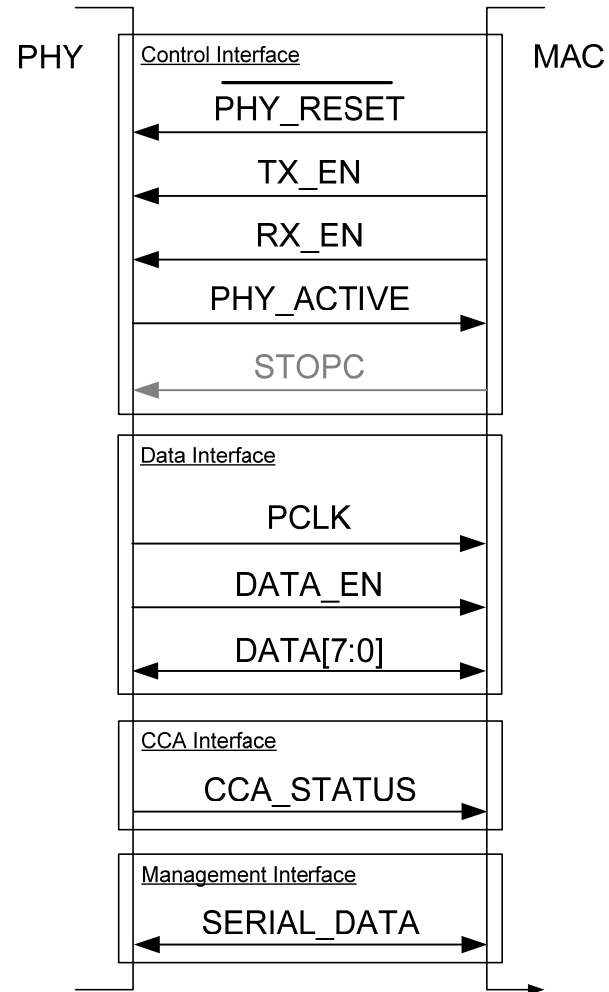


- Motivation
 - Focused industry development
 - Easier prototyping
 - Discrete and macrocell implementations
- Key features
 - MAC controls timing; Simple PHY model
 - Synchronous Interface
 - Minimum Number of Signal Lines
 - Simple State Machine
 - Sleep & Active States

Interface Signals



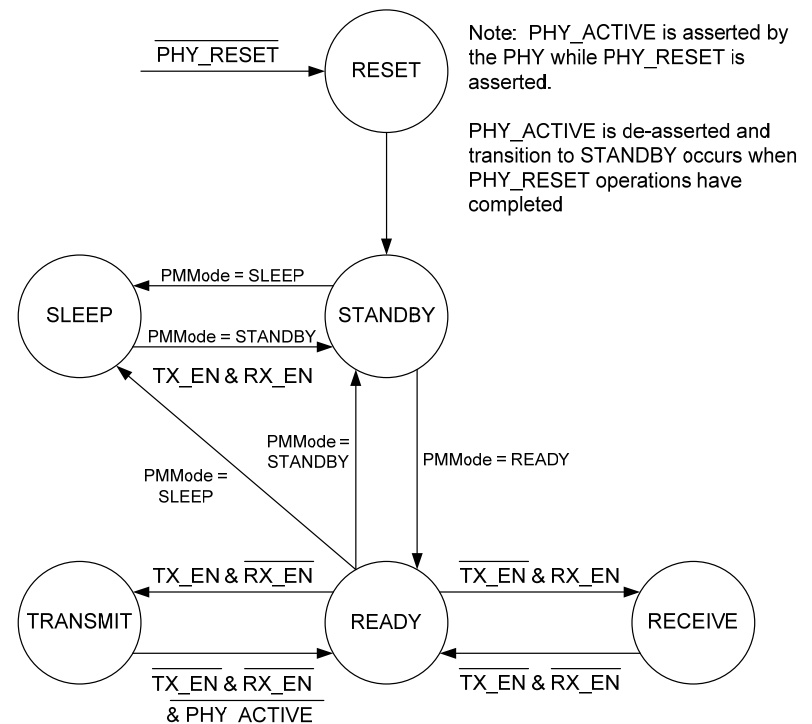
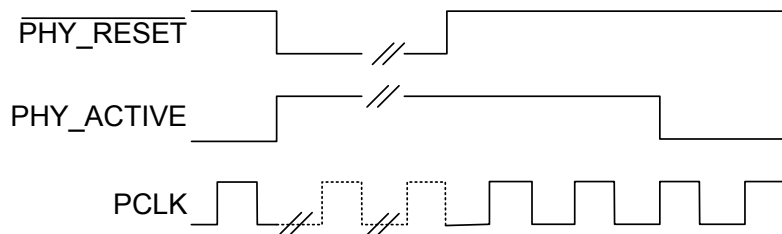
- Four Signal Groups
 - Control Interface
 - Data Interface
 - CCA Interface
 - Management Interface



PHY Reset



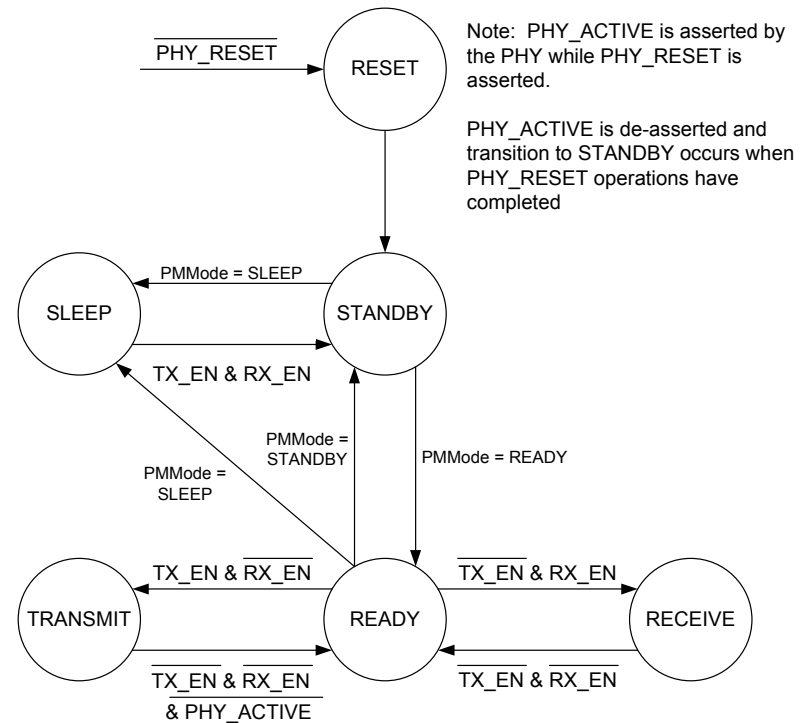
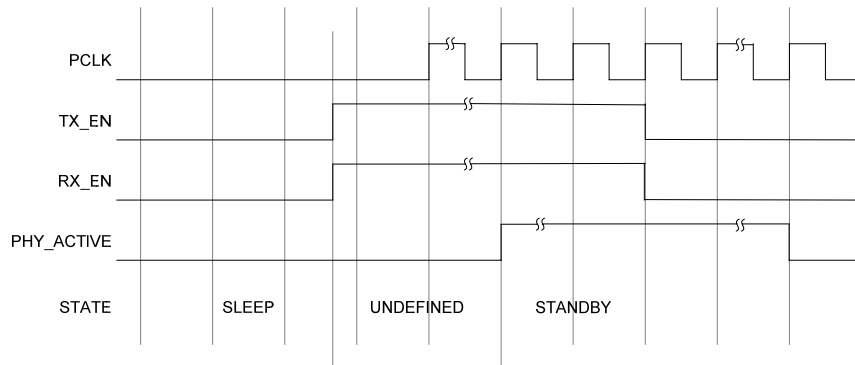
- PHY can be reset at any time and from any state
- MAC asserts $\overline{\text{PHY_RESET}}$ for PHY specific duration
- PHY_ACTIVE asserted by PHY
- PCLK may be off or undefined
- PHY de-asserts PHY_ACTIVE to signal stable PCLK and STANDBY state
- MAC Checks RDY bit in CONTROL reg



Exit From Sleep



- PCLK is off
- Wake action via TX_EN & RX_EN
- PHY_ACTIVE asserted when in STANDBY state
- MAC Handshake Completion by de-asserting TX_EN & RX_EN

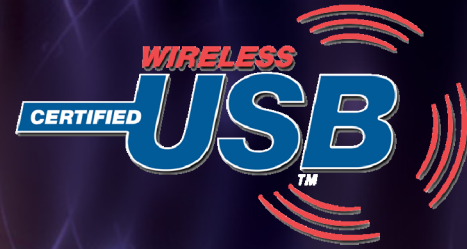


PHY Registers



- Dynamic Registers
 - Used primarily by MAC to control PHY operation
 - Must be implemented by PHY
- Static Registers
 - Define static PHY parameters that PHYs must specify
 - May be implemented on PHY chip, or can be part of datasheet

Dynamic Register Set



Regulatory Extension

Ranging Timer

PHY State

Receive Control

Transmit Control

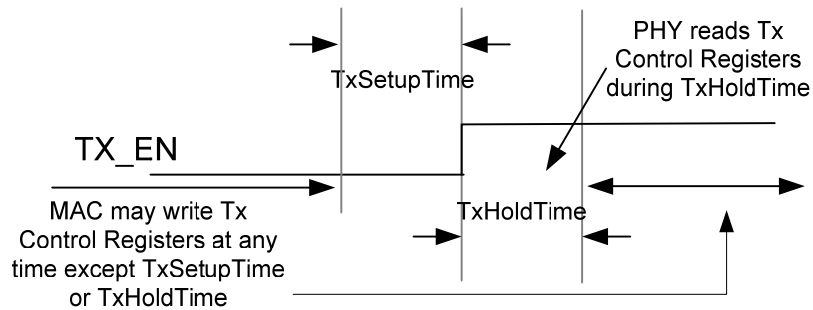
Regulatory Control

	bit-7	bit-4	bit-3	bit-0
1F(h)	Reserved			
0C(h)	Reserved			
0B(h)	CRDEExtension			
0A(h)	Reserved			
09(h)	RANGINGTIMER			
08(h)	RANGINGTIMER [31:24]			
07(h)	RANGINGTIMER			
06(h)	RANGINGTIMER [23:16]			
05(h)	RANGINGTIMER			
04(h)	RANGINGTIMER [15:8]			
03(h)	RANGINGTIMER			
02(h)	RANGINGTIMER [7:0]			
01(h)	PM			
00(h)	Reserved			PMMODE
	RXCTL			
05(h)	Reserved		RXANT	PTON RXPT
04(h)	RXCHAN			
03(h)	Reserved		RXCH	
02(h)	TXCTL			
01(h)	TXPWR		TXANT	Reserved TXPT
00(h)	TXCHAN			
	Reserved		TXCH	
	CRD			
01(h)	CRD			Reserved
00(h)	CONTROL			
	Reserved	CCRE	RNGEN	Reserved RDY

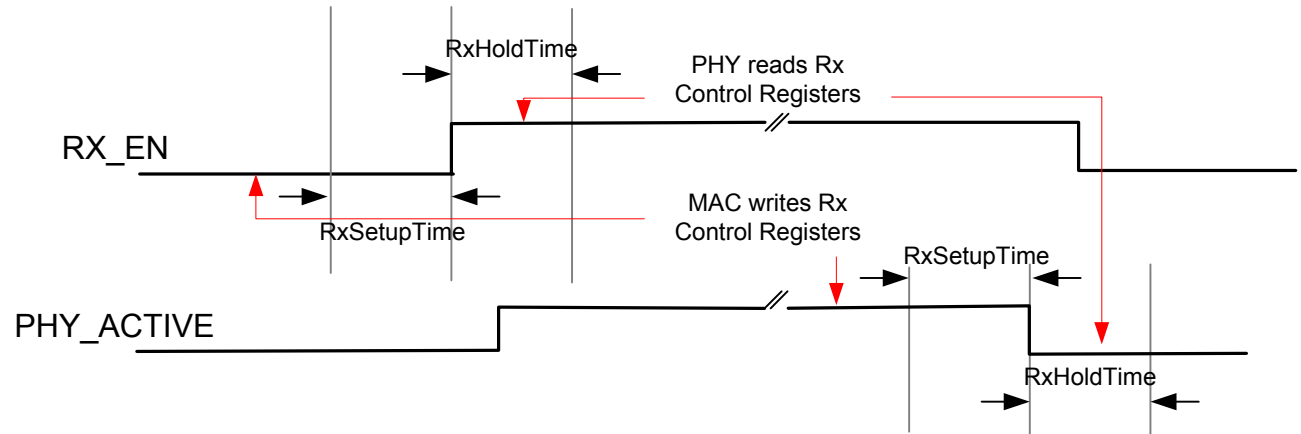
Register Access Timing



- Transmit



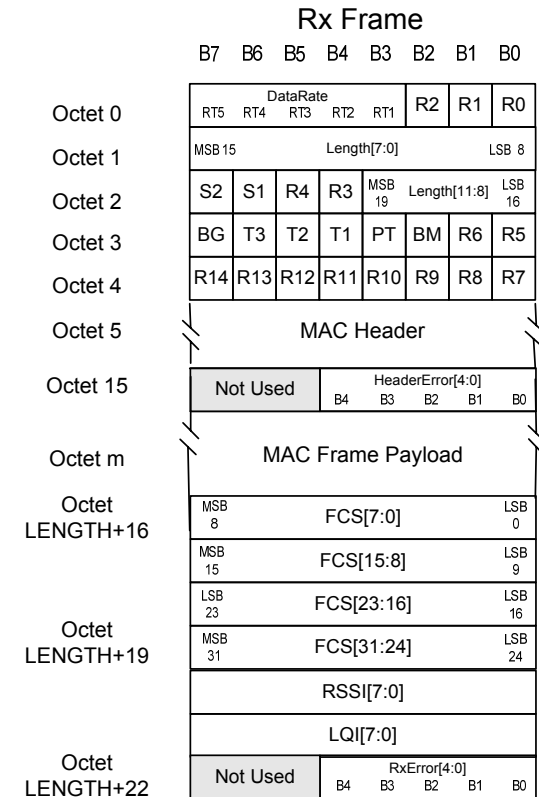
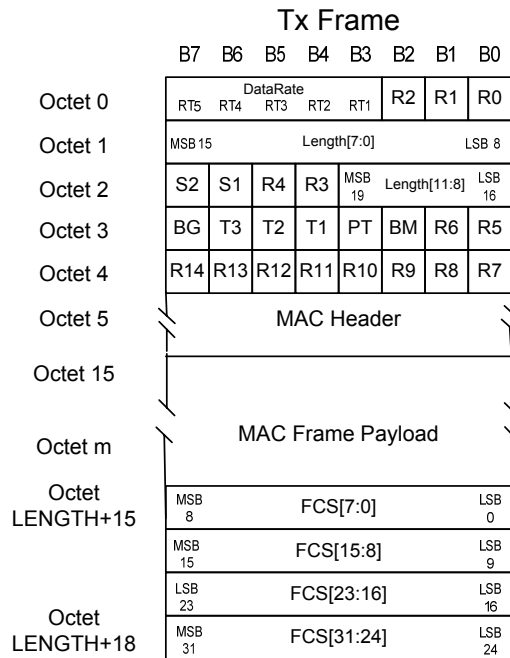
- Receive



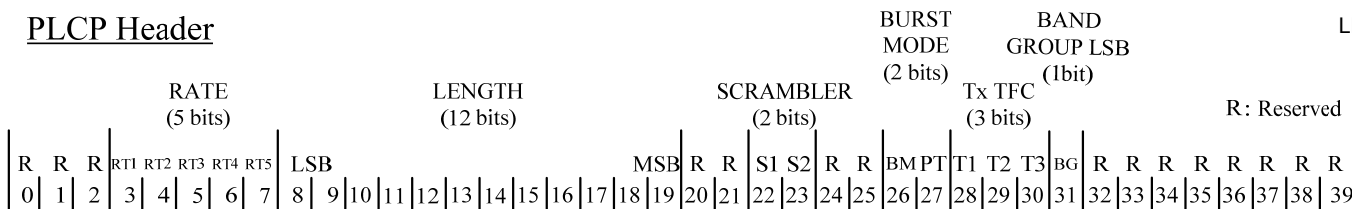
Frame Format



- On transmit:
 - MAC responsible for all fields
- On Receive:
 - PHY passes what it received to MAC, along with status bytes



PLCP Header



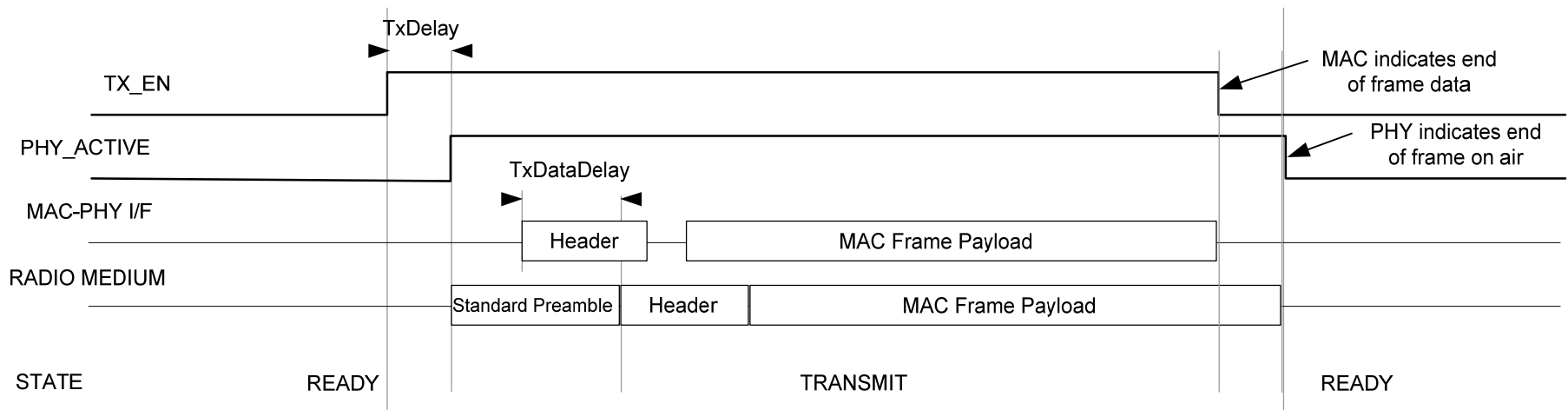


Theory of Operation

- TX_EN, RX_EN & PHY_ACTIVE encode all interface semantics
- All signals are synchronous to rising edge of PCLK
- DATA[7:0] is qualified by DATA_EN
- PHY_ACTIVE provides accurate on-air beginning of frame and end of frame timing from PHY to MAC
 - Tx and Rx offsets to compensate for PHY processing delays
- No 'handshake' between PHY and MAC to indicate when status bytes are being passed
 - MAC counts bytes to determine when the status bytes have arrived

Transmit Delay Intervals

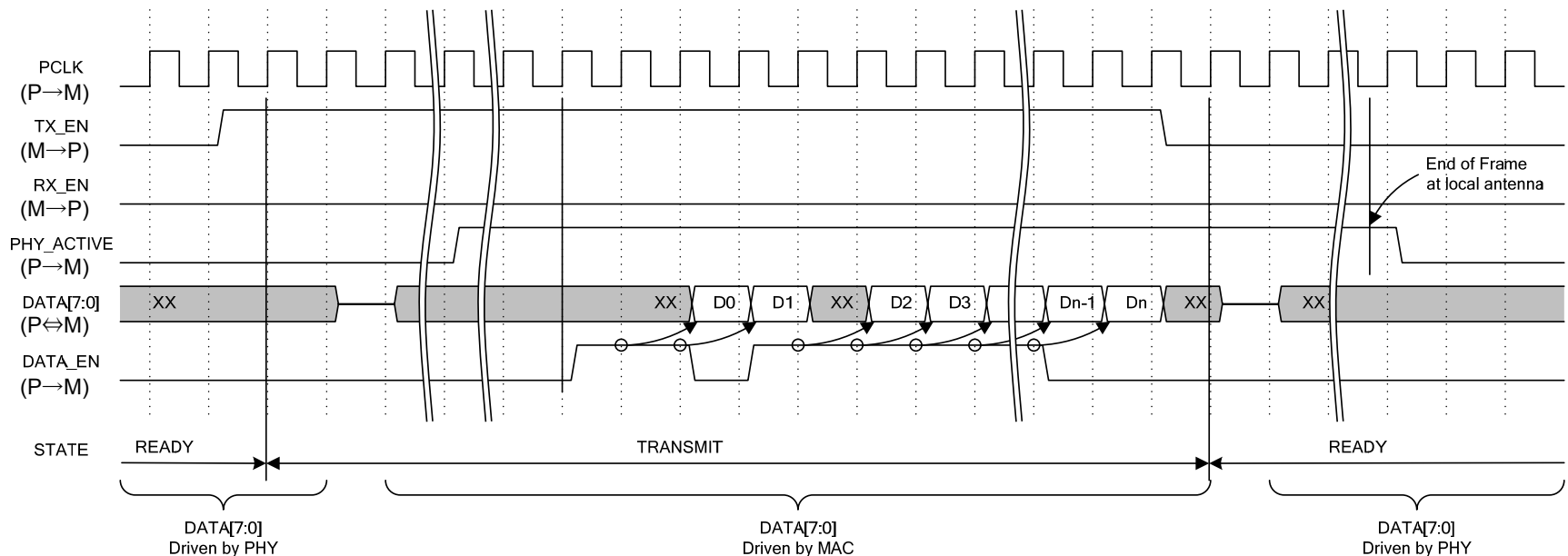
- TxDelay: PHY specific fixed time from TX_EN assertion to beginning of preamble
 - Gives MAC precise control of over-the-air timing
- TxDataDelay: PHY won't request data earlier than TxDataDelay (4us) before end of preamble
 - Gives MAC more time to process previous frame
- PHY_ACTIVE: Provides explicit over-the-air frame timing info



Single Frame Transmit



- PHY uses Data_En to request data from MAC
 - Two clock delay from Data_En assertion to data valid
- MAC deasserts TX_EN when last byte delivered to PHY

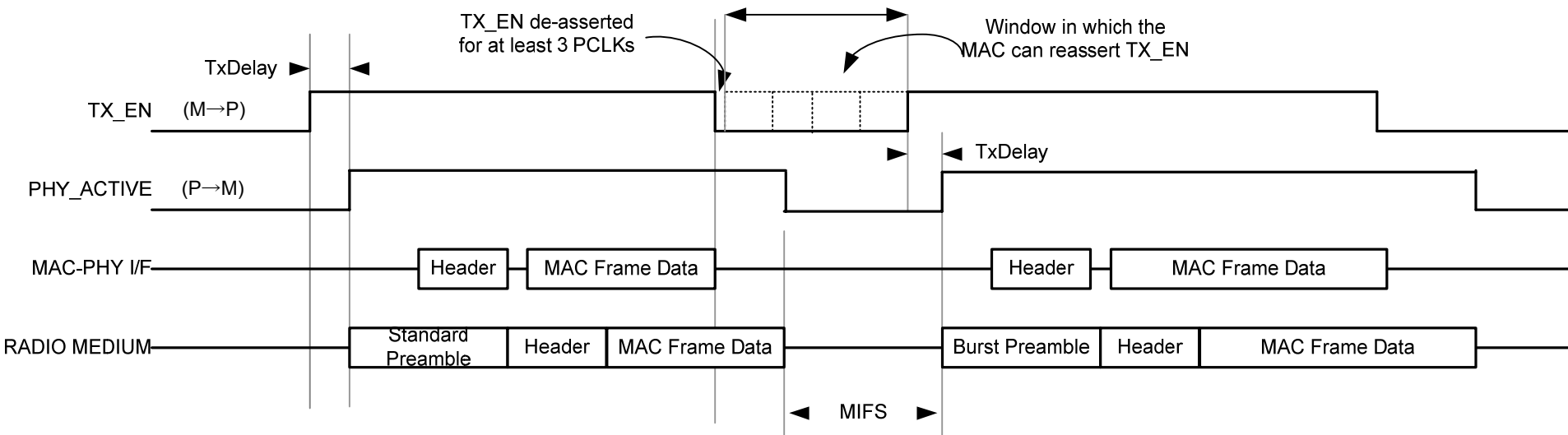


Note change in bus ownership

Burst Mode Transmit



- PHY owns MIFS timing between frames
- TX_EN re-assertion at least TxDelay before MIFS expires
 - Must be deasserted at least 3 PCLK cycles
- BM bit in PLCP must be set



Preamble Control for Transmit

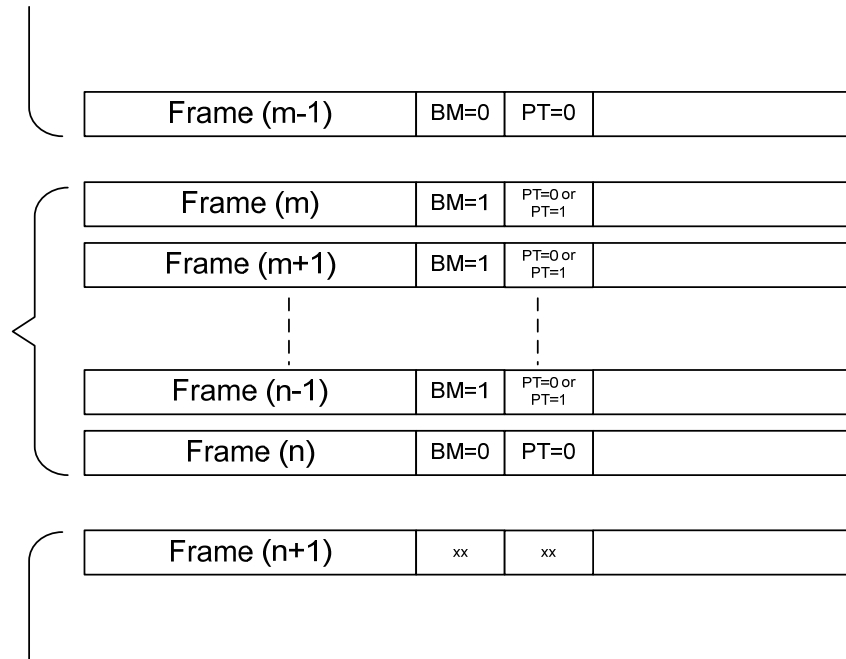


- If in Burst Mode
 - PT tells PHY what preamble to use for next frame
 - Overrides TXPT in register set
- If not in Burst Mode
 - TXPT specified preamble type

Previous Burst or Single Frame Transmission

Burst Transmission

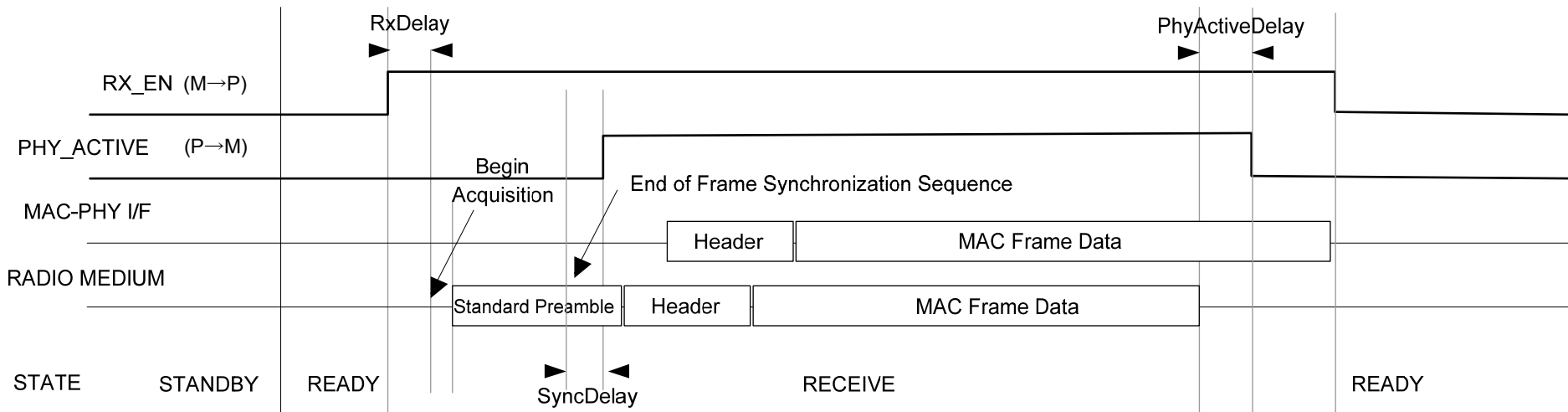
Next Burst or Single Frame Transmission



Receive Delay Intervals



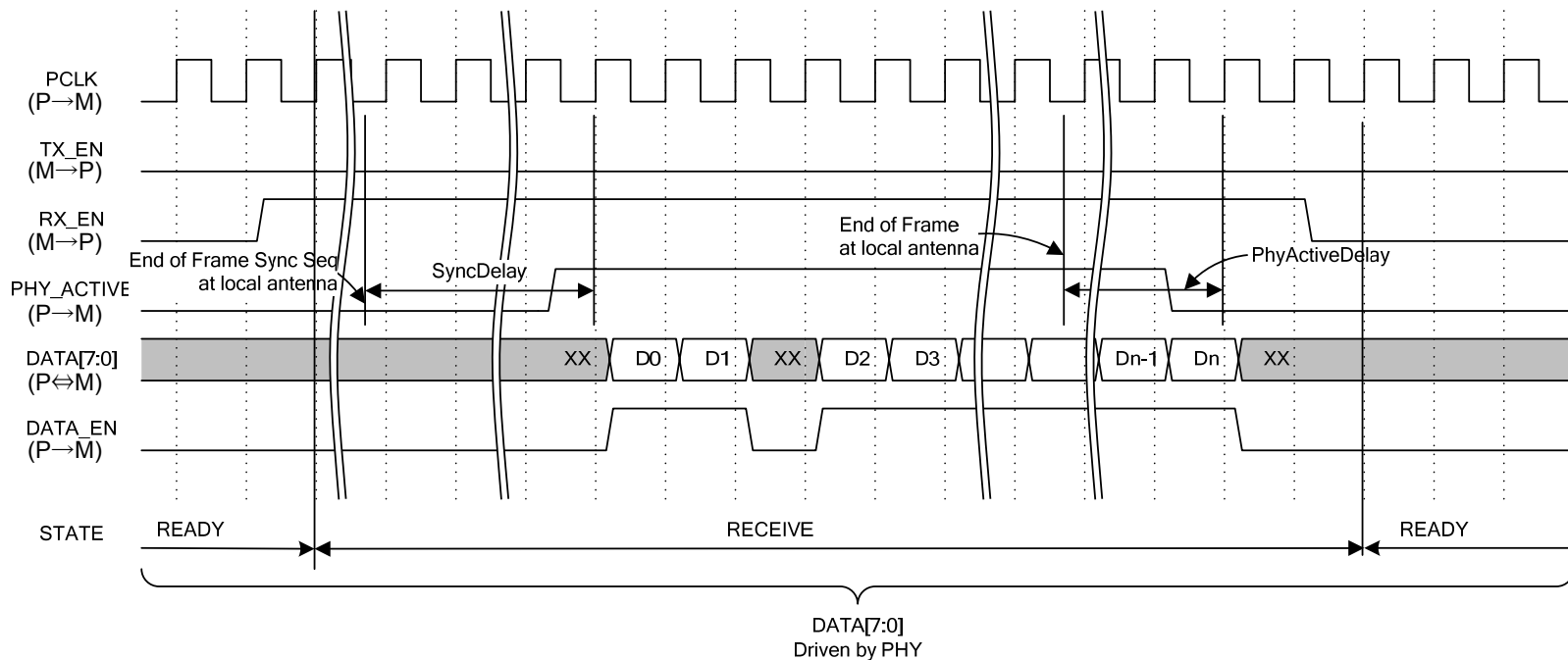
- RxDelay: Time from when MAC asserts RX_EN until PHY is ready to receive
- PHY_ACTIVE edges provide beginning and end of frame timestamps
 - SyncDelay: Time after sync point in preamble until Phy_Active is asserted
 - PhyActiveDelay: Time from end of frame on air until Phy_Active is deasserted



Single Frame Receive



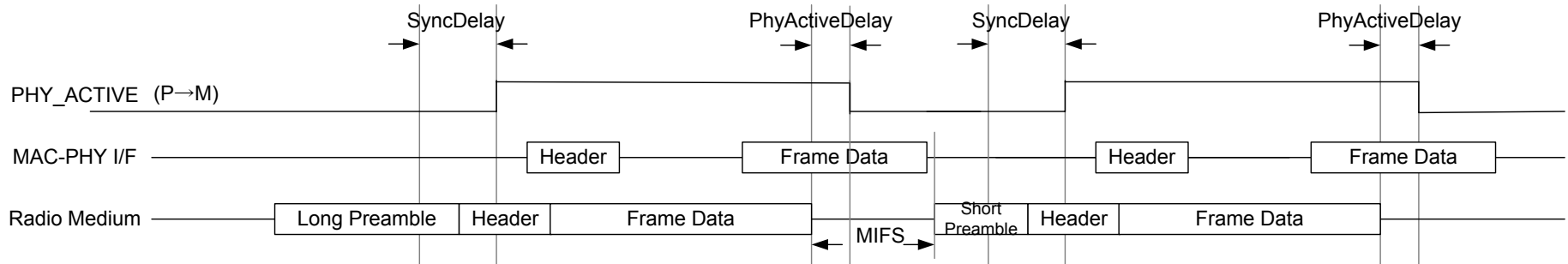
- PHY uses Data_En to deliver data to MAC
 - Data_En asserted and data valid at same clock edge



Burst Mode Receive



- RX_EN maintained asserted during Burst Mode Receive
- PLCP Header signals subsequent frame preamble and burst continuation
- Usual start and end of frame timing via PHY_ACTIVE, SyncDelay and PHYActiveDelay



Preamble Control for Rx



- Burst Mode
 - Next frame arrives exactly MIFs later
 - PT identifies preamble type on next frame
- PTON
 - Can disable PHY processing of PT
- BM and PT not really used by MAC

Previous Burst or Single Frame Transmission

Frame (m-1)	BM=0	PT=0	
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Burst Transmission

Frame (m)	BM=1	PT=0 or PT=1	
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Frame (m+1)	BM=1	PT=0 or PT=1	
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Frame (n-1)	BM=1	PT=0 or PT=1	
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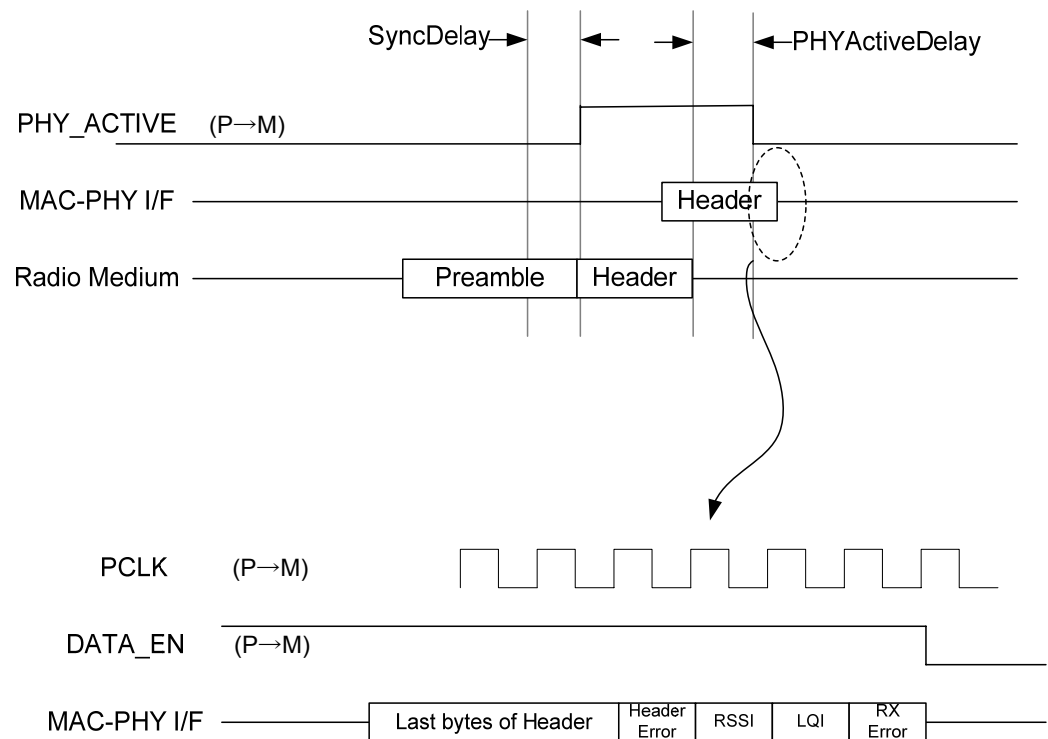
Frame (n)	BM=0	PT=0	
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Next Burst or Single Frame Transmission

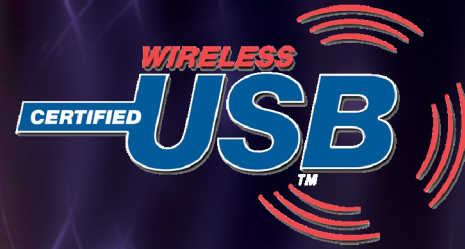
Frame (n+1)	xx	xx	
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Zero Length Frame Rx

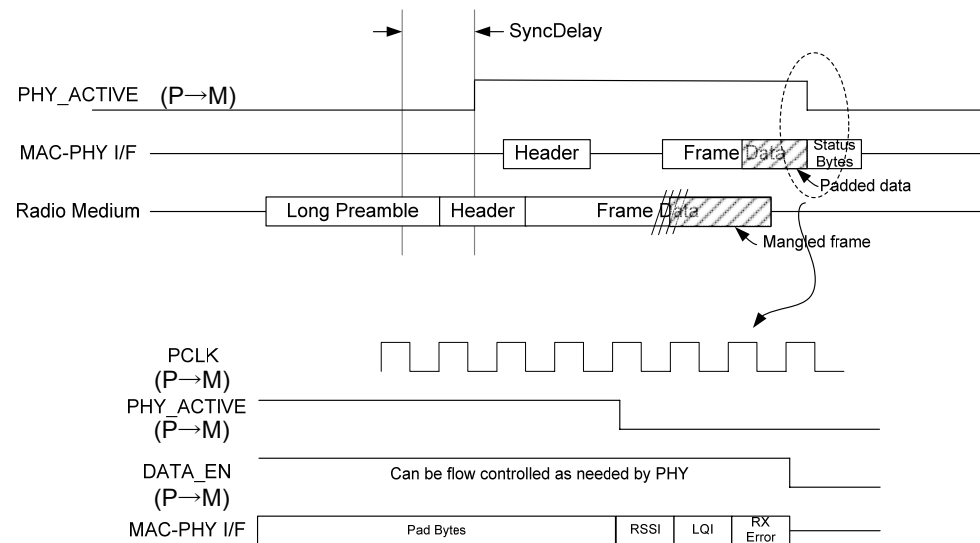
- PHYActiveDelay allows accurate end-of-frame-on-air timing
- Frame status bytes follow header status byte on data lines
 - Flow-controlled by DATA_EN
 - MAC knows to expect them because length was zero



PHY Aborted Rx



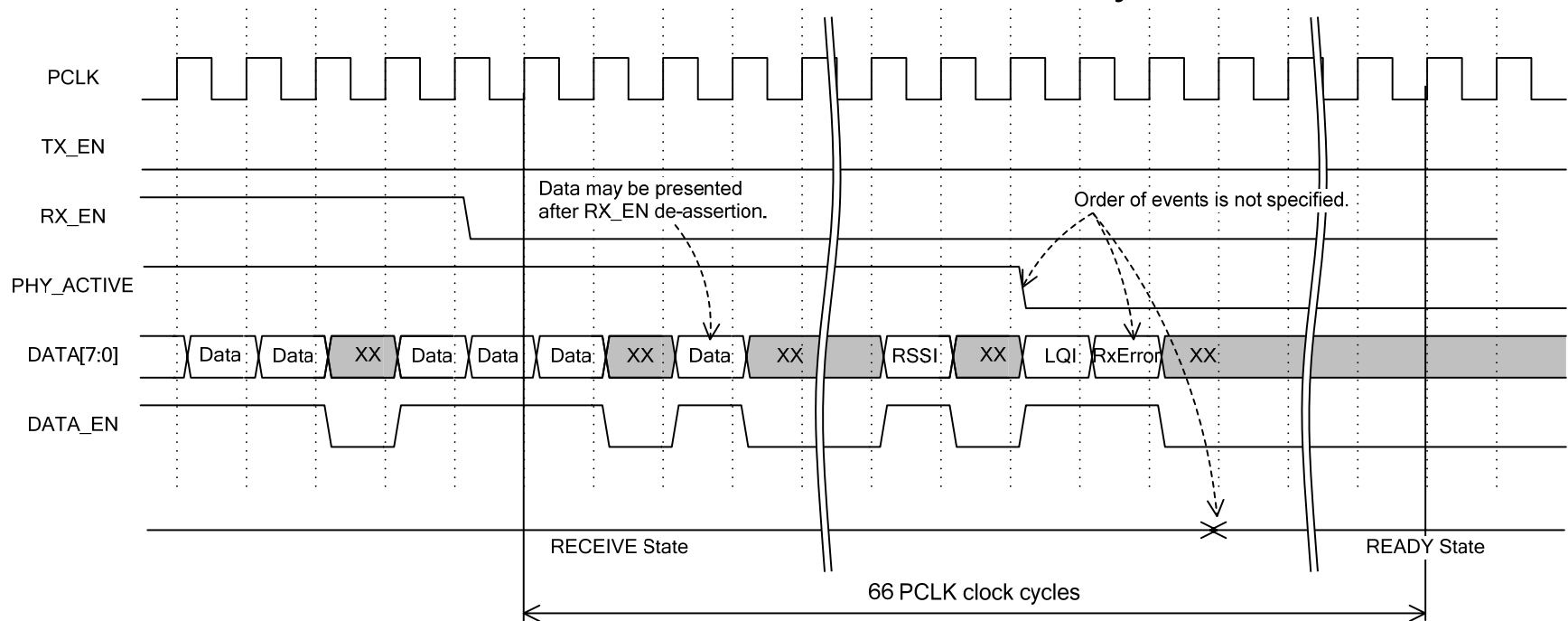
- This case is an Unrecoverable Detected Payload Error
- After detecting error, PHY transfers enough bytes (pad) to meet the header specified length.
- PHY de-asserts PHY_ACTIVE after pad bytes and then passes status bytes to MAC



MAC Aborted Rx



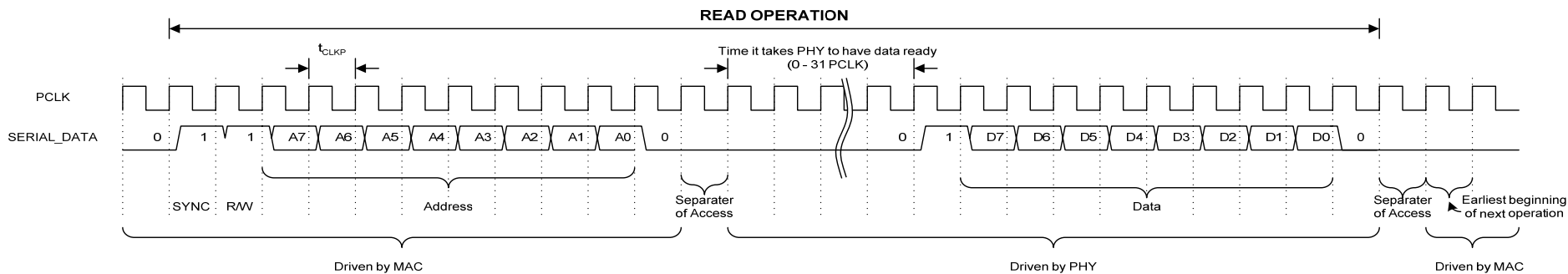
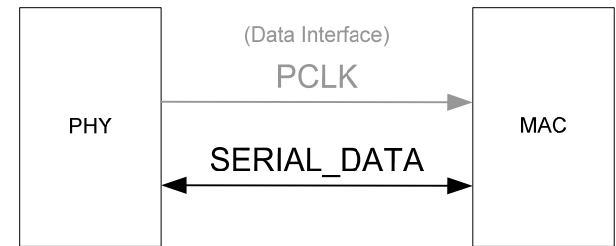
- This is the common case where MAC determines (from header data) that the packet is not interesting for this device. MAC de-asserts RX_EN
- PHY responds by de-asserting PHY_ACTIVE
- MAC assumes last three bytes delivered (after 66 clocks) are Rx status bytes



Serial Register Access



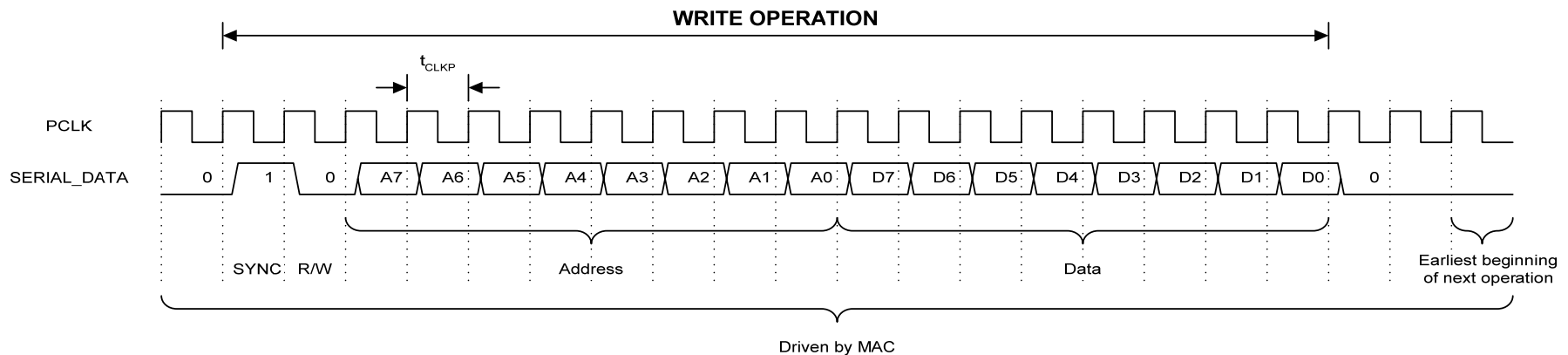
- Bi-directional signal for register read/write
- Synchronous to PCLK
- Start pulse '1'
 - Then '1' = read operation
 - 8-bit address
 - Release signal to PHY
 - 8-bit data



Serial Register Access

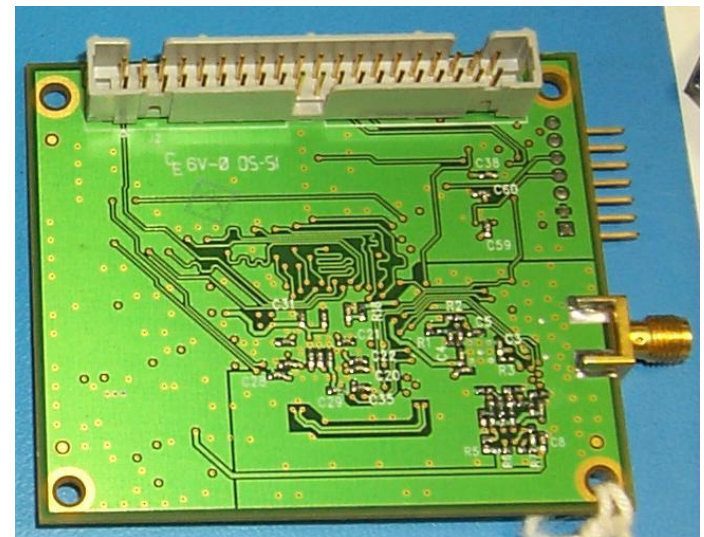
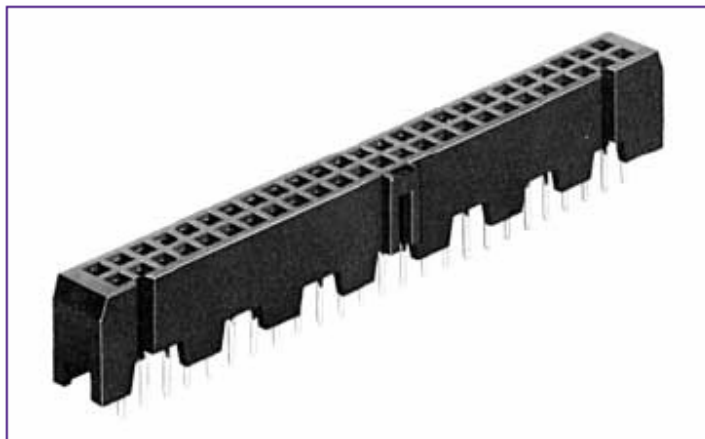


- Write Operation
 - Start pulse '1'
 - Then '0' = write
 - 8-bit address / 8-bit data
 - No change of signal drive



Standardized Connector

- Standard connector defined for easy prototyping and debug
 - 2x20 IDE-style connector
 - Implemented by many MAC and PHY vendors
- Spec location: www.intel.com/go/wusb
 - Look in 'Whitepapers' section



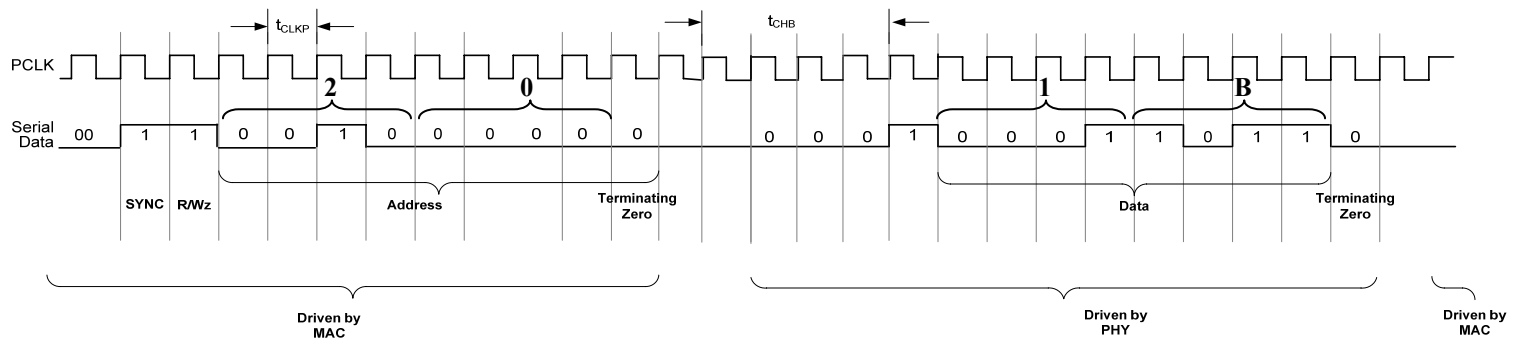


Back-up Slides

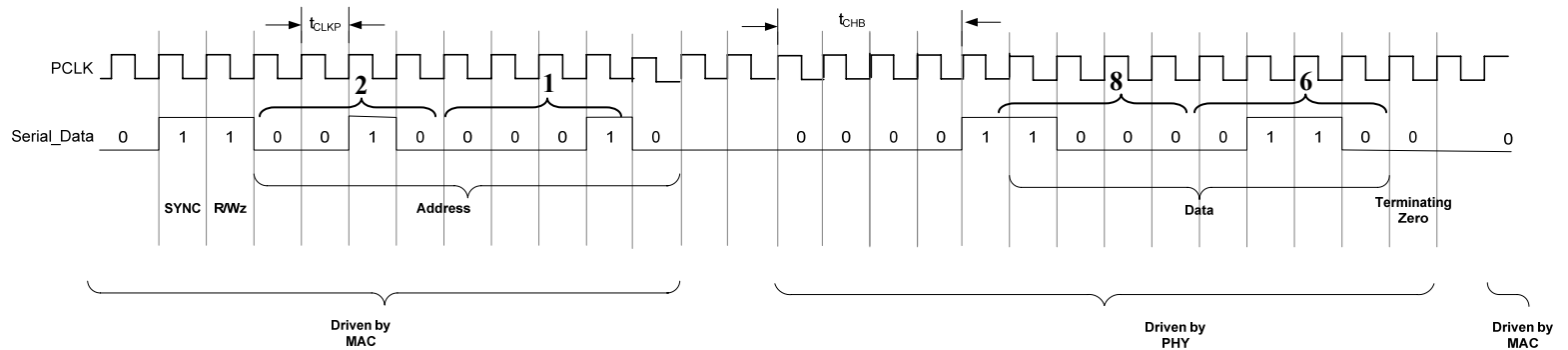
Read Example



- Address 0x20 Data 0x1 B

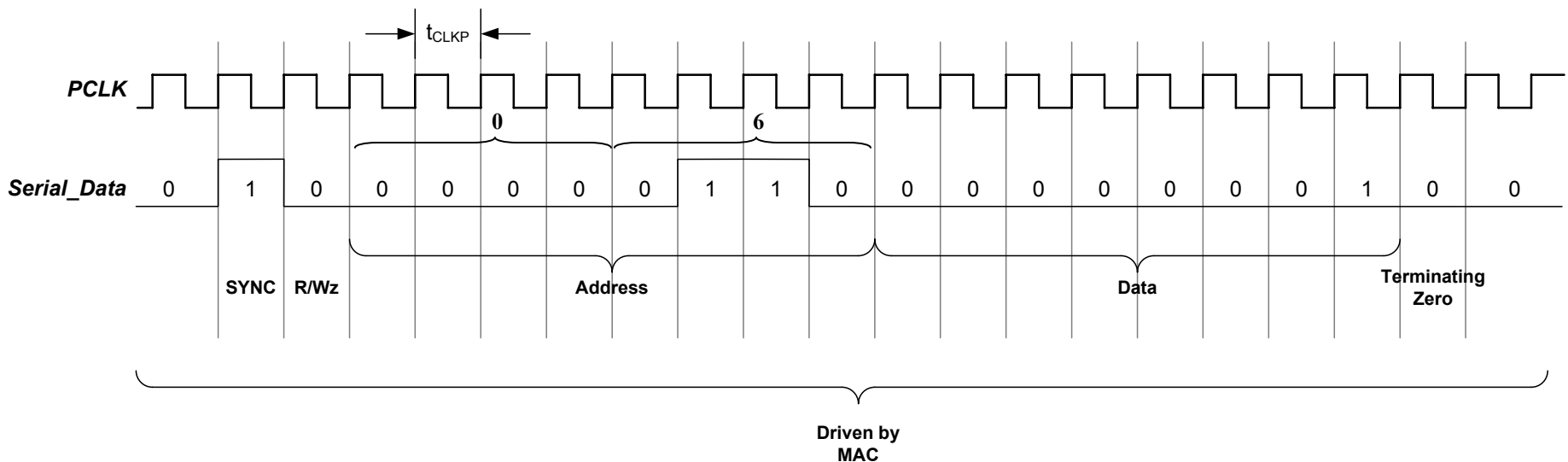


- Address 0x21 Data 0x86

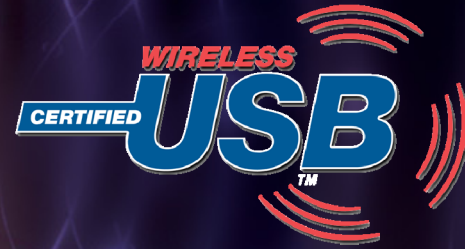


Write Example

- Set PMMODE to READY
address 0x06, data 0x00



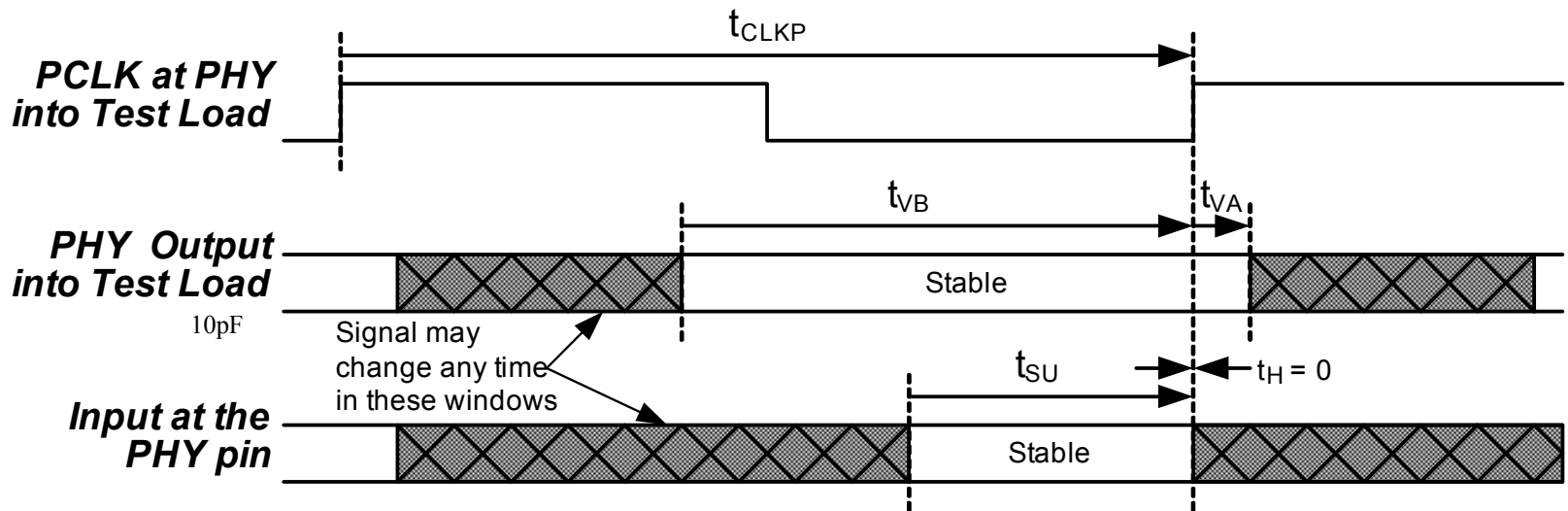
I/O DC Specifications



- 3.3V signaling levels for good interoperability
- Should not require new buffer designs

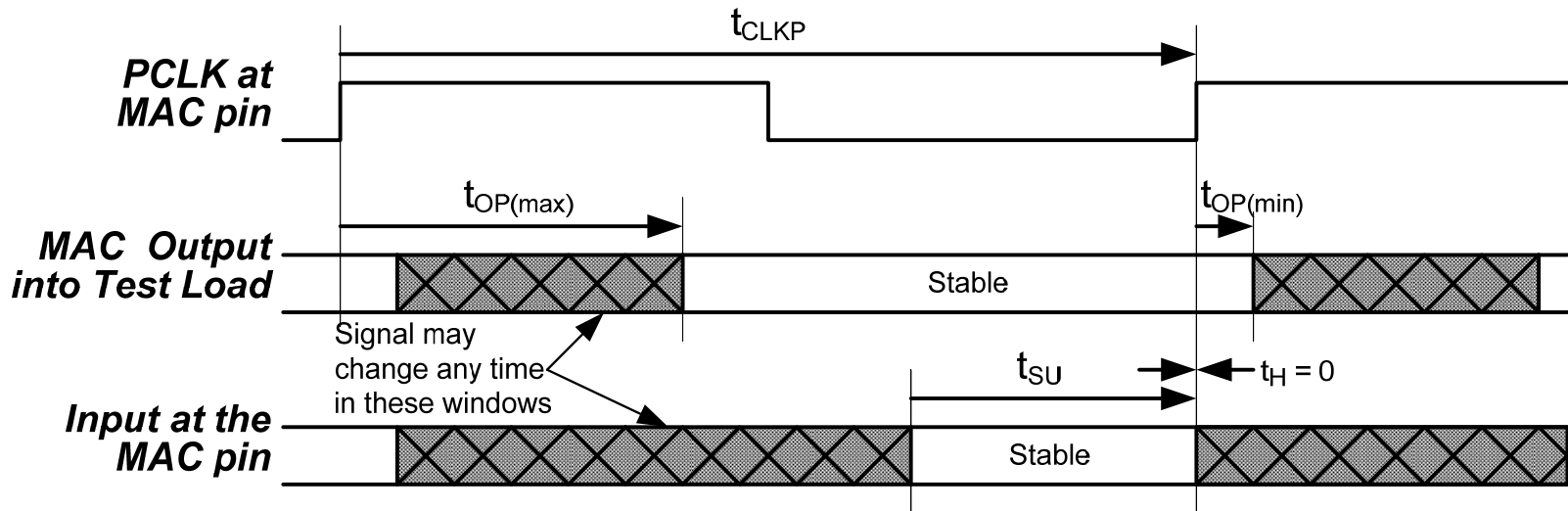
	Parameter	Description	Conditions	Min	Max	Units
	V_{CC}	Supply Voltage		3	3.6	V
Input	V_{IH}	Input high voltage		2	$V_{CC}+0.5$	V
	V_{IL}	Input low voltage		-0.3	0.8	V
	I_{IL}	Input leakage current	$0 < V_{in} < V_{CC}$	-10	10	μA
	C_{IN}	Input pin capacitance			10	pF
Output	V_{OH}	Output high voltage	$I_{out} = -4mA$	2.4		V
	V_{OL}	Output low voltage	$I_{out} = 4mA$		0.4	V

Signal Timing at PHY



Value	Description	Max	Min
t_{CLKP}	PHY Clock Period	-	15ns
t_{VB}	Time PHY output data is valid before the rising edge of PCLK	-	9ns
t_{VA}	Time PHY output data is valid after the rising edge of PCLK	-	1ns
t_{SU}	Setup time, to rising edge of PCLK	-	5ns
t_H	Hold time, from rising edge of PCLK	-	0ns

Signal Timing at MAC



Value	Description	Max	Min
t_{CLKP}	PHY Clock Period	-	15ns
t_{OP}	Time MAC output data is valid from the rising edge of PCLK	6ns	1ns
t_{SU}	Setup time, to rising edge of PCLK	-	5ns
t_H	Hold time, from rising edge of PCLK	-	0ns

MAC to PHY Setup & Hold



Ideal MAC to PHY Setup Margin

Tclk	=	15.0 ns
- Tco(max)	=	- 6.0 ns
- Tsu	=	- 5.0 ns
- Tpclk_flt	=	- 0.2d ns
- Tflt(max)	=	- 0.2d ns
Tsu_margin	=	(4.0 - 0.4d) ns

Ideal MAC to PHY Hold Margin

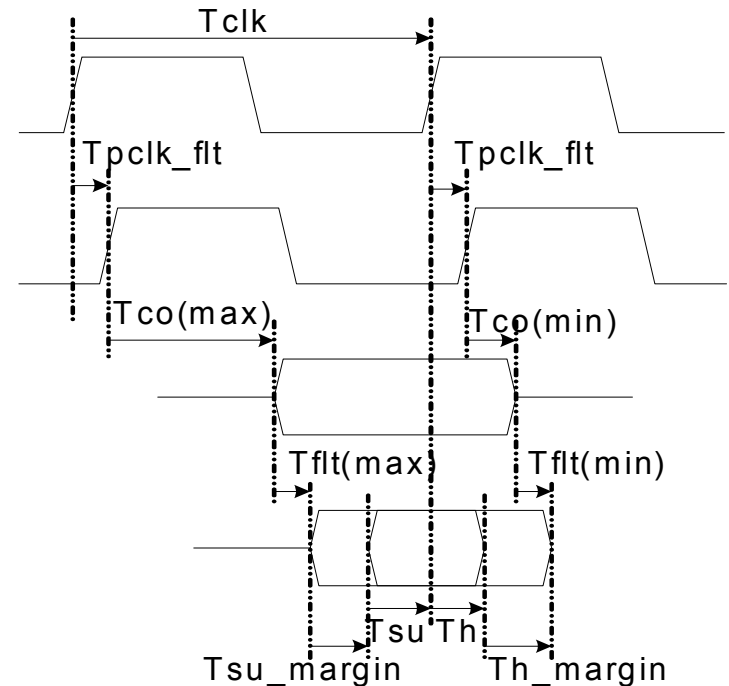
Tco(min)	=	1.0 ns
- Th	=	- 0.0 ns
+ Tpclk_flt	=	+ 0.2d ns
+ Tflt(min)	=	+ 0.2d ns
Th_margin	=	(1.0 + 0.4d) ns

PCLK at PHY
into test load

PCLK at the
MAC pin

MAC Outputs
into test load

Inputs at the
PHY pins



Notes:

- Ideal margin calculations ignore clock jitter, trace length/impedance mismatch, crosstalk, reflections, etc.
- Signal propagation delay assumed to be 200 ps/in for both min and max.
- d = Trace length in inches

PHY to MAC Setup & Hold



Ideal PHY to MAC Setup Margin

T_{vb}	=	9.0 ns
- T_{su}	=	- 5.0 ns
- $T_{flt(max)}$	=	- 0.2d ns
+ T_{pclk_flt}	=	+ 0.2d ns
T_{su_margin}	=	4.0 ns

Ideal PHY to MAC Hold Margin

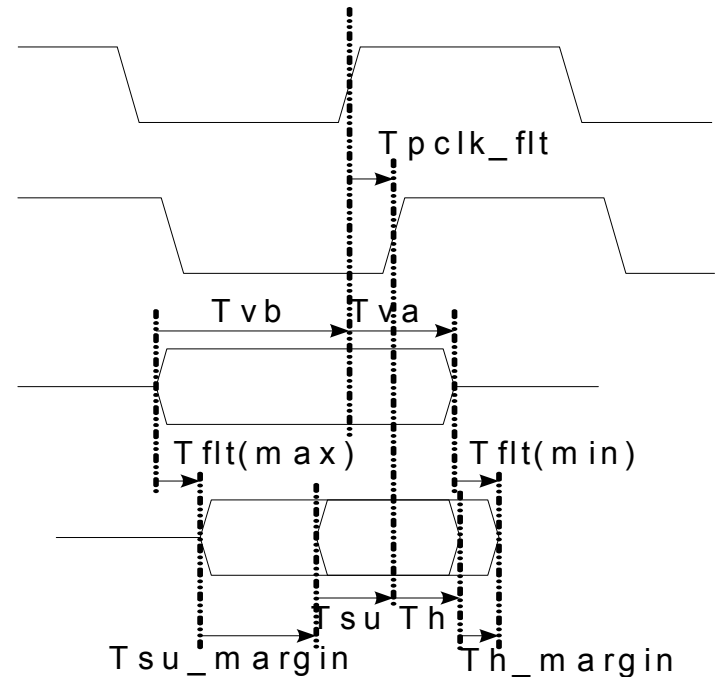
T_{va}	=	1.0 ns
- T_h	=	- 0.0 ns
+ $T_{flt(min)}$	=	+ 0.2d ns
- T_{pclk_flt}	=	- 0.2d ns
T_h_margin	=	1.0 ns

PCLK at PHY
into test load

PCLK at the
MAC pin

PHY Outputs
into test load

Inputs at the
MAC pins



Notes:

- Ideal margin calculations ignore clock jitter, trace length/impedance mismatch, crosstalk, reflections, etc.
- Signal propagation delay assumed to be 200 ps/in for both min and max.
- d = Trace length in inches

CCA Reporting



- CCA controlled by CCRE register (CONTROL)
- Reporting begins CCAValidTime after setting CCRE
- CCA cannot be reported during TRANSMIT, STANDBY, SLEEP states

