USB DevDays

Active Cable

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USB Developer Days 2019 – Taipei, Taiwan

November 20, 2019

Presentation Agenda

- Introduction
- Active Cable Eco-System
- USB PD
- What coming for USB4™
- High Level Requirements
- Mechanical / Thermal
- Eco-system issues observed
- Summary

How do they fit in eco-system

- ***The maximum passive cable length is inversely proportional to its maximum speed***
    - USB 3.2 Gen1 ~2 meter
    - USB 3.2 Gen2 ~1 meter
    - USB4™ Gen 3 ~ 0.8 meter
- Active Cables' longer lengths enable applications like
    - Extra Large Displays
    - Cameras, Machine Vision, Virtual Reality
- Active Cables are already in the USB eco-system, but in small quantities
    - Higher speed busses such as Thunderbolt™ and DisplayPort™ already use Active Cables

Use Cases – Docks (w/ 15.4” Laptop)

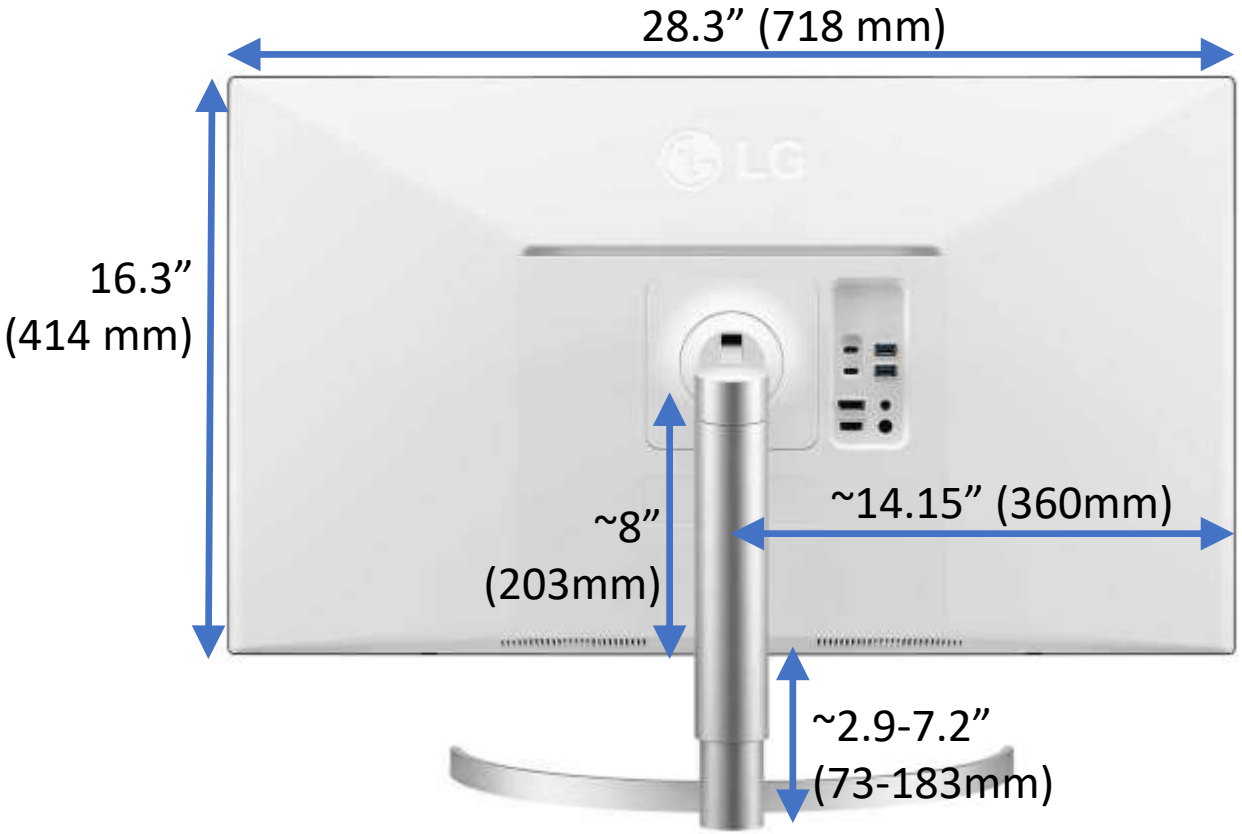
12.95” (329 mm)

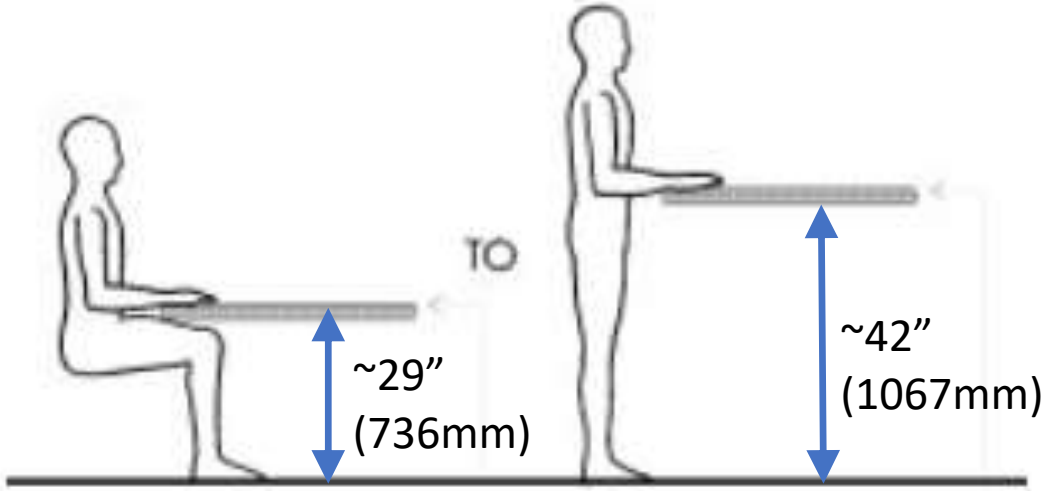
8.75” (222 mm)

3.1”
(78.7 mm)

31.5” = 0.8 meter

Use Case: 32” Display and Sit/Stand Desks





Height for Sit-to-stand Adjustable Work Surfaces

- Minimum: 26” - 40”; Range = 15"
- Optimal: 22” - 47”; Range = 25"

31.5” = 0.8 meter

Optically Isolated Active Cable (OIAC)

- Use cases
  - Medical – MRI machines
  - Industrial – factory Floor (i.e., Cameras)
  - Extended Lengths – up to 50m
    - Remote Storage (RAIDs)

- Limitations
  - No VBUS Power through cable
  - No USB2
  - Both ends must start as DFP
    - At least one end MUST be DRD capable
    - Both ends must supply Vconn

- USB4™ work will be forth coming (2020)

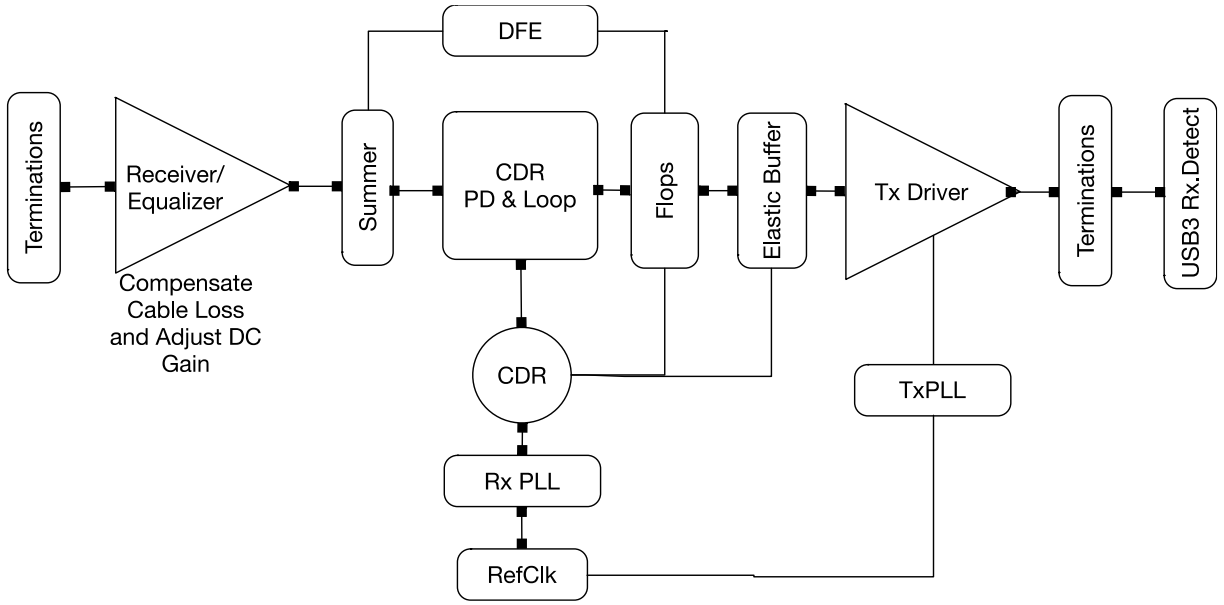
Active Cables Types (< 5 meters)

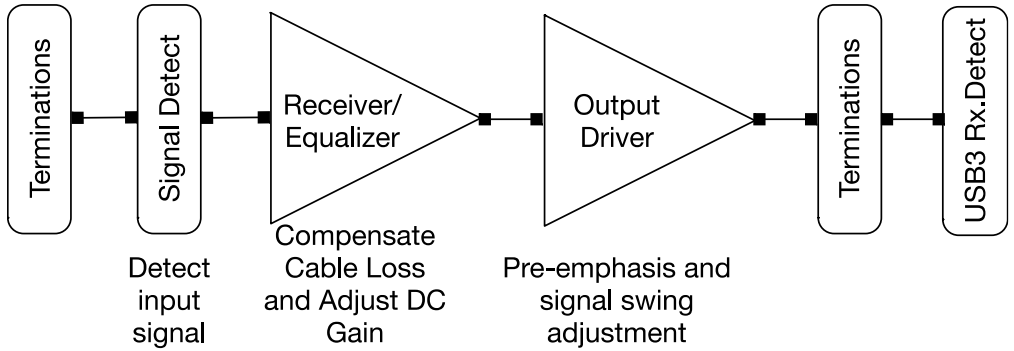
- High Speed Interface Identification
  - Active Elements: re-timer, Linear re-driver *(Under Investigation)*
  - Physical Connection: Copper, Optical

- USB PD Identification allows for the system to understand full link
  - Re-timer Link Training (USB4™) – Port to re-timer and re-timer to Port
  - Re-driver Link Training (USB4™) – Port to Port
  - Allows Link Training to be optimized for cable type
  - Optical – Future proof

Active Cable - Re-driver vs. Re-timer

- Re-timer is defined in Appendix E in USB 3.2
- There will be a forth coming document for USB4™ re-timers (by end of 2019)



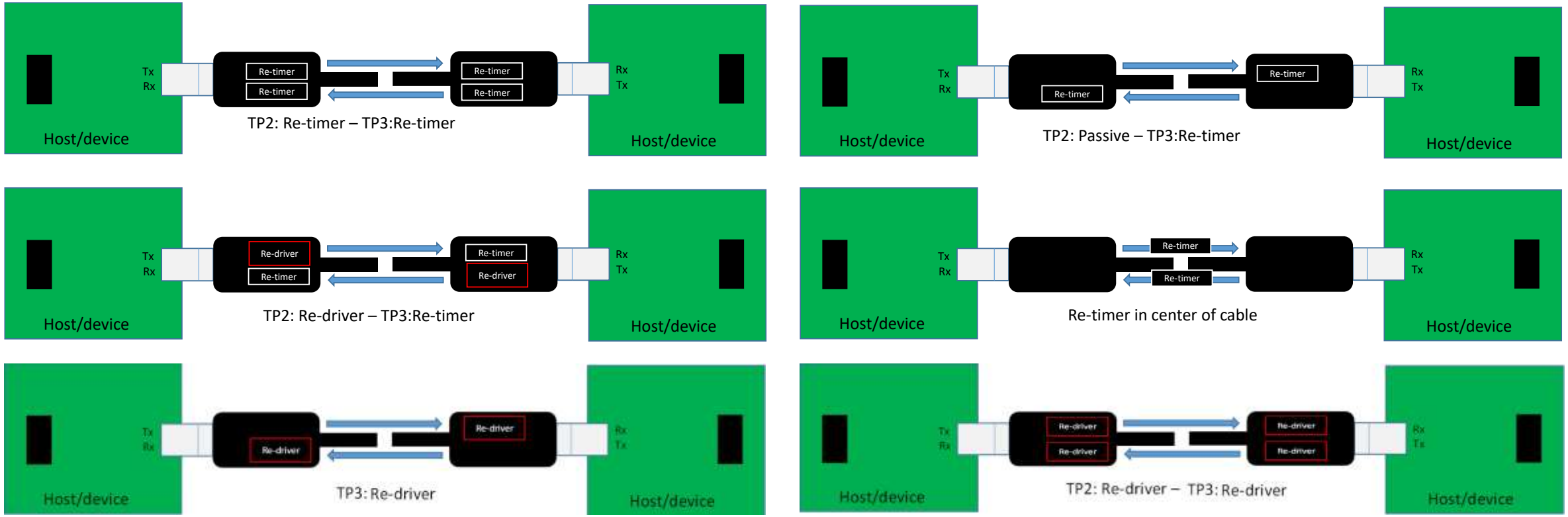


USB 3.2 Gen1/USB4: Bit Level Re-timer
USB 3.2 Gen2: SRIS Re-timer
Digital circuit capable of resetting the jitter budget and more complex equalization

Linear Re-driver
Analog circuit not capable of resetting the jitter budget

USB 3.2 Cable Architectures

- **Re-drivers are currently *under investigation* in USB-IF**
- Active cables without re-timers connected to TP3 are *currently* out of scope.



USB PD

- Active Cables shall respond to SOP’ and optionally on SOP”
  - SOP’ and SOP” assignment is fixed at time of manufacture
- Discover Identity (eMarker) returns information about the cable
  - High Speed Link
    - re-timer, Linear re-driver
    - Copper, Optical
  - Optically Isolated Active Cable
- Cable Status reports plug’s internal temperature and thermal shutdown status
- New for USB4™ – Entry to USB operation (See next slide)
- Resets
  - Cable Reset (Resets logic)
  - Data Reset (USB4™) (Cycles Vconn)
- When Alternate Modes are supported
  - Discover SVIDs, Modes
  - Enter/Exit Mode

USB4™ Active Cables

- Support for USB4™ Active Cable expected to be added to Chapter 6 by end of 2019
- Power on default: USB 3.2
- USB4 Entry
  - Entry sequence is defined in the USB Type-C® Specification Release 2.0
    - Discover Ports, Cables (Discover ID - SOP and SOP') (See next slide)
    - Decision Flow (Chapter 5 – USB Type-C spec)
    - Thunderbolt™ Alt-Mode Compatibility (Appendix F – USB4 spec)
  - USB PD Specs defines the Enter USB message to configure the cable into USB4 operation
- SBU participate in link training in USB4
  - Re-timed Active Cable:
    - Digital Signaling specification in USB4
    - Passive cable specification in USB 3.2
  - Re-driven Active Cable:
    - Passive cable specification (same as USB 3.2)

USB4™: Cable - Discover ID

- Passive Cable VDO

Bit(s)	Field	Description
		…
B2…0	USB Highest Speed	000b = [USB 2.0] only, no SuperSpeed support 001b = [USB 3.2] Gen1 010b = [USB 3.2]/ [USB4] Gen2 011b = [USB4] Gen3 011b…111b = Reserved, Shall Not be used

- Active Cable VDO1

Bit(s)	Field	Description
		…
B23…21	VDO Version	Version Number of the VDO (not this specification Version): • Version 1.3 = 011b
		…
B2…0	USB Highest Speed	000b = [USB 2.0] only, no SuperSpeed support 001b = [USB 3.2] Gen1 010b = [USB 3.2]/ [USB4] Gen2 011b = [USB4] Gen3 011b…111b = Reserved, Shall Not be used

- Active Cable VDO2

Bit(s)	Field	Description
		…
B14…12	U3/CLd Power	000b: >10mW 001b: 5-10mW 010b: 1-5mW 011b: 0.5-1mW 100b: 0.2-0.5mW 101b: 50-200µW 110b: <50µW 111b: ***Reserved***, ***Shall Not*** be used
		…
B10	Physical Connection	0b = Copper 1b = Optical
B9	Active element	0b = Active Re-driver 1b = Active Re-timer
B8	USB 4 Supported	0b = ***[USB4]*** supported 1b = ***[USB4]*** not supported
		…
B2	Optically Isolated Active Cable	0b = No 1b = Yes
B0	USB Signaling Gen	0b = Gen 1 1b = Gen 2 or higher Note: see VDO1 USB Highest Speed for details of Gen supported.

Retimed Active Cable SBU Characteristics
(USB4™ Re-timed Cables)

Defined as digital signals. SBU is received on the SBRX and communicated on SBTX per the link training protocol.
→ Will be released in the USB4™ Active Cable (added to USB Type-C Spec Chapter 6) – End of 2019

Table 3-1. SBTX and SBRX Specifications

Symbol	Description	Min	Max	Units	Conditions
$SBTX_{VOH}$	SBTX High Voltage	2.4	3.47	Volts	SBTXIOH = −600 µA (set by 3.4 V/0.5 MΩ). See Note 1.
$SBTX_{VOL}$	SBTX Low Voltage	−0.05	0.4	Volts	SBTXIOL = 600 µA (set by 3.4 V/ 10 KΩ). See Note 1.
$SBRX_{VIH}$	SBRX High Voltage Detection	2.0	3.72	Volts	See Note 2, Note 6.
$SBRX_{VIL}$	SBRX Low Voltage Detection	−0.3	0.65	Volts	See Note 7.
$SBRX_{IIH}$	SBRX High input current	--	25	µA	Vin = VDD.
$SBRX_{IIL}$	SBRX Low input current	--	0.4	µA	Vin = 0 V.
SBX_{TRTF}	SBTX/SBRX 10-90% Rise/Fall time	3.5	--	ns	Minimum to reduce crosstalk and EMI. See Note 3.
$SBTX_{PULL\_UP\_RES}$	SBTX pull-up resistor	7.0K	10.5K	Ω	See Note 4.
$SBRX_{PULL\_DOWN\_RES}$	SBRX pull-down resistor	0.70M	1.05M	Ω	See Note 5.
$SBTX_{SOURCE\_IMPEDANCE}$	SBTX output impedance	25	90	Ω	
SBRX_Cin	SBRX Input Capacitance	--	8	pF	
SBX_UI	UI duration	980	1020	ns	

Notes:
1. This parameter shall be verified in both transaction and steady state. The steady state condition shall be measured with a continuous high or low level. The transaction state condition shall be measured when sending SBX data. Over/undershoot shall be ignored.
2. A buffer may be used between the connector and the Router to meet these logic levels. When present, this buffer shall meet SBRXVIH and SBRXVIL as defined above.
3. Verify this parameter in transaction and not from power down to power up. The minimum is specified to control crosstalk and EMI.
4. A Router shall terminate the SBTX signal to 3.3 V nominal power.
5. A Router shall terminate the SBRX signal to GND.
6. Logical high maps to VIH.
7. Logical low maps to VIL.

Active Cable SBU Characteristics
(USB 3.2 & USB4™ Re-driven cables)

Defined in terms of passive cable characteristics

Name	Description	Min	Max	Units
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wire		26	ns
rCable_SBU	DC resistance of SBU wires in the cable in USB		40	Ω
vCable_SBU	Cable voltage swing on SBU wires	−0.3	4.0	V
Insertion Loss[1]	Cable insertion Loss		5 @ 0.5MHz 7 @ 1MHz 12 @ 10MHz 13 @ 25MHz 15 @ 50MHz 16 @ 100MHz	dB
iCableSBU	Maximum end-to-end current	-25	+25	mA

Active Cable Requirements

	USB 3.2 Active Cables			USB 4 Active Cables	
Features	Optically Isolated Active Cable	Short Active Cable		Short Active Cable	
USB4	Not Supported	Not Supported		Re-driven	Re-timed
USB 3.2	Re-driven	Re-driven	Re-timed	Re-driven	Re-timed
SBU	Optional normative support in Alternate Modes only	Passive		Passive	USB 3.2: Passive (Pass through) USB4: Digital (Participates in link training)
Number Of Lanes	2-lane support required				
USB 2.0	Only USB2.0 Bus Reset and Billboard[1]	Passive Connection		Passive Connection	
End-to-End USB-PD Communication	Subset of messages supported	All messages supported		All messages supported	
End-to-End Ground and Vbus Connections	No[2]	Yes		Yes	
Vconn Power Consumption in Active State	1.0W Maximum (1-lane)[3] 1.5W Maximum (2-lane)[3]				
Alternate Modes	Optional				
Notes					

1) An OIAC Legacy Adapter required for USB 2.0 support. (See Section 6.6.4.3.1)
2) Requires OIAC Legacy Adapter for use with a Sink (See Section 6.6.4.1 and 6.6.4.3.1)
3) OIAC Vconn Power is per plug end

Power Requirements

- VBUS
  - All active cables meet the same limits of the IR Drop on VBUS and GND as passive cables.
- VCONN
  - VCONN sourced at only one end of the cable and is isolated from the other by the cable
  - VCONN sink requirements
    - 1W when operating one lane (1.5 W when operating two lanes)
    - Power dissipation in U3/CLd, Rx.Detect, or eSS.Disabled is very low because cable may be in that state for extended periods with VCONN applied.

Power State Requirements

State	Requirement	Maximum Power Consumption VCONN	Target Power Consumption VCONN	Power Consumption Notes
U0/CL0	Required	1.0W 1-lane 1.5W 2-lane		Applies to POLLING.LFPS, TRAINING, and RECOVERY states.
U1/CL1	Logically required	≤ U0/CL0 power		Forwarding LFPS is required
U2/CL2	Logically required	≤ U1/CL1 power		Forwarding LFPS is required
U3/CLd	Required	5 mW	2 mW	eMarker in sleep.
Rx.Detect	Required	5 mW	2 mW	Rx.Detect period may be lengthened when no USB 3.2 terminations have been detected. eMarker in sleep.
eSS.Disabled	Required	5 mW	1 mW	USB 3.2 is disabled. eMarker in sleep.

Linear Re-driver (LRD) Active Cable
Investigation Topics being discussed

- LFPS Attenuation Requirements
- Return loss
- Insertion loss
- Noise
- Frequency and Time Domain Specifications

- For both USB4™ and backward compatibility to USB 3.2 systems

- USB4: If a Router Assembly contains linear re-drivers, a re-timer shall be placed between the linear re-driver and the USB Type-C connector

USB 3.2/USB4™ U0 Active Cable Latency

- Repeaters in active cables will meet the U0 delay requirements defined in USB 3.2 Appendix E
- USB4 re-timer requirements are subject to change

Retimer Standard	Specification	Re-timer Requirement	Active Cable Requirement
USB 3.2 Gen1 x1	U0 Latency	≤ 50 ns re-timer	125 ns cable legacy interoperability 3 ms cable new host/devices/hubs
USB 3.2 Gen2 x1	U0 latency	≤ 140 ns re-timer	305 ns cable legacy interoperability 3 ms cable new host/devices/hubs
USB 3.2 Gen1 x2	U0 Latency	≤ 300 ns re-timer	3 ms
USB 3.2 Gen2 x2	U0 Latency	≤ 200 ns re-timer	3 ms
USB4	tLatency2	≤ 50 ns re-timer	not defined
	tLatency3	≤ 30 ns re-timer	
	tSkew	≤ 8 ns Lane0/lane1 added skew and Latency difference between directions of re-timer	

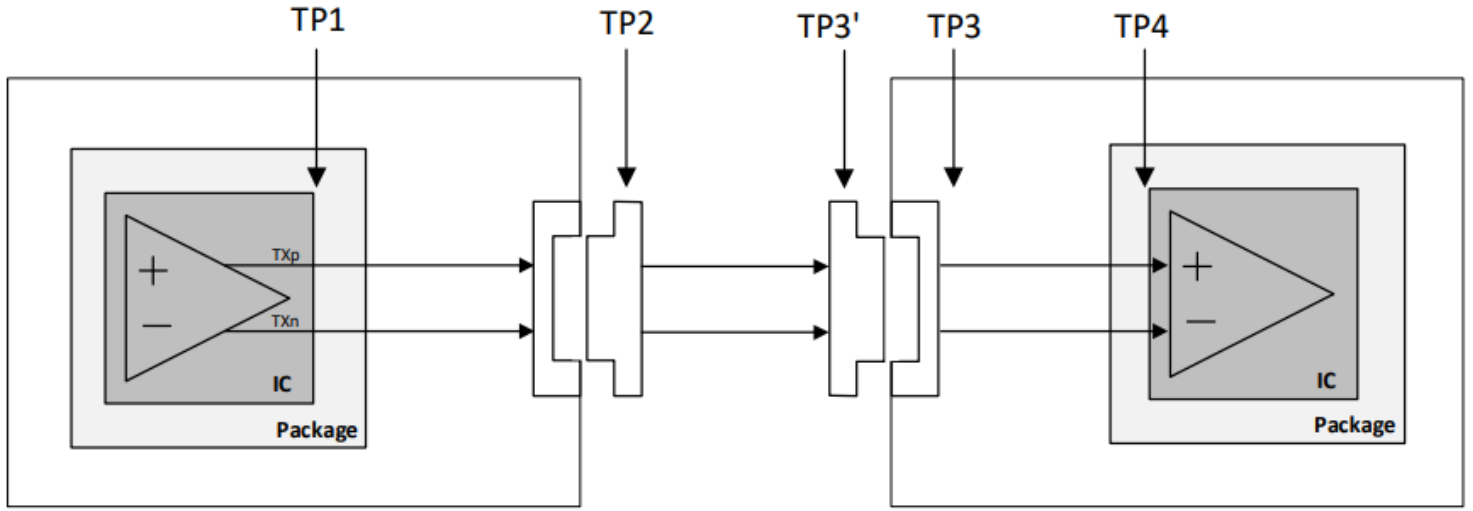
USB 3.2/USB4™ Sleep State Exit latency

Retimer Standard	Specification	Link Requirement	Re-timer Requirement
USB 3.2	Ux_EXIT_TIMER	≤ 6 ms	t13-t11 80 µs – 2 ms[1]
	U1 minimum residency	3 µs	t13-t11 0.9 µs – 1.2 µs[2] (Table 6-31)
USB4	Host determines the number of retimers during initial link training. Host determines if entering CL0s, CL1, CL2, CLd is feasible		tTxShut, < 100 ns (sending CL_Off and shutting down transmitters)
			tIdleRx, ≥ 130 ns (wait after receiving LFPS before starting calibration
			tCLxLock, , ≤ 60 µs (Symbol lock on CLx exit)
			tSwitchSSC, ≤ 60 µs (Clock switch during CLx exit with SSC) tSwitchNoSSC, ≤ 10 µs (Clock switch during CLx exit with no SSC)

1. Four re-timers t13-t11 is 320 µs to 8 ms which exceeds the U2_Exit_Timer. Hosts are recommended to disable U1 and U2 on externally facing ports.
2. Four re-timers t13-t11 is 3.6 µs – 4.8 µs which exceeds the U1 minimum residency. Hosts are recommended to disable U1 and U2 on externally facing ports.

USB 3.2/USB4™ Test Points Definition

Test Point	Description
TP1	Transmitter silicon pad
TP2	Transmitter port mated connector output
TP3	Receiver port mated connector input
TP4	Receiver silicon pad



Alternate Modes (Optional)

- Discovery via USB PD
  - ***Discover SVIDs*** on SOP' only
  - ***Discover Modes*** on SOP' only
- Enter/Exit Mode
  - ***Enter*** and ***Exit*** mode will be communicated on SOP' and on SOP'' when the SOP'' Controller Present bit is set in the Active Cable
- Notes for Alt Mode Operation
  - Maintain the plug's Maximum Skin Temperature below the requirement
  - Recommended to reduce power in sleep states
  - Required to reduce power in USB 3.2 U3 or equivalent (if supported in the Alt Mode)

Active Cable Compliance

- USB PD Level
  - eMarker Response
  - USB PD commands
- VCONN Power
  - Maximum power
  - Suspend power
- Cable Startup and Reset
  - USB 3.2 Default
  - USB4™ Entry
- Fall back modes
- Signal Integrity (if supported)
  - USB 2.0
  - USB 3.2 Gen 1/2
  - USB4 Gen 2/3
  - SBU
- Compliance documents will follow after the Active Cable Specification releases

Mechanical Requirements

- Same as Passive Cables
- Plug Spacing
  - x1 Operation (1 W on VCONN)
    - Active cables support the USB Type-C® vertical and horizontal spacing defined Chapter 3 when functioning in x1 operation
  - x2 Operation (1.5 W on VCONN)
    - However, x2 operation may impose thermal constraints on the spacing
    - Appendix D (USB Type-C Spec) provides system design guidance to minimize the thermal impact due to connector spacing

Products designed for USB4™ and USB 3.2 x2 operation with multiple adjacent USB Type-C connectors need to closely follow guidelines in Appendix D to minimize the likelihood the active cable will go into thermal shutdown.

Thermal Requirements

- Thermal Shutdown
  - When “internal temperature” reaches the “shutdown temperature” (As defined in USB-PD)
    - Disconnect Data
      - USB 3.2 - Goto eSS.Disabled state
      - USB4™ – TBD
  - Thermal shutdown status and internal temperature (°C) is reported in USB PD ***Cable Status***
  - Shut down temperature reported in the USB PD ***Discover Identity***
- Maximum Skin Temperature

Cable Temperature Requirements

Maximum Internal to Skin Temperature Offset	Design specific
Maximum Internal Operating Temperature	Design specific
Maximum Skin Temperature Plastic/Rubber[1]	80 °C
Maximum Skin Temperature Metal[1]	55 °C

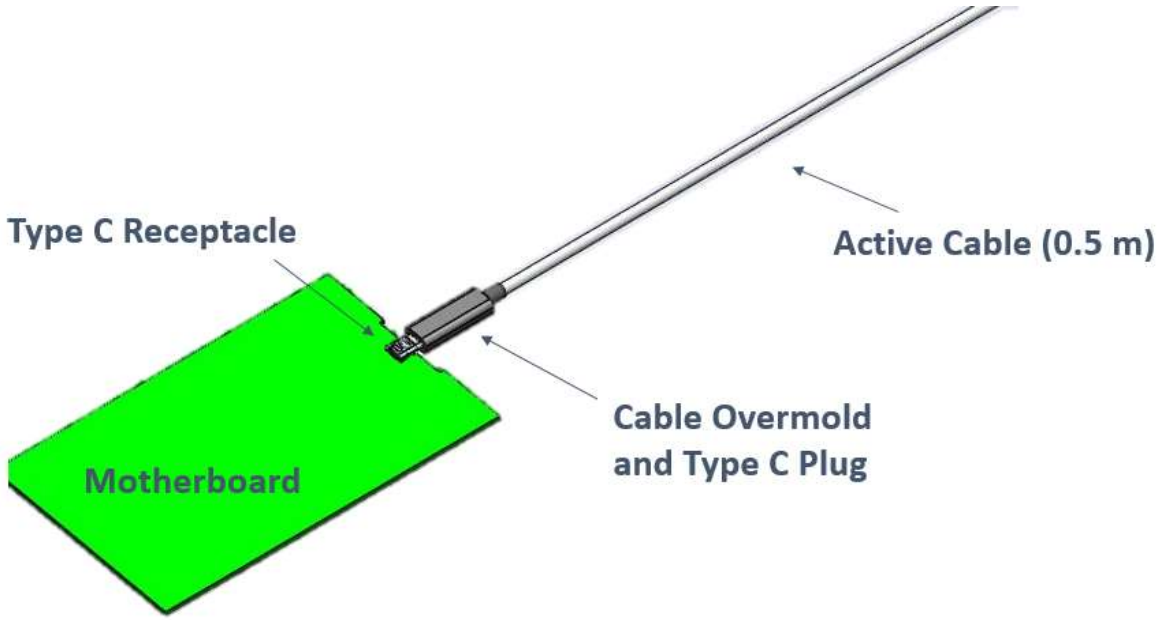
Note 1: IEC 69950-1 reduced by 5 °C

- Cable Status should be reported while in any Alternate Mode and in Thermal Shutdown

Thermal Design Considerations
(Appendix D)

- Provides case studies to show the thermal impacts of certain factors affecting the active cable maximum plug skin temperature
  - IC power
  - V_{BUS} Current
  - Port Spacing
  - Receptacle heat sinking

Active Cable Model (Single Port, Top Mount Receptacle)



Active Cable Thermal Design Considerations

- Design the heat sink of cable to tradeoff flow to the cable plug and IC temperature
- Design for maximum IC Junction temperature
  - This may be lower than the maximum plug skin temperature
- Design to shutdown at a cable plug skin temperature per Table 5-6 or lower
  - Cable vendors should build in margin to the specification
- Active cables may shutdown at lower temperatures that the specification allows

- Passive cables dissipate ~250 mW in the plug at 5 A
- Active x1 cables dissipate ~750 mW in the plug at 5 A (500 mW from electronics)
- Active x2 cables dissipate ~1 W in the plug at 5 A (750 mW from electronics)
- This power has to be dissipated somehow

Single Port Spacing Simulations
(USB4™ / USB3.2 x1)

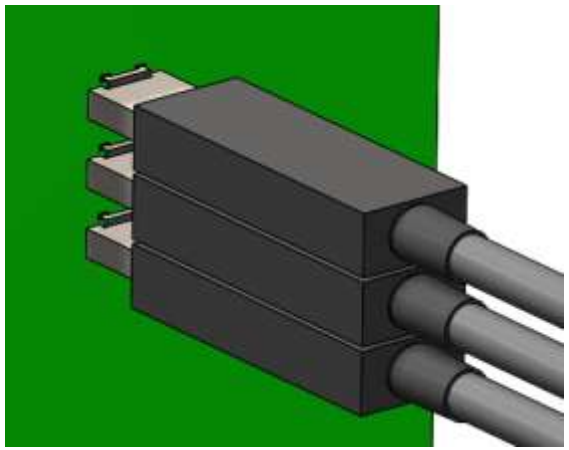
- Assumptions
  - 500 mW power dissipation in each plug from electronics
  - 35 °C Ambient
  - 60 °C Thermal Boundary (motherboard temperature)
  - Plastic housing shell
- Requirements
  - TS (Plug skin temperature) must be less than 30 °C above ambient
- No special design considerations needed if motherboard is 60 °C maximum
- Thermal shutdown occurs by 80 °C TS (plug skin temperature)

	3 A VBUS	5 A VBUS
T_S (°C)	57	60

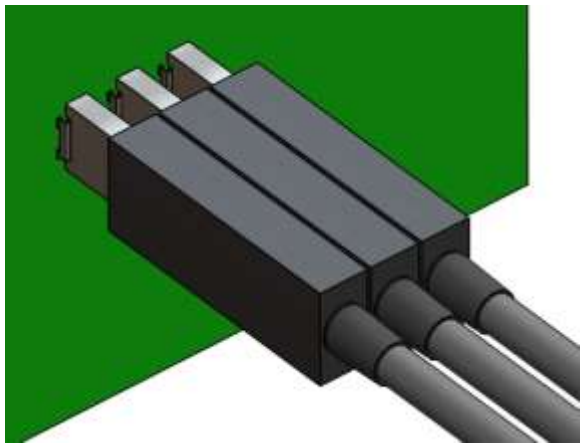
Multi-Port Spacing Considerations

- Heat transfers between cables
- Heat dissipation through natural convection is less effective than in the single port case
- Radiation is less effective than in the single port case
- Center cable plug skin surface temperature is the hottest

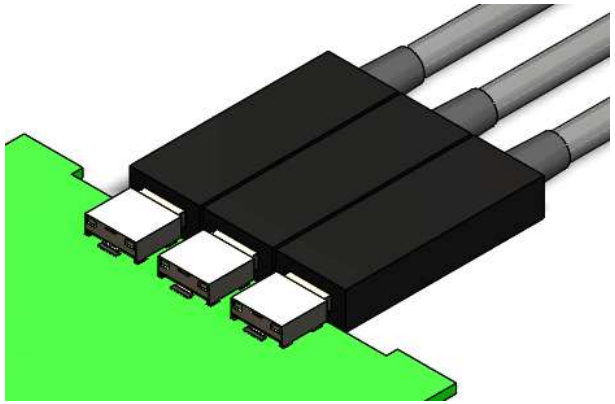
Vertically Stacked Horizontal Connectors 3x1 (VERT)



Horizontally Stacked Vertical Connectors 1x3 (HZ90)



Horizontally Stacked Horizontal Connectors 1x3 (HORZ)

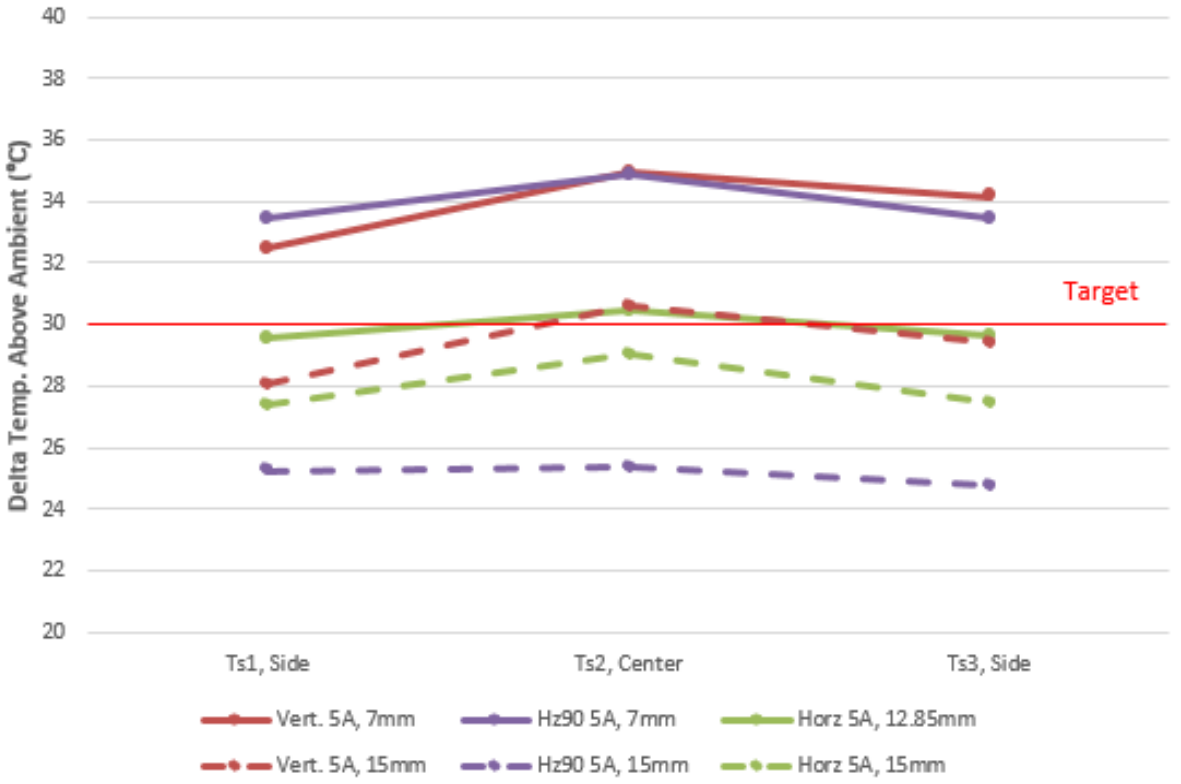


Multi-Port Spacing Simulations
(USB4™ / USB3.2 x1)

- Assumptions
  - 35 °C Ambient, 60 °C Thermal Boundary (motherboard temperature)
  - 500 mW power dissipation in each plug from electronics

USB 3.2 x1 3A Active Cable in 3-port Configuration

USB 3.2 x1 5A Active Cable in 3-port Configuration



Multi-Port Spacing Design Considerations
(USB4™ / USB 3.2 x1)

- 3 A Ports
  - It is possible to maintain the cable TS (plug skin temperature) at 30 °C above ambient at minimum spacing with no special heat spreader or heat sink
  - The board thermal design should be simulated next to the receptacle and a reasonable maximum temperature maintained
- 5 A Ports
  - It is not possible to maintain the cable TS at 30 °C above ambient at minimum spacing in all orientations with no special heat spreader or heat sink in all cases
  - Thermal simulation should be performed and minimum port spacing increased or a heat spreader or heat sink added to the board design
  - The board thermal design should be simulated next to the receptacle and a reasonable maximum temperature maintained

Single Port Spacing Simulations
(USB4™ / USB 3.2 x2)

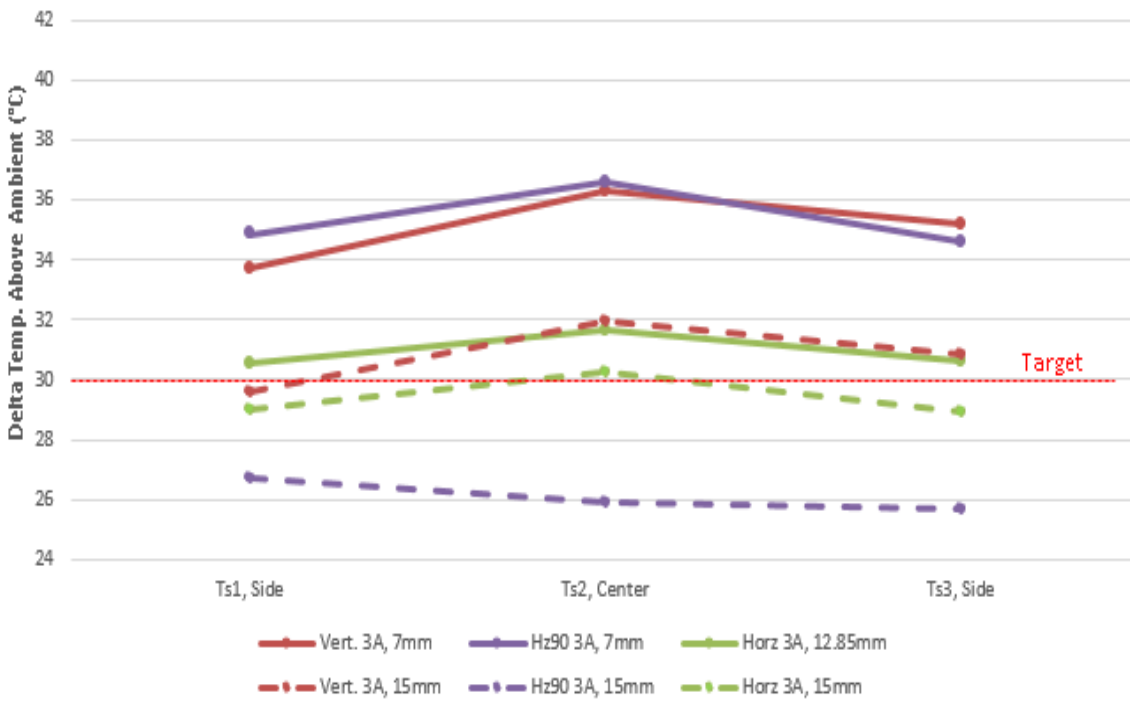
- Assumptions
  - ***750 mW power dissipation*** in each plug from electronics
  - 35 °C Ambient
  - 60 °C Thermal Boundary (motherboard temperature)
- Requirements
  - TS (Plug skin temperature) must be less than 30 °C above ambient
- No special design considerations needed if motherboard is 60 °C maximum
- Recommended that 5 A VBUS designs test and verify thermal designs
- Thermal shutdown occurs by 80 °C TS

	3A VBUS	5A VBUS
T_S (°C)	61	64

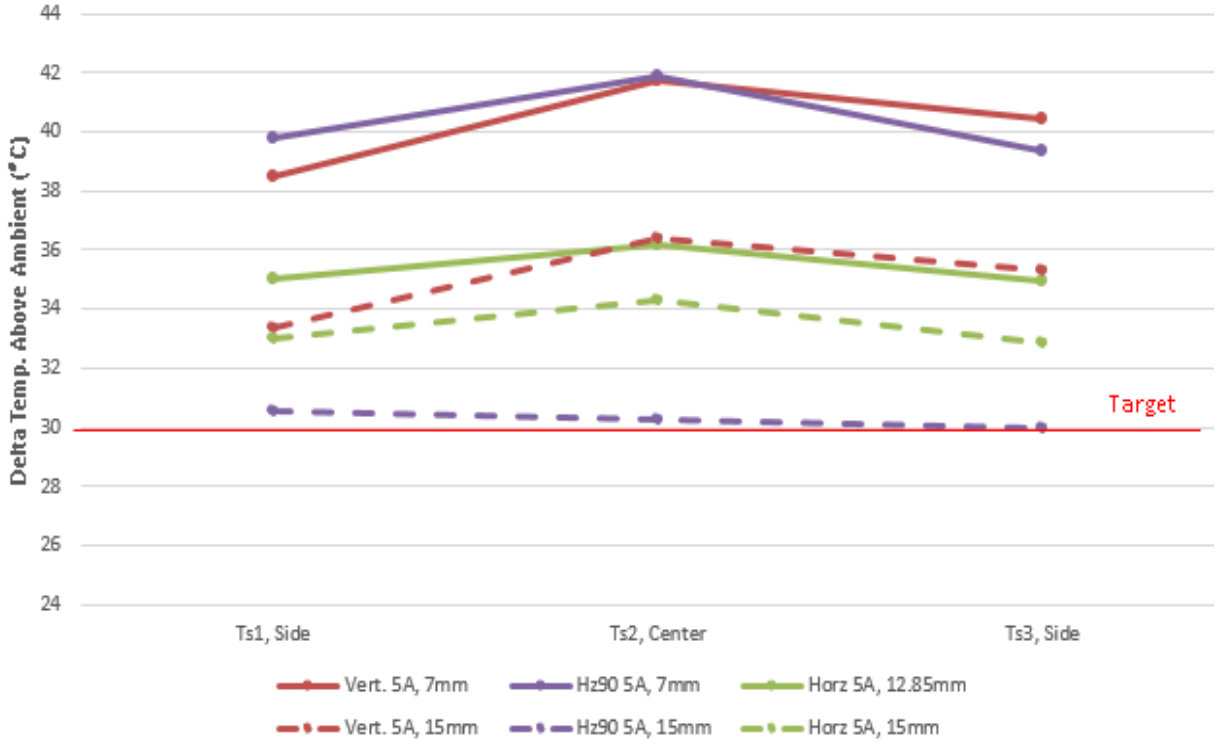
Multi-Port Spacing Results
(USB4™ / USB 3.2 x2)

- Assumptions
  - 35 °C Ambient, 60 °C Thermal Boundary (motherboard temperature)
  - 750 mW power dissipation in each plug from electronics

3A Active Cable in 3-port Configuration



5A Active Cable in 3-port Configuration



Multi-Port Spacing Design Considerations
(USB4™ / USB 3.2 x2)

- 3 A Ports
  - It is not possible to maintain the cable TS at 30 °C above ambient at minimum spacing with no special heat spreader or heat sink
  - Thermal simulation should be performed and minimum port spacing increased or a heat spreader or heat sink added to the board design
  - The board thermal design should be simulated next to the receptacle and a reasonable maximum temperature maintained
- 5 A Ports
  - It is not possible to maintain the cable TS at 30 °C above ambient at minimum spacing with no special heat spreader or heat sink
  - Thermal simulation should be performed and minimum port spacing increased **AND** a heat spreader or heat sink added to the board design
  - The board thermal design should be simulated next to the receptacle and a reasonable maximum temperature maintained

Summary of Design Considerations (Thermal)

Remember that Hosts, Hubs, and Devices do not control the type of cable connected or the ambient temperature

Designers must consider and simulate:

- Port Spacing and orientation
- USB Type-C® Receptacle heat sink, spreader, or cooling
- Motherboard temperature
- V_{BUS} Current per port
- Number of USB 3.2 lanes (x1 or x2)

Eco-System Issues Observed

Bug Type	Description	Status
VCONN	VCONN not supplied in USB3.2 system	Not Compliant
	VCONN current limit too low in Host/Device	Hosts do not go through Compliance Devices may not be checked in Compliance[1]
	VCONN not re-applied supplied after Sleep	Hosts do not go through Compliance Devices may not be checked in Compliance[1]
	Mis-assignment of SOP'/SOP"	Resolved with fixed SOP'/SOP" assignment
	Error Recovery of Sink as Vconn Source	ECR Required for USB Type-C USB4 covered with ***Data Reset***
USB 3.2 Re-timer	Hosts don't understand retimer exit latency in U1/U2	Recommendation Hosts disable U1/U2
	Improper handling of SKP OS	IP updated. Some early IP did not implement the ECN
NOTES:		
1) This will be reviewed to be added in compliance		

Conclusions / Summary

- USB4 Active Cable Spec will be out end of 2019
- Compliance Spec will be out in 2020

- Please comply to the above specifications for best user experience

Time for Q&A

Backup

USB4™ Passive Cable Link Budget

Speed	Total Budget. (dB)	Host (dB)	Cable (dB)	Device (dB)
USB 3.2 Gen1	20	6.5	7	6.5
USB 3.2 Gen2	23	8.5	6	8.5
USB 3.2 Gen2 w/ USB4 Gen2 Host	26	5.5	12	8.5
USB4 Gen2	23	5.5	12	5.5
USB4 Gen3	22.5	7.5	7.5	7.5

USB4™: USB Entry mode

- UFP VDO 1

B27…24	Device Capability	Bit / Description 0 — *[USB 2.0]* Device Capable 1 — *[USB 2.0]* Device Capable (Billboard only) 2 — *[USB 3.2]* Device Capable 3 — *[USB 4.0TM]* Device Capable
B23…6	***Reserved***	***Shall*** be set to zero.
B5…3	Alternate Modes	Bit / Description 0 — Supports *[TBT3]* Alternate Mode 1 — Supports Alternate Modes that reconfigure the signals on the *[USB Type-C® 2.0]* connector – except for *[TBT3]*. 2 — Supports Alternate Modes that do not reconfigure the signals on the *[USB Type-C® 2.0]* connector
B2…0	USB Highest Speed	000b = *[USB 2.0]* only, no SuperSpeed support 001b = *[USB 3.2]* Gen1 010b = *[USB 3.2]*/*[USB 4.0TM]* Gen2 011b = *[USB 4.0TM]* Gen3 100b…111b = ***Reserved***, ***Shall Not*** be used See *[USB Type-C® 2.0]* for definitions.

- DFP VDO

Bit(s)	Field	Description
B31…29	DFP VDO Version	Version Number of the VDO (not this specifica • Version 1.0 = 000b Values 001b…111b are ***Reserved*** and ***Shall N***
B28…27	***Reserved***	***Shall*** be set to zero.
B26…24	Host Capability	Bit / Description 0 — *[USB 2.0]* Host Capable 1 — *[USB 3.2]* Host Capable 2 — *[USB 4.0TM]* Host Capable
B23…5	***Reserved***	***Shall*** be set to zero.
B4…0	Port Number	Unique port number to identify a specific por

- UFP VDO 2

Bit(s)	Field	Description
B31…30	***Reserved***	***Shall*** be set to zero.
B29…23	USB4 Min Power	Minimum power in watts required to function in *[USB 4.0TM]* operation.
B22…16	USB4 Max Power	Power in watts required for full functionality excluding any power required for battery charging or for redistribution in *[USB 4.0TM]* operation.
B15…14	***Reserved***	***Shall*** be set to zero.
B13…7	USB3 Min Power	Minimum power in watts required to function in *[USB 3.2]* operation.
B6…0	USB3 Max Power	Power in watts required for full functionality excluding any power required for battery charging or for redistribution in *[USB 3.2]* operation.

USB 3.2 Power-on and Rx.Detect

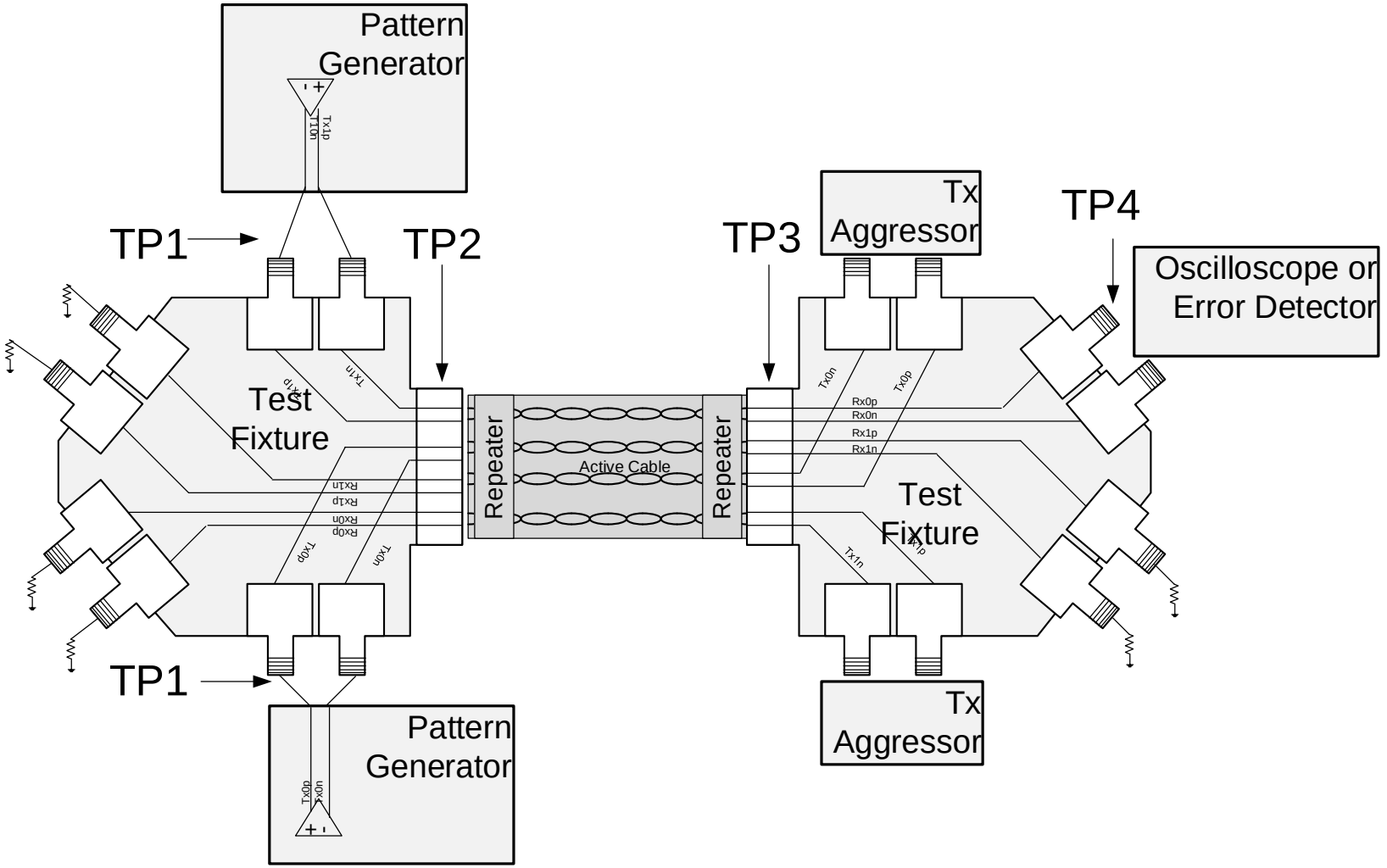
- Active cables perform far-end receiver termination detection (USB 3.2 Appendix E)
- An active cable complete power-on and far-end receiver termination detection through the cable within tFWD_RX.DETECT

Table 5-8 Active Cable Power-on Requirements

Parameter	Minimum	Maximum	Units
ZRX-HIGH-IMP-DC-POS	per USB 3.2	per USB 3.2	
RRX-DC	per USB 3.2	per USB 3.2	
tFWD-RX.DETECT		42	ms

USB 3.2 Compliance Test Setup

Figure 5-8 SuperSpeed Compliance Test Setup



USB 3.2 TP1 (5.2.5.4.6.1)

- Normative (set at the pattern generator for compliance testing) – Subset of the USB 3.2 Spec

Table 5-11 Active Cable USB 3.2 Stressed Source Swing, TP1

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX-DE-RATIO}$	Tx de-emphasis	USB 3.2 Table 6-17	−3.1+/-1.0	dB	Nominal is 3.5 dB for Gen 1 operation. Gen 2 transmitter equalization requirements are described in USB 3.2 Section 6.7.5.2.
$V_{PRESHOOT}$	Tx Preshoot	USB 3.2 Table 6-17	2.2+/-1.0	dB	Gen 2 transmitter equalization requirements are described in USB 3.2 Section 6.7.5.2.

Table 5-12 Active Cable USB 3.2 Stressed Source Jitter, TP1 (Same as USB 3.2)

Symbol	Parameter	Gen 1 (5GT/s)	Gen 2 (10GT/s)	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.0100	UI rms	1
J_{Rj_p-p}	Random Jitter peak- peak at 10^{-12}	0.17	0.14	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3

USB 3.2 TP2 (5.2.5.4.6.2)

- Informative (used to check the stressed signal for active cable JTOL testing)
- Design guidance for active cable input receiver

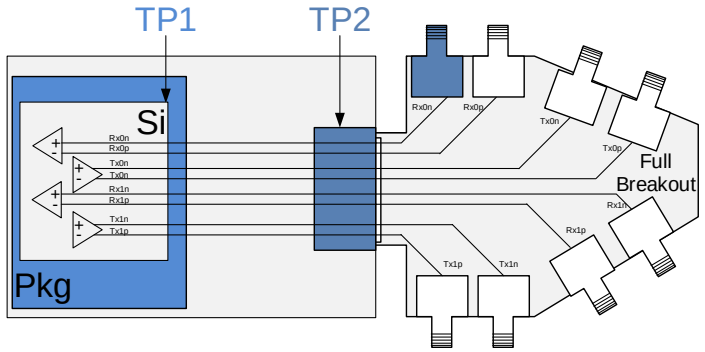


Table 5-13 Active Cable USB 3.2 Input Swing at TP2 (Informative)

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	250 (min) 1000 (max)	250 (min) 850 (max)	mV	Nominal is 550mV p-p
$V_{TX-DE-RATIO}$	Tx de-emphasis	0 (min) 4.0 (max)	2.1 (min) 4.1 (max)	dB	There is no de-emphasis requirement for Gen1.
$V_{PRESHOOT}$	Tx Preshoot	NA	1.2 (min) 3.2 (max)	dB	Applicable to USB3.2 Gen2 operation only

USB 3.2 TP3 (5.2.5.4.6.3)

- Informative (not used for compliance testing)
- Design guidance for active cable output driver
- No De-emphasis required

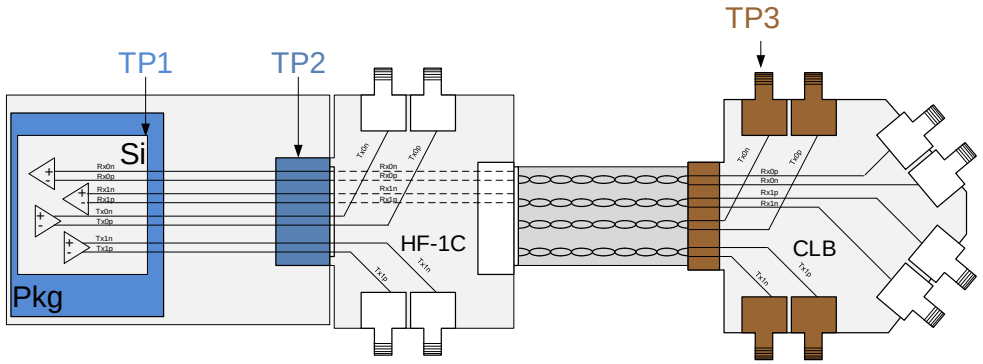


Table 5-14 Active Cable USB 3.2 Output Swing at TP3 (Informative)

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
$V_{RX-DIFF-PP-POST-EQ}$	Differential Rx peak-to-peak voltage	300 (min) 850 (max)	300 (min) 850 (max)	mV	Measured after the Rx EQ function (Section 6.8.2). Nominal is 0.5 V p-p
$V_{TX-DE-RATIO-GEN1}$	Tx de-emphasis	0 (min) 4.0 (max)	NA	dB	No preshoot allowed
$V_{TX-DE-RATIO}$ + $V_{PRESHOOT-GEN2}$	Tx de-emphasis + Tx Preshoot	NA	0 (min) 3.0 (max)	dB	Sum of the de-emphasis and preshoot. There is no de-emphasis and pre-shoot requirement.

USB 3.2 TP4 (5.2.5.4.6.4)

- Normative (tested in compliance)
- The active cable transmitter output is defined at TP4 for both high and low loss channels
  - The requirements for TP4 are defined in the USB3.2 specification Table 6-20
  - The input signal for the test will be applied at TP1 per Section 5.2.5.4.6.1
- The low loss test board will be used to test the maximum output swing
  - The maximum loss test board will be used to test the minimum output swing. Jitter must be met with both test boards
- The active cable bit-error-rate will be tested at TP4 and meet or exceed a BER of 10-12
  - The error detector used will have the ability to remove SKP ordered sets

USB3.2 Test Points: TP4 (Rx Silicon Pad)

- Used for Tx eye measurement
  - Eye height
  - TJ (using RJ measured @ TP3)
- In practice, signal is measured @ TP3
  - Compliance board is embedded by Sigtest.