USB PD CTS ENGINEERING CHANGE NOTICE FORM

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Title: xxxx
Applied to: USB PD CTS Specification Version 1.0 Revision 1

Brief description of the functional changes proposed:
The parameter tPSTransition max is used in several Power Supply tests where the correct parameter is tPSTransition min. There are in fact a total of approximately 22 places in the document that incorrectly refer to tPSTransition max instead of tPSTransition min. "The PSTransitionTimer is used by the Policy Engine to timeout on a PS_RDY Message."

Benefits as a result of the proposed changes:

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

An analysis of the hardware implications:

An analysis of the software implications:

An analysis of the compliance testing implications:

An analysis of the Vendor Info File (VIF) implications:

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Actual Change Requested

Changes in red

There are in fact a total of approximately 22 places in the document that incorrectly refer to tPSTransition max instead of tPSTransition min. Only 6 cases are shown here.

To Text:

TEST.PD.PS.SRC.1 Multiple Request Load Test

Description: As a Sink only, the Tester verifies that the Source UUT responds correctly to various Request messages.
Test Specific Tester Behavior: N/A
Test Conditions:

	Consumer Only, C/P	Provider Only, P/C, DRP
Rev2Src		✓
Rev3ChkdSrc		✓

Test Requirements: If Captive_Cable = YES, **vSrcNew min** or **vPpsNew min** limit shall be (vSrcNew min) - (0.75*I/X) or (vPpsNew min) - (0.75*I/X), where I is the actual current being drawn, and X=3 if the sourced PDO contract is within the range (0, 3A], or X=5 if the sourced PDO contract is within the range (3A, 5A)

Test Procedures:

1. The Tester runs bring-up procedure with the UUT as a Source COMMON.BU.PD.1.
2. The Tester repeats the following steps for each of the PDOs (in the Source Capabilities message), starting with the first PDO:
    a. If the next Request will be for a PPS transition involving a current decrease (but no PDO change), the Tester reduces its current draw to the new level required, before sending the Request. (This avoids the current limit in the UUT shutting off VBUS.) The Tester draws the requested Operating Current / Power with a current transition slew rate of 100mA per µs. The Tester monitors VBUS voltage and the check fails if VBUS voltage is not within the limits of PpsNew. [TEST.PD.PS.SRC.1#9]
    b. The Tester sends a Request message.
        i. B27 (GiveBack Flag) = 0b
        ii. B26 (Capability Mismatch) = 0b
        iii. B25 (USB Communication Capable) = 0b
        iv. B24 (No USB Suspend) = 1b
        v. For Fixed, Battery or Variable PDO:
            1. B19…10 (Operating Current / Power):
                a. For first Request: 0mA/0mW

b. For subsequent Request: As defined in Step 2.f.i

2. B9…0 (Maximum Operating Current / Power) = Maximum Current / Power in the Source PDO.

vi. For PPS:

1. B19…9 (Output Voltage) = Maximum Voltage offered in Source APDO

2. B6…0 (Operating Current):

a. For first Request: 1A

b. For subsequent Request: As defined in Step 2.f.II

The initial Request is for PDO #1 (5V Fixed) at 0mA. The complete list of Requests is defined in step 2.f.

c. The check fails if an Accept message is not received. [TEST.PD.PS.SRC.1#10]

d. The check fails if PS_RDY message is not received within tPSTransition min ~~max~~ from the last bit of the EOP of Accept message. [TEST.PD.PS.SRC.1#11]

e. The Tester performs the following checks:

i. If the transition involves a current decrease (but no PDO change) [TEST.PD.PS.SRC.1#1]

1. **For Fixed, Battery or Variable PDOs**:
The Tester decreases current to the new value within tSnkNewPower min of the last bit of the GoodCRC sent in response to the Accept message. The Tester draws the requested Operating Current / Power with a current transition slew rate of 100mA per µs. The Tester monitors VBUS voltage and the check fails if VBUS voltage is not within the limits of vSrcNew.

2. **For PPS**:
The current was already reduced in step 2.a.

ii. If the transition involves a current increase (but no PDO change), the Tester increases current to the new value after the last bit of the GoodCRC sent in response to the PS_RDY message. The Tester draws the requested Operating Current / Power with a current transition slew rate of 100mA per µs. The Tester monitors VBUS voltage and the check fails if VBUS voltage is not within the limits of vSrcNew or vPpsNew. [TEST.PD.PS.SRC.1#2]

iii. If the transition involves a change of PDO, decrease the power drawn by the Tester to less than pSnkStdby within tSnkStdby of the last bit of the GoodCRC sent in response to the Accept message. The Tester performs the following checks:

1. The Tester checks that VBUS remains within vSrcNew or vPpsNew of the starting voltage within tSrcTransition min after the end of the GoodCRC sent in response to the Accept message. [TEST.PD.PS.SRC.1#3]

2. The Tester checks that the VBUS transition meets vSrcSlewPos and vSrcSlewNeg. [TEST.PD.PS.SRC.1#4]

3. During the voltage transition, the Tester checks that the VBUS voltage remains within vSrcValid limits from the time of crossing into the vSrcValid limits until tSrcSettle max. [TEST.PD.PS.SRC.1#5]

4. The Tester checks that the VBUS voltage remains within vSrcNew or vPpsNew limits between tSrcSettle max and 100ms after tSrcSettle max. [TEST.PD.PS.SRC.1#6]
5. The Tester checks that the UUT does not send PS_RDY before VBUS is within vSrcNew or vPpsNew. [TEST.PD.PS.SRC.1#7]
6. After having sent GoodCRC in response to PS_RDY, the Tester increases its current draw to:
    a. For Fixed, Battery and Variable PDOs:

        The current or power requested.
    b. For PPS PDO:

        80% of the current requested (except that for the last step 0mA will be drawn.

    The Tester checks that the VBUS voltage remains within vSrcNew or vPpsNew limits for 100ms after receivingPS_RDY[TEST.PD.PS.SRC.1#8]

f. The Tester repeats Step-2a to Step-2e, replacing the appropriate fields with the next value from the following list. The Tester sends 9 separate Request messages for each PDO (7 separate Request messages for PPS):

    i. For Fixed, Battery and Variable PDOs, replace B19…10 (Operating Current / Power):

        1. 0mA / 0mW [performed in Step 2.b; listed here for reference only]
        2. 25% of Maximum Current / Power in the Source PDO
        3. 50% of Maximum Current / Power in the Source PDO
        4. 75% of Maximum Current / Power in the Source PDO
        5. 100% of Maximum Current / Power in the Source PDO
        6. 75% of Maximum Current / Power in the Source PDO
        7. 50% of Maximum Current / Power in the Source PDO
        8. 25% of Maximum Current / Power in the Source PDO
        9. 0mA / 0mW

    ii. For PPS PDO, replace B19..9 (Output Voltage) and B6…0 (Operating Current):

        1. Maximum Voltage offered in Source APDO @ 1A (Tester will draw 0mA) [performed in Step 2.b; listed here for reference only]
        2. Maximum Voltage offered in Source APDO @ 1A (Tester will draw 80% of this.)
        3. Maximum Voltage offered in Source APDO @ (1A + Maximum Current offered in Source APDO)/2. (Tester will draw 80% of this.)
        4. Maximum Voltage offered in Source APDO @ Maximum Current offered in Source APDO. (Tester will draw 80% of this.)
        5. Maximum Voltage offered in Source APDO @ (1A + Maximum Current offered in Source APDO)/2. (Tester will draw 80% of this.)
        6. Maximum Voltage offered in Source APDO @ 1A (Tester will draw 80% of this)
        7. Maximum Voltage offered in Source APDO @ 1A (Tester will draw 0mA)

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TEST.PD.PS.SRC.2 PDO Transitions

Description: As a Sink only, the Tester enumerates all possible transitions among the PDOs of the UUT and verifies the UUT performs PDO transitions correctly.
Test Specific Tester Behavior: N/A
Test Conditions:

	Consumer Only, C/P	Provider Only, P/C, DRP
Rev2Src		✓
Rev3ChkdSrc		✓

Test Procedures:

1. The Tester runs bring-up procedure with the UUT as a Source COMMON.BU.PD.1.
2. The Tester repeats the following steps using the PDO as provided in the **PDO Sequence Table**:
    a. The Tester sends a Request message:
        i. B27 (GiveBack Flag) = 0b
        ii. B26 (Capability Mismatch) = 0b
        iii. B25 (USB Communication Capable) = 0b
        iv. B24 (No USB Suspend) = 1b
        v. For Fixed, Battery or Variable PDO:

            B19…10 (Operating Current / Power) = 100mA / 0.5W
            B9…0 (Maximum Operating Current / Power) = 100mA / 0.5W

        For PPS PDO:

            B19…9 (Output Voltage) = Maximum Voltage offered in Source APDO
            B7…0 (Operating Current) = 1A

    b. The check fails if an Accept message is not received. [TEST.PD.PS.SRC.2#1]
    c. The check fails if PS_RDY message is not received within tPSTransition ~~max~~ min from the last bit of the EOP of Accept message. [TEST.PD.PS.SRC.2#2]
    d. The Tester performs the following checks:

    Decrease the power drawn by the Tester to less than pSnkStdby within tSnkStdby min of the last bit of the GoodCRC sent in response to the Accept message. The Tester performs the following checks:

        1. The Tester checks the VBUS is within vSrcNew of the starting voltage within tSrcTransition min after the end of the GoodCRC sent in response to the Accept message. [TEST.PD.PS.SRC.2#3]
        2. The Tester checks that the VBUS transition meets vSrcSlewPos and vSrcSlewNeg. [TEST.PD.PS.SRC.2#4]
        3. During the voltage transition, the Tester checks that the VBUS voltage remains within vSrcValid limits from the time of crossing into the vSrcValid limits until tSrcSettle max. [TEST.PD.PS.SRC.2#5]
        4. The Tester checks that the VBUS voltage is within vSrcNew limits between tSrcSettle max and 100ms after tSrcSettle max. [TEST.PD.PS.SRC.2#6]
        5. The Tester checks that the UUT does not send PS_RDY before the VBUS is within vSrcNew. [TEST.PD.PS.SRC.2#7]

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TEST.PD.PS.SNK.2 Initial Sink PDO Transitions Post PR Swap

Description: The Tester verifies that the new Source UUT performs PDO transitions correctly.
Test Specific Tester Behavior:

- The Tester is a Dual-Role Power, initially a Source
- The Tester sends Sink Capabilities setting B27 (Unconstrained Power) to 0b COMMON.PROC.PD.3

Test Conditions:

	Consumer Only, C/P, DRP	Provider Only, P/C
Rev2Snk	✓	
Rev3ChkdSnk	✓	

Test Procedures:

1. The Tester runs bring-up procedure with the UUT as a Sink COMMON.PROC.BU.2
2. After this point the tester should reject any PR_swap request.
3. The Tester sends a PR_Swap message.
4. The Tester checks the response: [TEST.PD.PS.SNK.2#1]
    a. The check fails if the UUT responds with a Reject message or Not_Supported, and the VIF field Accepts_PR_Swap_As_Snk is "Yes".
    b. The test ends here if the UUT responds with a Reject message or Not_Supported.
    c. If the UUT responds with a Wait message, the Tester resends PR_Swap every tPRSwapWait + 15ms for 10 times. Once the Tester has repeated for 10 times, the check fails, and the test ends here.
    d. If the UUT responds with an Accept message, the Tester checks that the VIF field PD_Port_Type is set to either "Consumer/Provider" or "DRP".
    e. If the UUT responds with an Accept message, the Tester checks that the VIF field Accepts_PR_Swap_As_Snk is "Yes".
5. At tSrcTransition max (this delay is from the last bit of GoodCRC sent in response to the Accept), the Tester drives the VBUS voltage to vSafe0V within tSrcSwapStdby max.
6. The Tester sends a PS_RDY at the deadline limit of tPSSourceOff min, the delay is from the time the last bit of the EOP of the GoodCRC corresponding to the Accept message.
7. The Tester checks that the UUT sends PS_RDY only after the UUT has applied vSafe5V. [TEST.PD.PS.SNK.2#2]
8. The Tester checks that the PS_RDY from the UUT is within tNewSrc max, this delay is from the GoodCRC sent by the UUT in response to the PS_RDY sent by the Tester. [TEST.PD.PS.SNK.2#3]
9. Once the Tester receives Source Capabilities message, the Tester establishes a PD contract using common procedure COMMON.PROC.PD.11.
10. After this point the Tester shall Reject any PR_Swap request received.
11. The Tester repeats the following steps using the PDO as provided in the **PDO Sequence Table**:
    a. The Tester sends a Request message:
        i. B27 (GiveBack Flag) = 0b
        ii. B26 (Capability Mismatch) = 0b
        iii. B25 (USB Communication Capable) = 0b
        iv. B24 (No USB Suspend) = 1b
        v. B19…10 (Operating Current / Power) = 100mA / 0.5W

vi. B9…0 (Maximum Operating Current / Power) = Maximum Current / Power in the Source PDO.

b. The check fails if the UUT does not respond with an Accept message. [TEST.PD.PS.SNK.2#4]

c. The check fails if PS_RDY message is not received within tPSTransition min ~~max~~ from the last bit of the EOP of Accept message. [TEST.PD.PS.SNK.2#5]

d. The Tester performs the following checks:

Decrease the power drawn by the Tester to less than pSnkStdby within tSnkStdby min of the last bit of the GoodCRC sent in response to the Accept message. The Tester performs the following checks:

1. The Tester checks the VBUS is within vSrcNew of the starting voltage within tSrcTransition min after the end of the GoodCRC sent in response to the Accept message. [TEST.PD.PS.SNK.2#6]

2. The Tester checks that the VBUS transition meets vSrcSlewPos and vSrcSlewNeg. [TEST.PD.PS.SNK.2#7]

3. During the voltage transition, the Tester checks that the VBUS voltage remains within vSrcValid limits upon crossing into the vSrcValid limits until tSrcSettle max. [TEST.PD.PS.SNK.2#8]

4. The Tester checks that the VBUS voltage is within vSrcNew limits between tSrcSettle max and 100ms after tSrcSettle max. [TEST.PD.PS.SNK.2#9]

5. The Tester checks that the UUT does not send PS_RDY before the VBUS is within vSrcNew. [TEST.PD.PS.SNK.2#10]

TEST.PD.PS.SNK.3 Multiple Request Load Test Post PR Swap

Description: The Tester verifies that the new Source UUT responds correctly to various Request messages.
Test Specific Tester Behavior:

- The Tester is a Dual-Role Power, initially a Source
- The Tester sends Sink Capabilities setting B27 (Unconstrained Power) to 0b COMMON.PROC.PD.3

Test Conditions:

	C/P, DRP	Consumer Only, Provider Only, P/C
Rev2Snk	✓	
Rev3ChkdSnk	✓	

Test Requirements: If Captive_Cable = YES, **vSrcNew min** or **vPpsNew min** limit shall be (vSrcNew min) - (0.75*I/X) or (vPpsNew min) - (0.75*I/X), where I is the actual current being drawn, and X=3 if the sourced PDO contract is within the range (0, 3A], or X=5 if the sourced PDO contract is within the range (3A, 5A)
Test Procedures:

1. The Tester runs bring-up procedure with the UUT as a Sink COMMON.PROC.BU.2
2. The Tester sends a PR_Swap message.
3. The Tester checks the response: [TEST.PD.PS.SNK.3#1]

a. The check fails if the UUT responds with a Reject message or Not_Supported, and the VIF field Accepts_PR_Swap_As_Snk is “Yes”.
b. The test ends here if the UUT responds with a Reject message or Not_Supported .
c. If the UUT responds with a Wait message, the Tester resends PR_Swap every tPRSwapWait + 15ms for 10 times. Once the Tester has repeated for 10 times, the check fails, and the test ends here.
d. If the UUT responds with an Accept message, the Tester checks that the VIF field PD_Port_Type is set to either “Consumer/Provider” or “DRP”.
e. If the UUT responds with an Accept message, the Tester checks that the VIF field Accepts_PR_Swap_As_Snk is “Yes”.

4. At tSinkTransition max (this delay is from the last bit of GoodCRC sent in response to the Accept), the Tester drives the VBUS voltage to vSafe0V within tSrcSwapStdby max.
5. The Tester sends a PS_RDY at the deadline limit of tPSSourceOff min, the delay is from the time the last bit of the EOP of the GoodCRC corresponding to the Accept message.
6. The Tester checks that the UUT sends PS_RDY only after the UUT has applied vSafe5V. [TEST.PD.PS.SNK.3#2]
7. The Tester checks that the PS_RDY from the UUT is within tNewSrc max, this delay is from the GoodCRC sent by the UUT in response to the PS_RDY sent by the Tester. [TEST.PD.PS.SNK.3#3]
8. Once the Tester receives Source Capabilities message, the Tester establishes a PD contract using common procedure COMMON.PROC.PD.11.
9. After this point the Tester shall Reject any PR_Swap request received.
10. The Tester repeats the following steps for each of the PDOs (in the Source Capabilities message), starting with the first PDO:

    a. If the next Request will be for a PPS transition involving a current decrease (but no PDO change), the Tester reduces its current draw to the new level required, before sending the Request. (This avoids the current limit in the UUT shutting off VBUS.) The Tester draws the requested Operating Current / Power with a current transition slew rate of 100mA per µs. The Tester monitors VBUS voltage and the check fails if VBUS voltage is not within the limits of PpsNew. [TEST.PD.PS.SNK.3#4]

    b. The Tester sends a Request message:

        i. B27 (GiveBack Flag) = 0b

        ii. B26 (Capability Mismatch) = 0b

        iii. B25 (USB Communication Capable) = 0b

        iv. B24 (No USB Suspend) = 1b

        v. For Fixed, Battery or Variable PDO:

            1. B19…10 (Operating Current / Power):

                a. For first Request: 0mA/0mW

                b. For subsequent Requests: As defined in Step 10.f.i

            2. B9…0 (Maximum Operating Current / Power) = Maximum Current / Power in the Source PDO.

        vi. For PPS:

            1. B19…9 (Output Voltage) = Maximum Voltage offered in Source APDO

            2. B6…0 (Operating Current):

a. For first Request: 1A

b. For subsequent Requests: As defined in Step 10.f.ii.

The initial Request is for PDO #1 (5V Fixed) at 0mA. Further requests are defined in step 10f.

c. The check fails if an Accept message is not received. [TEST.PD.PS.SNK.3#12]
d. The check fails if PS_RDY message is not received within tPSTransition min ~~max~~ from the last bit of the EOP of Accept message. [TEST.PD.PS.SNK.3#13]
e. The Tester performs the following checks:

i. If the transition involves a current decrease (but no PDO change) [TEST.PD.PS.SNK.3#4]

1. **For Fixed, Battery or Variable PDOs**:
The Tester decreases current to the new value within tSnkNewPower min of the last bit of the GoodCRC sent in response to the Accept message. The Tester draws the requested Operating Current / Power with a current transition slew rate of 100mA per µs. The Tester monitors VBUS voltage and the check fails if VBUS voltage is not within the limits of vSrcNew.

2. **For PPS**:
The current was already reduced in step 10a.

ii. If the transition involves a current increase (but no PDO change), the Tester increase current to the new value after the last bit of the GoodCRC sent in response to the PS_RDY message. The Tester draws the requested Operating Current / Power with a current transition slew rate of 100mA per µs. The Tester monitors VBUS voltage and the check fails if VBUS voltage is not within the limits of vSrcNew or vPpsNew. [TEST.PD.PS.SNK.3#5]

iii. If the transition involves a change of PDO, decrease the power drawn by the Tester to less than pSnkStdby within tSnkStdby min of the last bit of the GoodCRC sent in response to the Accept message. The Tester performs the following checks:

1. The Tester checks that VBUS remains within vSrcNew or vPpsNew of the starting voltage within tSrcTransition min after the end of the GoodCRC sent in response to the Accept message. [TEST.PD.PS.SNK.3#6]

2. The Tester checks that the VBUS transition meets vSrcSlewPos and vSrcSlewNeg. [TEST.PD.PS.SNK.3#7]

3. During the voltage transition, the Tester checks that the VBUS voltage remains within vSrcValid limits from the time of crossing into the vSrcValid limits until tSrcSettle max. [TEST.PD.PS.SNK.3#8]

4. The Tester checks that the VBUS voltage remains within vSrcNew or vPpsNew limits between tSrcSettle max and 100ms after tSrcSettle max. [TEST.PD.PS.SNK.3#9]

5. The Tester checks that the UUT does not send PS_RDY before the VBUS is within vSrcNew or vPpsNew. [TEST.PD.PS.SNK.3#10]

6. After having sent GoodCRC in response to PS_RDY, the Tester increases its current draw to:

a. For Fixed, Battery and Variable PDOs: the current or power requested

b. For PPS PDO: 80% of the current requested (except that for the last step 0mA will be drawn)

7. The Tester checks that the VBUS voltage remains within vSrcNew or vPpsNew limits for 100ms after receiving PS_RDY.

[TEST.PD.PS.SNK.3#11]

f. The Tester repeats Step-10a through Step-10d, **replacing** The appropriate fields with the next value from the following list. The Tester sends 9 separate Request messages for each PDO (6 separate Request messages for PPS):

i. For Fixed, Battery and Variable PDOs, replace B19…10 (Operating Current / Power):

1. 0mA / 0mW [performed in Step 10.b; listed here for reference only]
2. 25% of Maximum Current / Power in the Source PDO
3. 50% of Maximum Current / Power in the Source PDO
4. 75% of Maximum Current / Power in the Source PDO
5. 100% of Maximum Current / Power in the Source PDO
6. 75% of Maximum Current / Power in the Source PDO
7. 50% of Maximum Current / Power in the Source PDO
8. 25% of Maximum Current / Power in the Source PDO
9. 0mA / 0mW

ii. For PPS PDO, replace B19…9 (Output Voltage) and B6…0 (Operating Current):

1. Maximum Voltage offered in Source APDO @ 1A (Tester will draw 0mA) [performed in Step 10.b; listed here for reference only]
2. Maximum Voltage offered in Source APDO @ 1A. (Tester draws 80% load)
3. Maximum Voltage offered in Source APDO @ (1A + Maximum Current offered in Source APDO)/2. (Tester draws 80% load)
4. Maximum Voltage offered in Source APDO @ Maximum Current offered in Source APDO. (Tester draws 80% load)
5. Maximum Voltage offered in Source APDO @ (1A + Maximum Current offered in Source APDO)/2. (Tester draws 80% load)
6. Maximum Voltage offered in Source APDO @ 1A (Tester draws 80% load)
7. Maximum Voltage offered in Source APDO @ 1A (Tester draws 0mA)

TEST.PD.PS.EPR.SRC3.1 Multiple EPR Request Load Test

Description: As a Sink only, the Tester verifies that the Source UUT responds correctly to various EPR_Request messages.
Test Specific Tester Behavior:
Test Conditions:

This test is applicable if the VIF parameter EPR_Supported_*As_Src* is set to Yes.

	Consumer Only	Provider Only, P/C, C/P, DRP
Rev3ChkdSrc		✓

Test Requirements: If Captive_Cable = YES, **vSrcNew min** or **vAvsNew min** limit shall be (vSrcNew min) - (0.75*I/X) or (vAvsNew min) - (0.75*I/X), where I is the actual current being drawn, and X=3 if the sourced PDO contract is within the range (0, 3A], or X=5 if the sourced PDO contract is within the range (3A, 5A)

Test Procedures:

1. There are 2 possible bring-up procedures:
    a. The UUT has VIF field PD_Port_Type set to Consumer/Provider, the Tester runs bring-up procedure with the UUT as a Source COMMON.PROC.BU.7.
    b. The UUT has VIF field PD_Port_Type set to anything else, the Tester runs bring-up procedure with the UUT as a Source COMMON.PROC.BU.1.
2. The check fails if the "EPR mode capable" field is set to 0 in the Source Capabilities message sent by UUT during the bring up procedure and the test stops here. [TEST.PD.PS.EPR.SRC3.1#1]
3. The Tester sends an EPR_Mode (Enter) message with the Action field set to 0x01(Enter) and Data field set to 140 (140W) and enters EPR mode using common procedure COMMON.PROC.PD3.5. [TEST.PD.PS.EPR.SRC3.1#2]
4. The Tester repeats the following steps for each of the EPR_PDOs only (in the EPR_Source Capabilities message), starting with the 8th PDO:
    a. The Tester sends an EPR_Request message.
        i. B27 (GiveBack Flag) = 0b
        ii. B26 (Capability Mismatch) = 0b
        iii. B25 (USB Communication Capable) = 0b
        iv. B24 (No USB Suspend) = 1b
        v. B22 (EPR Mode Capable) = 1b
        vi. For Fixed PDO:
            1. B19…10 (Operating Current):
                a. For first EPR_Request: 0mA
                b. For subsequent Request: As defined in Step 4.f.i
            2. B9…0 (Maximum Operating Current) = Maximum Current in the Source PDO.
        vii. For EPR AVS APDO:
            1. B20…9 (Output Voltage) = Maximum Voltage offered in Source APDO
            2. B6…0 (Operating Current):
                a. For first EPR_Request: 0mA
                b. For subsequent Request: As defined in Step 4.e.i

The initial EPR_Request is for PDO #8 (28V Fixed) at 0mA. The complete list of EPR_Request is defined in step 4.e.

b. The check fails if an Accept message is not received. [TEST.PD.PS.SRC.1#11]
c. The check fails if PS_RDY message is not received within tPSTransition min ~~max~~ from the last bit of the EOP of Accept message. [TEST.PD.PS.SRC.1#12]
d. The Tester performs the following checks:

    i. If the transition involves a current decrease (but no PDO change), the Tester decreases current to the new value within tSnkNewPower min of the last bit of the GoodCRC sent in response to the Accept message. The Tester draws the requested Operating Current with a current transition slew rate of 100mA per µs. The Tester monitors VBUS voltage and the check fails if VBUS voltage is not within the limits of vSrcNew or vAvsNew. [TEST.PD.PS.EPR.SRC3.1#3]

    ii. If the transition involves a current increase (but no PDO change), the Tester increases current to the new value after the last bit of the GoodCRC sent in response to the PS_RDY message. The Tester draws the requested Operating Current with a current transition slew rate of 100mA per µs. The Tester monitors VBUS voltage and the check fails if VBUS voltage is not within the limits of vSrcNew or vAvsNew. [TEST.PD.PS.EPR.SRC3.1#4]

    iii. If the transition involves a change of PDO, decrease the power drawn by the Tester to less than pSnkStdby within tSnkStdby of the last bit of the GoodCRC sent in response to the Accept message. The Tester performs the following checks:

        1. The Tester checks that VBUS remains within vSrcNew or vAvsNew of the starting voltage within tSrcTransition min after the end of the GoodCRC sent in response to the Accept message. [TEST.PD.PS.EPR.SRC3.1#5]

        2. The Tester checks that the VBUS transition meets vSrcSlewPos and vSrcSlewNeg. [TEST.PD.PS.EPR.SRC3.1#6]

        3. During the voltage transition, the Tester checks that the VBUS voltage remains within vSrcValid limits from the time of crossing into the vSrcValid limits until tSrcSettle max. [TEST.PD.PS.EPR.SRC3.1#7]

        4. The Tester checks that the VBUS voltage remains within vSrcNew or vAvsNew limits between tSrcSettle max and 100ms after tSrcSettle max. [TEST.PD.PS.EPR.SRC3.1#8]

        5. The Tester checks that the UUT does not send PS_RDY before VBUS is within vSrcNew or vAvsNew. [TEST.PD.PS.EPR.SRC3.1#9]

        6. After having sent GoodCRC in response to PS_RDY, the Tester increases its current draw to the current requested and The Tester checks that the VBUS voltage remains within vSrcNew or vAvsNew limits for 100ms after receiving PS_RDY [TEST.PD.PS.EPR.SRC3.1#10]

e. The Tester repeats Step-4a to Step-4d, replacing the appropriate fields with the next value from the following list. The Tester sends 9 separate EPR_Request messages for each EPR_PDO.

    i. For Fixed PDOs, replace B19…10 (Operating Current) and For EPR AVS APDO, replace B6…0 (Operating Current):

        1. 0mA [performed in Step 4.b; listed here for reference only]

        2. 25% of Maximum Current

3. 50% of Maximum Current
4. 75% of Maximum Current
5. 100% of Maximum Current
6. 75% of Maximum Current
7. 50% of Maximum Current
8. 25% of Maximum Current
9. 0mA

TEST.PD.PS.EPR.SRC3.2 PDO Transitions in EPR Mode

Description: As a Sink only, the Tester enumerates all possible transitions among the PDOs of the UUT and verifies the UUT performs PDO transitions correctly in EPR Mode.
Test Specific Tester Behavior: N/A
Test Conditions:

This test is not applicable if the VIF parameter EPR_Supported_*As_Src* is set to No

	Consumer Only	Provider Only, P/C, C/P, DRP
Rev3ChkdSrc		✓

Test Procedures:

1. There are 2 possible bring-up procedures:
    a. The UUT has VIF field PD_Port_Type set to Consumer/Provider, the Tester runs bring-up procedure with the UUT as a Source COMMON.PROC.BU.7.
    b. The UUT has VIF field PD_Port_Type set to anything else, the Tester runs bring-up procedure with the UUT as a Source COMMON.PROC.BU.1.
2. The check fails if the "EPR mode capable" field is set to 0 in the Source Capabilities message sent by UUT during the bring up procedure and the test stops here. [TEST.PD.PS.EPR.SRC3.2#1]
3. The Tester sends an EPR_Mode (Enter) message with the Action field set to 0x01(Enter) and Data field set to 140 (140W) and enters EPR mode using common procedure COMMON.PROC.PD3.5[TEST.PD.PS.EPR.SRC3.2#2]
4. The Tester repeats the following steps using the PDO as provided in the **EPR_PDO Sequence Table**: Note, PDO Transitions only applicable for valid PDOs in the EPR_Source_Capabilities. Ignore the unused PDOs. For AVS APDO, request the max, min, and mid voltages in sequence.
    a. The Tester sends an EPR_Request message:
        i. B27 (GiveBack Flag) = 0b
        ii. B26 (Capability Mismatch) = 0b
        iii. B25 (USB Communication Capable) = 0b
        iv. B24 (No USB Suspend) = 1b
        v. B22 (EPR Mode Capable) = 1b
        vi. For Fixed PDO:

B19…10 (Operating Current) = 100mA
B9…0 (Maximum Operating Current) = 100mA
For EPR AVS PDO:
B20…9 (Output Voltage) = Maximum Voltage offered in Source APDO
B7…0 (Operating Current) = 100mA

b. The check fails if an Accept message is not received. [TEST.PD.PS.EPR.SRC3.2#3]
c. The check fails if PS_RDY message is not received within tPSTransition min ~~max~~ from the last bit of the EOP of Accept message. [TEST.PD.PS.EPR.SRC3.2#4]
d. The Tester performs the following checks:

Decrease the power drawn by the Tester to less than pSnkStdby within tSnkStdby min of the last bit of the GoodCRC sent in response to the Accept message. The Tester performs the following checks:

1. The Tester checks the VBUS is within vSrcNew or vAvsNew of the starting voltage within tSrcTransition min after the end of the GoodCRC sent in response to the Accept message. [TEST.PD.PS.EPR.SRC3.2#5]

2. The Tester checks that the VBUS transition meets vSrcSlewPos and vSrcSlewNeg. [TEST.PD.PS.EPR.SRC3.2#6]

3. During the voltage transition, the Tester checks that the VBUS voltage remains within vSrcValid limits from the time of crossing into the vSrcValid limits until tSrcSettle max. [TEST.PD.PS.EPR.SRC3.2#7]

4. The Tester checks that the VBUS voltage is within vSrcNew or vAvsNew limits between tSrcSettle max and 100ms after tSrcSettle max. [TEST.PD.PS.EPR.SRC3.2#8]

5. The Tester checks that the UUT does not send PS_RDY before the VBUS is within vSrcNew or vAvsNew. [TEST.PD.PS.EPR.SRC3.2#9]