USB Implementers Forum Technical White Paper Propagation Delay between Host Transceivers and Downstream Ports

May 11th, 2015

The USB 2.0 Specification limits the amount of time for a packet to travel from the host transceiver to the peripheral transceiver. The signal must travel across traces between the transceivers and USB connectors, across cable(s) and through any intervening hub(s). The specification also limits the amount of time for the host/peripheral to respond with a handshake which must, then, make the return trip. If it takes too long for all this to happen, the USB host and peripheral are allowed to error out the transaction.

Time measurements for this are performed in the interpacket gap tests. Interpacket gap is measured directly in high-speed, but is not measured in full-speed or low-speed. (Full-speed and low-speed signal quality is tested behind 5 tiers of hubs to empirically validate interpacket gap and bus turn-around time.)

Section 7.1.19 of the USB 2.0 Specification discusses delays. There you will find that signals in a cable must travel from connector to connector within 26ns (5.2ns/m max). This is why standard detachable cables are limited to 5 meters. The specification also limits the signal travel time to 3ns between the host transceiver and the downstream port. Travel time inside peripherals is limited to 1ns. High-speed hubs are required to repeat a signal within 36 bit-times + 4ns.

7.1.19.1 Low-/full-speed End-to-end Signal Delay

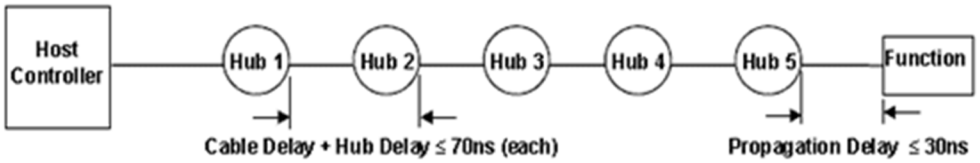

Figure 7-41. Worst-case End-to-end Signal Delay Model for Low-/full-speed

7.1.19.2 High-Speed End-to-end Delay

A high-speed host or device expecting a response to a transmission must not timeout the transaction if the inter-packet delay is less than 736 bit times, and it must timeout the transaction if no signaling is seen within 816 bit times.

These timeout limits allow a response to be seen even for the worst-case round trip signal delay. In high-speed mode, the worst-case round trip signal delay model is the sum of the following components:

12 max length cable delays (6 cables)	= 312 ns
10 max delay hubs (5 hubs)	= 40 ns + 360 bit times
1 max device response time	= 192 bit times
Worst-case round trip delay	= 352 ns + 552 bit times = 721 bit times

Full function personal computers are required to support high-speed, full-speed and low-speed. High-speed is achieved by implementing an EHCI. Full-speed and low-speed may be

achieved by implementing a companion UHCI or OHCI controller, which has no impact on the interpacket gap. Alternately, full-speed and low-speed may be achieved by embedding a high-speed hub downstream of the EHCI, which does directly impact interpacket gap.

If a high-speed hub is embedded in a PC, then interpacket gap measurements from the host's downstream port must account for the embedded hub's repeater delays. Adding 1 intervening hub adds 158ns (76 bit times) to the round trip timeout budget for high-speed signaling. This is added to the maximum 192 bit times allowed for the host itself or a total of 268 bit times.

Should an embedded high-speed hub be implemented, then the maximum number of nested hubs that can be supported downstream of the PC is reduced by one. When testing a product with an embedded high-speed hub, the tester should select 1 hub in the downstream section of USB Electrical Test tool. More information on how to test high-speed signal quality of a product with an embedded hub can be found in the readme file included with the download of USBET.