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Revision History:

<table>
<thead>
<tr>
<th>Revision</th>
<th>Issue Date</th>
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</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>July 2021</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
| 1.01     | August 2021| Editorial changes.  
|          |            | Updated list of provided files to include `tmu_fpga.exe`.  
|          |            | Made troubleshooting section for USB ethernet gadget into its own step. |
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Introduction

Time Measurement Equipment is an essential part of Time Synchronization Compliance testing. It is based on the Serial Time Link Protocol (STLP) that transmits current Grand Master time every 16 μsec. STLP is parsed and analyzed by a Time Measurement Equipment, which is FPGA based hardware.

There are two usages for such equipment:

Standalone Measurement

![Figure 1: Standalone setup](image1)

Comparative Time Measurement

![Figure 2: Pair Setup](image2)
# Required Hardware and Software

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Vendor</th>
<th>Link</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quad Motherboard</td>
<td>proFPGA</td>
<td><a href="https://www.profpga.com/products/motherboards-overview/profpga-quad">https://www.profpga.com/products/motherboards-overview/profpga-quad</a></td>
</tr>
<tr>
<td>Case (optional)</td>
<td>proFPGA</td>
<td><a href="https://www.profpga.com/products/miscellaneous-overview/duo">https://www.profpga.com/products/miscellaneous-overview/duo</a></td>
</tr>
<tr>
<td>Intel USB4 Evaluation Board</td>
<td>USB-IF</td>
<td><a href="https://www.usb.org/estore">https://www.usb.org/estore</a></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Software</th>
<th>Vendor</th>
<th>Link</th>
</tr>
</thead>
<tbody>
<tr>
<td>proFPGA-2020C-install.exe</td>
<td>proFPGA</td>
<td>*Contact proFPGA for this software</td>
</tr>
<tr>
<td>Files to use with USB4CV</td>
<td>USB-IF</td>
<td><a href="https://usb.org/compliancetools#anchor_usb4tools">https://usb.org/compliancetools#anchor_usb4tools</a></td>
</tr>
</tbody>
</table>

Please contact proFPGA about getting necessary items listed above.

https://www.profpga.com/
email: profpga@prodesign-europe.com
Quad Motherboard

Figure 3: Quad Motherboard

Duo & Quad Casing (optional)

Figure 4: Optional case for FPGA
Virtex® 7 module XC7V2000T

Figure 5: Virtex® 7 module

Intel USB4 Evaluation Dock as USB4 KG Device:

Figure 6: Intel USB4 Evaluation Dock
STLP Cable

STLP cable connects Intel USB4 Evaluation Dock TMU_CLK_OUT output and carries STLP protocol to FPGA.

The cable has 3 ends as shown on the following figure.

![Figure 7: STLP cable](image)

One end of the cable connects to Intel USB4 Evaluation Dock with SMP connector:

![Figure 8: Connecting SMP to Intel USB4 Evaluation Dock](image)

The other end of the cable has female header (size 0.1”):
Figure 9: STLP cable showing both ends. 0.1" 6pin housing and push-on SMP connectors
STLP Cable construction procedure for the Intel USB4 Evaluation Dock

These instructions can also be used to make custom cables for testing products that do not use SMP connectors for TMU_CLK_OUT.

The following materials will be necessary:

- 2x RF cable at least 48” with push-on SMP connectors.
  *Note:* Do not use semi-rigid type. Choose Braided Shielding (eg: PE3C3584/PH180-48)
- 3x 0.1” (2.54mm) Female crimp pins
- 1x 0.1” (2.54mm) Crimp connector housing 1x6-pin
- Wire stripper
- Crimping tool
- Soldering iron
- Heat shrink tubes
- Solder
- Solder flux (optional)

1. Strip the cable outer insulation/plastic jacket.

2. Carefully undo the braided shielding.
3. Strip about 0.5-1.0” of the dielectric insulation to expose the center conductor.
4. Use crimping tool to attach female crimp pins to the center conductors.
5. Add small amount of solder to center of female crimp pin to make ensure center conductor retains contact.
6. Repeat steps 1-5 for the 2nd cable.
7. Take one cable’s braid and twist to neatly compress the wires.
8. Repeat steps 4 and 5 for this twisted wire. Make sure to apply solder to the entire twisted wire.
9. Wrap the other cable’s braiding around the base of the crimped and soldered braid.
10. Put on heat shrinking tubes as desired for each of the three cable ends. Make sure to leave plenty of space past the crimp pins to allow the cables to slide into housings and be locked in.

11. Insert pins into the housing and give it a light tug test to ensure that the pin is secured in place.
   - GND braids to pin 1 (GND)
   - Choice of cable to pin 4 (PB)
   - Remaining cable to pin 6 (PA)
Connecting the system

Installing the module

Virtex® 7 module shall be installed on connector TA1 of Quad Motherboard

![Image of Virtex® 7 Module position on Quad Motherboard]

**Figure 10: Virtex® 7 Module position on Quad Motherboard**

Connecting STLP cable

STLP cable will need to be connected to the following pins located on the Virtex module:

![Diagram of Virtex® 7 Module Pins]

**Figure 11: Virtex® 7 Module Pins**
Figure 12: Pin 1 on ProFPGA
Figure 13: Connecting proFPGA and Intel USB4 Evaluation Dock using STLP cable. (Left) Both PA and PB connected. (Right) Only PA connected.
proFPGA Initial Setup on USB4CV System

This setup procedure only needs to be done once on a system and tester will only need to rely on the provided batch files for startup and shut down of the FPGA.

You will need to contact proFPGA for software install executable. Their contact can be found in the Required Hardware and Software section of this document.

The following files are provided by the USB-IF at https://usb.org/compliancetools#anchor_usb4tools to use proFPGA with USB4CV:

- TMU_FPGA.bat
- tmu_fpga.exe
- proj.cfg
- fmxc7v2000tr2.bit
- fpga_startup.bat
- fpga_shutdown.bat

All files should be placed into the following path to use with USB4CV:

```
C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance
```

Install proFPGA software

Run proFPGA software installation executable and set install path to `C:\ProDesign\proFPGA-2020C`

```
INSTALLED.txt
md5sum.txt
proFPGA-2020C-install.exe
proFPGA-2020C-install.sh
```
Connect proFPGA to USB4CV System

1. Turn on power supply.
2. Change the switch on mother board from OFF to ON
3. Connect proFPGA to USB4CV System
   i. If you purchased the optional case for the FPGA, use a USB2.0 STD B to A cable to connect STD B port on front of proFPGA to USB-A port on USB4CV System. (Do not use the ethernet port on the FPGA)

   ii. If you did not get the optional case for the FPGA, use a USB2.0 microB to A cable to connect from microB port on proFPGA to Type A port on USB4CV System.
Install Driver for USB Ethernet/RNDIS Gadget

This driver is needed to interface with the FPGA through the USB-A port.

1. Look for device in Device Manager. **The device probably is listed as serial device COM:**
   
   Open Windows Device Manager, in section ‘Ports (COM & LPT)’ select entry ‘Serial USB device’, right click and select ‘Update Driver Software’. You can verify this is the connection to the FPGA by unplugging FPGA from USB4CV System and seeing if that device goes away.

Figure 14: Update driver in Device Manager
i. Select **“Browse my computer for driver software”**

![Figure 15: Select “Browse my computer for driver software”](image)

ii. Specify path to the proFPGA Windows drivers which come with the proFPGA software release and press ‘Next’:

![Figure 16: Specify path to the proFPGA](image)
iii. Allow installation of the driver. Press ‘Install’ to continue.

Figure 17: Allow installation

Set Static IP Address on USB4CV System

To use a Static IP address, first set up your USB4CV System’s IP address to Static IP Address.

1. Open Control Panel and select Network and Sharing Center.

Figure 18: Network and Sharing Center
2. Click on **Change Adapter Settings**

![Change adapter setting](image1)

**Figure 19: Change adapter setting**

3. Click on “USB Ethernet/RNDIS Gadget”

![USB Ethernet/RNDIS Gadget](image2)

**Figure 20: USB Ethernet/RNDIS Gadget**
4. Click on “Properties”.

![Image of Ethernet Status with Properties highlighted]

**Figure 21: Choose “Properties”**


![Image of Ethernet Properties with Internet Protocol Version 4 highlighted]

Click on “Internet Protocol Version 4 (TCP/IPv4)” and open Properties.
Figure 22: Internet Protocol Version 4 (TCP/IPv4)

6. Click on “Use the following IP address”

In the IP address section type **169.254.0.1** (this is USB4CV System IP address)

In the subnet mask type **255.255.255.0**

Figure 23: IP address and the subnet mask

7. Click “OK”

Figure 24: Click OK
Verify that FPGA connection to USB4CV System works

1. Open Command Prompt and enter `ping 169.254.0.2`

![Figure 25: Ping proFPGA IP address](image1)

2. Make sure you received all packets

![Figure 26: All packets received](image2)
Using proFPGA

With all files in the correct locations, all you need to do now is use the provided Windows Batch files to start up and shut down the FPGA. Every time the FPGA is powered on, you need to burn the bit file again using the provided startup batch file. Once you start up the FPGA, follow USB4 TMU CTS for connections to test setups.

A good indication for when the FPGA is ready to use is by looking for a line of LEDs next to the power switch on the Quad motherboard. When initially powering on the FPGA, only a few LEDs will be lit:

![Figure 27: Top half of Quad motherboard](image)

![Figure 28: LEDs indicating bit file not burned](image)
Once you’ve burned the bit file, you can see that many more LEDs are lit:

![Figure 29: LEDs indicating bit file burned](image)

Start up proFPGA (burning the bit file)

Every time the FPGA is powered up, it is necessary to burn the FPGA with the bit file. `fpga_start-up.bat` will do this by running the following commands:

a. `cd C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance`

```
C:\Users\SWZ-14\cd C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance
C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance>
```

b. `profpga_run.exe proj.cfg -u`

```
C:\Users\SWZ-14\cd C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance
C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance>profpga_run.exe proj.cfg -u
```
c. Wait until loading .bit file is done

**Shut Down proFPGA**

Please run the shutdown script and wait for proFPGA to fully shutdown before powering off the FPGA.

*fpga_shutdown.bat* will shut down the FPGA by running the following command:

```
profpga_selftest C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance\proj.cfg -d
```

Wait until proFPGA finishes shutdown.

**Troubleshooting:**

If you are not able to turn on the FPGA with the batch files, please make sure that you followed the initial setup procedure correctly. Files need to be in a specific folder path and uses the specific IP address indicated in this procedure.
LEDs for PA and PB

When connecting to test setups defined in TMU CTS, FPGA module has dedicated LEDs that will light up when it is getting TMU_CLK_OUT from a device that is connected to a host and has established a stable link.

Figure 30: Blue LED lit for PA connection

Figure 31: Orange LED lit for PB connection