USB4TM

Time Measurement Equipment – Setup Procedure

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1.00	July 2021	Initial release.
1.01	August 2021	Editorial changes. Updated list of provided files to include tmu_fpga.exe . Made troubleshooting section for USB ethernet gadget into its own step.
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1.03	September 2023	Updated the KG USB4 Device board

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Introduction

Time Measurement Equipment is an essential part of Time Synchronization Compliance testing. It is based on the Serial Time Link Protocol (STLP) that transmits current Grand Master time every 16 □sec. STLP is parsed and analyzed by a *Time Measurement Equipment*, which is FPGA based hardware.

There are two usages for such equipment:

Standalone Measurement





Comparative Time Measurement



Figure 2: Pair Setup

A. Required Hardware and Software

Hardware Vendor	Link
-----------------	------

Quad Motherboard	proFPGA	https://www.profpga.com/products/motherboardsoverview/profpga- quad
Virtex 7 Module XC7V2000T	proFPGA	https://www.profpga.com/products/fpga-modulesoverview/virtex- 7-based/profpga-xc7v2000t
Case (optional)	proFPGA	https://www.profpga.com/products/miscellaneousoverview/duo-
Goodway Gatkex Board with TMU CLK Out Board (DBD1210L1)	Good Way Technology Co., Ltd.	https://www.goodway.com.tw/

Software	Vendor	Link
proFPGA-2020C-install.exe	proFPGA	*Contact proFPGA for this software
Files to use with USB4CV	USB-IF	https://usb.org/compliancetools#anchor_usb4tools

Please contact proFPGA about getting the necessary items listed above.



https://www.profpga.com/ email: profpga@prodesign-europe.com

A1. Quad Motherboard



Figure 3: Quad Motherboard

A2. Duo & Quad Casing (optional)



Figure 4: Optional case for FPGA

A3. Virtex[®] 7 module XC7V2000T



Figure 5: Virtex® 7 module

A4. Goodway Gatkex Board with TMU CLK Out as USB4 KG Device:

Contact Info: raymond_chan@goodway.com.tw & vivian_liao@goodway.com.tw



Figure 6: Goodway Gatkex Board with TMU CLK Out

A5. STLP Cable

STLP cable connects Goodway Gatkex Board TMU_CLK_OUT output and carries STLP protocol to FPGA.

The cable has 3 ends as shown on the following figure.



Figure 7: Example

One end of the cable connects to Goodway Gatkex Board with TMU CLK Out with SMP connector:



Figure 8: Connecting SMP to Goodway Gatkex Board with TMU CLK Out

The other end of the cable has female header (size 0.1"):



Figure 9: STLP cable showing both ends. 0.1" 6pin housing and push-on SMP connectors

A5.1. STLP Cable construction procedure for the Goodway Gatkex Board with TMU CLK Out

These instructions can be used to make custom cables for testing products that do not use SMP connectors for TMU CLK OUT.

The following materials will be necessary:

- 2x RF cables each at least 48inches long with push-on SMP connectors.
 Note: Do not use semi-rigid type. Choose braided shielding (eg: PE3C3584/PH180-48)
- 1x 0.1inch (2.54mm) Crimp connector housing 1x6-pin
- Wire stripper
- Heat shrink tubes
- 3x Heat shrink tubes with solder ring
- Heat gun
- 3x 2inch pre-crimped wires
- Hot glue gun

1. Strip at least 1" of the outer insulation.



2. Carefully undo the braided shielding. It is recommended to use a small and fine tool to poke into the braids and pull towards the open end of the cable. Start from the end of the cable and slowly work down to slowly undo the braiding.



3. Strip about 1/4 inch of the dielectric insulation to expose the center conductor.



4. Take a pre-crimped wire and feed into a heat shrink tube with solder ring. Take the exposed center conductor and insert into one of the crimps. Then pull the heat shrink tube over this connection and line the solder ring up with the metal-to-metal contact portion.



- 5. Use heat gun to shrink the tube and pay extra attention to melt the solder ring. Solder ring should visibly deform or fill in gaps of the crimp contact.
- 6. Repeat steps 1-5 for the second cable.
- 7. Combine both Ground braids by twisting them together. Repeat steps 4 and 5 on this combined braid.



8. Use heat shrink (no solder ring) to cover excess exposed braiding.



- 9. Insert pins into the housing and give it a light tug test to ensure that the pin is secured in place:
 - GND braids to pin 1 (GND)
 - Choice of cable to pin 4 (PB)
 - Remaining cable to pin 6 (PA)



10. Apply hot glue to bottom of housing. Make sure to fill in spaces between the three cables and also overlap onto the plastic housing to prevent the cables from bending when attaching this cable to FPGA.



B. Connecting the system

B1. Installing the module

Virtex® 7 module shall be installed on connector TA1 of Quad Motherboard



Figure 10: Virtex ® 7 Module position on Quad Motherboard

B2. Connecting STLP cable

STLP cable will need to be connected to the following pins located on the Virtex module:



Figure 11: Virtex ® 7 Module Pins



Figure 12: Pin 1 on ProFPGA



Figure 13: Connecting proFPGA and Goodway Gatkex Board using STLP cable. (Left) Both PA and PB connected. (Right) Only PA connected.

C. proFPGA Initial Setup on USB4CV System

This setup procedure only needs to be done once on a system and tester will only need to rely on the provided batch files for startup and shut down of the FPGA.

You will need to contact proFPGA for software install executable. Their contact can be found in the Required Hardware and Software section of this document.

The following files are provided by the USB-IF at <u>https://usb.org/compliancetools#anchor_usb4tools</u> to use proFPGA with USB4CV:

- TMU_FPGA.bat
- tmu_fpga.exe
- proj.cfg
- fmxc7v2000tr2.bit
- fpga_startup.bat
- fpga_shutdown.bat

All files should be placed into the following path to use with USB4CV:

C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance

C1. Install proFPGA software

Run proFPGA software installation executable and set install path to C:\ProDesign\proFPGA-2020C\



C2. Connect proFPGA to USB4CV System

- 1. Turn on the power supply.
- 2. Change the switch on mother board from OFF to ON
- 3. Connect proFPGA to USB4CV System:
 - If you purchased the optional case for the FPGA, use a USB2.0 STD
 B to A cable to <u>connect STD B port on front of proFPGA to USB-</u>
 <u>A port on USB4CV System</u>. (Do not use the ethernet port on the FPGA)



 ii. If you did not get the optional case for the FPGA, use a USB2.0 microB to A cable to <u>connect from</u> microB port on proFPGA to Type A port on USB4CV System.



C3. Install Driver for USB Ethernet/RNDIS Gadget

This driver is needed to interface with the FPGA through the USB-A port.

C3.1. Identify Device Driver for FPGA

Open Device Manager. The device is most likely listed as a Serial Device COM under 'Ports (COM & LPT)'.

Verify this device is the FPGA by unplugging FPGA from the USB4CV System and seeing if the device goes away.



Figure 14: Update driver in Device Manager

C3.2 Update Driver Software

Right-click the Serial USB Device and select "Update Driver Software". Select "Browse my computer for software".



Figure 15: Select "Browse my computer for driver software"

Specify path to the proFPGA Windows drivers which came with the proFPGA software release and press 'Next':

÷	Update Drivers - Linux USB Ethernet/RNDIS Gadget	×
	Browse for drivers on your computer	
	Search for drivers in this location:	
	C\ProDesign\proFPGA-2020C\driver	
	→ Let me pick from a list of available drivers on my computer This list will show available drivers compatible with the device, and all drivers in the same category as the device.	

Figure 16: Specify path to the proFPGA

Allow installation of the driver. Press 'Install' to continue.



Figure 17: Allow installation

C4. Set Static IP Address for FPGA

To use a Static IP address, first set up your USB4CV System's IP address to Static IP Address.

1. Open Control Panel and select Network and Sharing Center.



Figure 18: Network and Sharing Center

2. Click on Change Adapter Settings

Control Panel Home	Control Panel Home View your basic network information and set up connections		
Change adapter settings	View your active networks		
Change advanced sharing	Specwerkz-net-2.4G	Access type: Internet	
ettings	Public network	Connections: Mi-Fi (Specwerkz-net-2.4G)	
Media streaming options			
	Unidentified network	Access type: No network access	
	Public network	Connections: 📱 Ethernet 3	
	Change your networking settings		
	Set up a new connection or netv	vork	
	Set up a broadband, dial-up, or	/PN connection; or set up a router or access point.	
	Troubleshoot problems		
	Diagnose and repair network pro	blems, or get troubleshooting information.	

Figure 19: Change adapter setting



Figure 20: USB Ethernet/RNDIS Gadget

4. Click on "Properties".

neral		
Connection		
IPv4 Connectiv	vity:	No network access
IPv6 Connectiv	vity:	No network access
Media State:		Enabled
Duration:		00:08:41
Speed:		425.9 Mbps
Details	1	
Details	Sent —	Received
Details	Sent —	Received
Details ctivity Bytes:	Sent — 58,360,758	Received

Figure 21: Choose "Properties"

5. Click on "Internet Protocol Version 4 (TCP/IPv4)" and open Properties.

tothonding	Sharing			
Connect us	sing:			
🖵 Linu	ıx USB Ether	net/RNDIS Gadget #	3	
			Configur	e
This conne	ection uses th	ne following items:		
	lient for Micro ile and Printe	osoft Networks r Sharing for Microsoft	Networke	^
	oS Packet S	cheduler	INCINOIRS	
		GIGGUIGI		
	nternet Protoc	col Version 4 (TCP/IP	v4)	
	nternet Protoc Nicrosoft Netv	col Version 4 (TCP/IP work Adapter Multiplex	v4) tor Protocol	
	nternet Protoc Nicrosoft Netv Nicrosoft LLD	col Version 4 (TCP/IP work Adapter Multiplex P Protocol Driver	v4) or Protocol	
	nternet Protoc Nicrosoft Netv Nicrosoft LLD Internet Protoc	col Version 4 (TCP/IP) work Adapter Multiplex P Protocol Driver col Version 6 (TCP/IP)	v4) tor Protocol v6)	~
	nternet Protoc Nicrosoft Netv Nicrosoft LLD Internet Protoc	col Version 4 (TCP/IP work Adapter Multiplex P Protocol Driver col Version 6 (TCP/IP	v4) xor Protocol v6)	× >
	nternet Protoco Nicrosoft Netw Nicrosoft LLD Internet Protoco all	col Version 4 (TCP/IP) work Adapter Multiplex P Protocol Driver col Version 6 (TCP/IP)	v4) kor Protocol v6) P <u>r</u> opertie	> ~
✓ ✓ ✓	nternet Protoco Nicrosoft Netw Nicrosoft LLD nternet Protoco all	col Version 4 (TCP/IP) work Adapter Multiplex P Protocol Driver col Version 6 (TCP/IP)	v4) kor Protocol v6) P <u>r</u> opertie	> >

Figure 22: Internet Protocol Version 4 (TCP/IPv4)

6. Click on "Use the following IP address"

In the IP address section type 169.254.0.1 (this is USB4CV System IP address)

In the subnet mask type 255.255.255.0

General	
You can get IP settings assigne this capability. Otherwise, you for the appropriate IP settings.	d automatically if your network supports need to ask your network administrator
Obtain an IP address auto	omatically
• Use the following IP addre	ss:
IP address:	169.254.0.1
Subnet mask:	255 . 255 . 255 . 0
Default gateway:	
Obtain DNS server addres	s automatically
• Use the following DNS serv	ver addresses:
Preferred DNS server:	· · · ·
Alternate DNS server:	
	it Advanced

Figure 23: IP address and the subnet mask

7. Click "OK"

General	
You can get IP settings assign this capability. Otherwise, you for the appropriate IP settings	ed automatically if your network supports need to ask your network administrator s.
Obtain an IP address aut	omatically
• Use the following IP addr	ess:
IP address:	169.254.0.1
Subnet mask:	255 . 255 . 255 . 0
Default gateway:	· · · · ·
Obtain DNS server addre	ss automatically
• Use the following DNS se	rver addresses:
Preferred DNS server:	· · · · · · · · ·
Alternate DNS server:	• 1.0 · · · ·
	20 US

Figure 24: Click OK

Verify that FPGA connection to USB4CV System works

1. Open Command Prompt and enter ping 169.254.0.2



Figure 25: Ping proFPGA IP address

2. Make sure you received all packets



Figure 26: All packets received

D. Using proFPGA with USB4CV

With all files in the correct locations, all you need to do now is use the provided Windows Batch files to start up and shut down the FPGA. Every time the FPGA is powered on, you need to burn the bit file again using the provided startup batch file. Once you start up the FPGA, follow USB4 TMU CTS for connections to test setups.

A good indication for when the FPGA is ready to use is by looking for a line of LEDs next to the power switch on the Quad motherboard. When initially powering on the FPGA, only a few LEDs will be lit:



Figure 27: Top half of Quad motherboard



Figure 28: LEDs indicating bit file not burned

Once you've burned the bit file, you can see that many more LEDs are lit:



Figure 29: LEDs indicating bit file burned

D1. Start up proFPGA (burning the bit file)

Every time the FPGA is powered up, it is necessary to burn the FPGA with the bit file. *fpga_start-up.bat* will do this by running the following commands:

a. cd C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance

Command Prompt		×
Microsoft Windows [Version 10.0.19041.572] (c) 2020 Microsoft Corporation. All rights reserved.		^
C:\Users\SWZ-14>cd C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance		
C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance>		

b. profpga_run.exe proj.cfg -u



c. Wait until loading .bit file is done

INFO	:	power up FPGA modules on motherboard 1			
INFO		power up FPGA module <mb1 0="" ta1=""></mb1>			
INFO		setting over-temperature shutdown to 84 deg. C			
INFO		enable PSUs (except IO voltage)			
INFO		enable VIO PSUs			
INFO		checking power-goods of FPGA modules on motherboard 1			
INFO		checking power-goods on FPGA module <mb1 0="" ta1=""></mb1>			
INFO		Release resets from FPGA modules on motherboard_1			
INFO		configure FPGAs on motherboard_1			
INFO		configure FPGAs 1			
INFO	: loading bitstream "C:/Users/Public/Documents/TMU_FPGA/USB4_Compliance/fmxc7v2000tr2.bit" into FPGA <mb1 0="" ta1=""> on MMI64 address 05 with id (</mb1>				
3000000	15 p	lease wait			
00.0 [>]			
INFO		: done			
INFO		: reset on sync_0 on motherboard_1 released			
INFO	: Rescanning for MMI64 modules inside User FPGAs. This operation may				
INFO	: deadlock if MMI64 inside the user design does not respond correctly.				
INFO	: Success.				
INFO	: MB 1.FPGA_TA1: Found profpga_ctrl module inside user design.				
INFO	Done				

D2. Shut Down proFPGA

Please run the shutdown script and wait for proFPGA to fully shutdown before powering off the FPGA.

fpga_shutdown.bat will shut down the FPGA by running the following command:

profpga_selftest C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance\proj.cfg -d

Wait until proFPGA finishes shutdown.

INFO	;	Power down motherboard 1
INFO		deactivating P12V A1
INFO		deactivating P12V C1
INFO		deactivating P12V A3
INFO		deactivating P12V C3
INFO		deactivating P3V3
INFO		deactivating P3V3_AUX

Troubleshooting:

If you are not able to turn on the FPGA with the batch files, please make sure that you followed the initial setup procedure correctly. Files need to be in a specific folder path and uses the specific IP address indicated in this procedure.

D3. LEDs for PA and PB

When connecting to test setups defined in TMU CTS, FPGA module has dedicated LEDs that will light up when it is getting TMU_CLK_OUT from a device that is connected to a host and has established a stable link.



Figure 30: Blue LED lit for PA connection



Figure 31: Orange LED lit for PB connection