USB Power Delivery ENGINEERING CHANGE NOTICE

Title: PPS Power Limit Bit update
Applied to: USB Power Delivery Specification Revision 3.1 Version 1.5

Brief description of the functional changes proposed:
Changing the rules for PPS sources to match what should be expected from these sources

Benefits as a result of the proposed changes:
Sinks will see a more consistent behavior form sources.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
Minor

An analysis of the hardware implications:
Minor, possibly a simplification.

An analysis of the software implications:
Probably none.

An analysis of the compliance testing implications:
Testing can be more consistent with better defined behavior of the UUT.

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Actual Change Requested

(a). Section 6.4.1.2.5.1.1

From Text:

When the PPS Power Limited bit is set, the SPR PPS Source ***Shall Not*** supply power that exceeds the Source's rated PDP; if the requested Output Voltage in the RDO exceeds the nominal Prog Voltage (e.g. 5V for the 5VProg), the SPR PPS ***Shall*** limit its output current such that for a PDP Rating of x Watts the output current limit is calculated as RoundDown(x/requested Output Voltage) to the nearest 50mA. . The SPR PPS Source ***Shall Not*** reject an RDO with an Output Current that is less than or equal to the Maximum Current in the APDO even if the requested Output Current is greater than the Source's current limit. An SPR PPS Source that sets the Power Output Limited bit ***Shall*** automatically limit its output current so as not to exceed its PDP Rating (See Figure 7-7).
When the PPS Power Limited bit is cleared, the SPR PPS Source ***Shall*** deliver the Maximum Current up to the Maximum Voltage as Advertised in its APDO.

To Text:

When the PPS Power Limited bit is set, the SPR PPS Source ***Shall*** operate in the same way as if the PPS Power Limited bit is clear (See Section 7.1.4.2) with the below exception:

- ***May*** supply power that exceeds the Source's rated PDP within the Optional operating area in Figure 7-9.

The SPR PPS Source ***Shall Not*** reject an RDO with an Output Current that is less than or equal to the Maximum Current in the APDO even if the requested Output Current is greater than the Source's PDP/requested Output Voltage.
When the PPS Power Limited bit is cleared, the SPR PPS Source ***Shall*** deliver the Maximum Current up to the Maximum Voltage as Advertised in its APDO.

(b). Section 7.1.4.2.3

From Text:

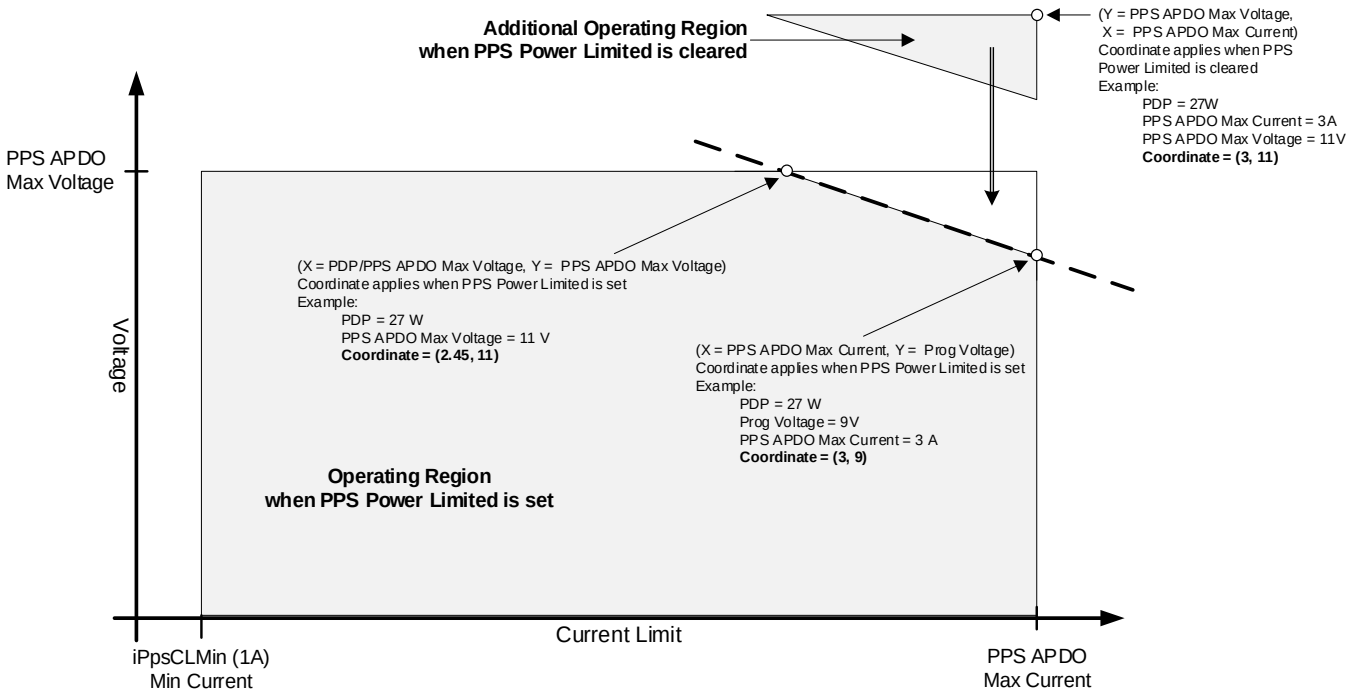
In Constant Power mode (when the PPS Power Limited bit is set) the Source ***Shall*** limit its output current so that the product of the output current times the output Voltage does not exceed the Source's PDP Rating. Sinks ***May Not*** limit their Operating Current request in the RDO but ***Shall*** meet the requirements of Section 7.2.9.
The relationship between SPR PPS programmable output Voltage and SPR PPS programmable Current Limit in the Constant Power mode Shall be as shown in Figure 7-9.

To Text:

In Constant Power mode (when the PPS Power Limited bit is set) the Source ***May*** supply power that exceeds the Source's rated PDP. Sinks ***May*** limit their Operating Current request in the RDO and ***Shall*** meet the requirements of Section 7.2.9.
The tolerances along the Constant Power Curve ***Shall Not*** extend into the Guaranteed Capability Area of Figure 7-9.

(c). Figure 7-1 SPR PPS Programmable Voltage and Current Limit

From:


Additional Operating Region
when PPS Power Limited is cleared
(Y = PPS APDO Max Voltage,
X = PPS APDO Max Current)
Coordinate applies when PPS
Power Limited is cleared
Example:
PDP = 27W
PPS APDO Max Current = 3A
PPS APDO Max Voltage = 11V
Coordinate = (3, 11)
PPS APDO
Max Voltage
Voltage
(X = PDP/PPS APDO Max Voltage, Y = PPS APDO Max Voltage)
Coordinate applies when PPS Power Limited is set
Example:
PDP = 27 W
PPS APDO Max Voltage = 11 V
Coordinate = (2.45, 11)
(X = PPS APDO Max Current, Y = Prog Voltage)
Coordinate applies when PPS Power Limited is set
Example:
PDP = 27 W
Prog Voltage = 9V
PPS APDO Max Current = 3 A
Coordinate = (3, 9)
Operating Region
when PPS Power Limited is set
Current Limit
iPpsCLMin (1A)
Min Current
PPS APDO
Max Current

To:

Capabilities when the Power Limited bit is set
The figure shows only the steady state after the transition