USB Power Delivery ENGINEERING CHANGE NOTICE

Title: Update to PPS Requirements
Applied to: USB Power Delivery Specification Revision 3.1 Version 1.7

Brief description of the functional changes proposed:
Raises the minimum voltage for PPS from 3.3 to 5V. Eliminates 5V Prog Improves the definition of the voltage and current steps Relaxes the Current Limit regulation

Benefits as a result of the proposed changes:
Simplifies design requirements and eliminates unnecessarily strict requirements for current limit regulation and voltage steps

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
Do not expect any.

An analysis of the hardware implications:
Should reduce hardware cost and simplify design and testing.

An analysis of the software implications:
None

An analysis of the compliance testing implications:
Relaxes parameter should make testing easier in the long run. Requires testers to comprehend the relaxed requirements..

USB Power Delivery ENGINEERING CHANGE NOTICE

Actual Change Requested

(a). Section 1.6, Table 1-1, P49

New Text:

Term	Description
Adjustable Voltage Supply (AVS)	A power supply whose output Voltage can be adjusted to an operating Voltage within its Advertised range. These capabilities are exposed by the Adjustable Voltage Supply (AVS) APDO (see Section 6.4.1.2.5). Note unlike the SPR PPS, the EPR AVS does not support current limit.
Augmented Power Data Object (APDO)	Data Object used to expose a Source Port's power capabilities or a Sink's power requirements as part of a ***Source_Capabilities*** or ***Sink_Capabilities*** Message respectively. Programmable Power Supply Data Object is defined.
Constant Voltage (CV)	A mode in which the Source output Voltage remains constant as the load changes.
Current Limit (CL)	A current limiting feature of an SPR PPS Source. When a Sink operating in SPR PPS mode attempts to draw more current from the Source than the requested Current Limit value, the Source reduces its output Voltage so the current it supplies remains at or below the requested value. Note current limit is not supported by EPR AVS Sources.
Differential Non-Linearity (DNL)	The difference between an ideal LSB step, and the real observable LSB step when the Power Source is operating in PPS mode. A DNL of 0 indicates that the step is ideal. If DNL is positive the step is larger than the ideal LSB, and if it is negative then the step is smaller than ideal.
EPR AVS	A power supply operating in EPR Mode whose output Voltage can be adjusted to an operating Voltage within its Advertised range. Unlike SPR PPS it does not support current limit. The AVS capabilities are exposed by the Adjustable Voltage Supply APDO (see Section 6.4.1.2.5).
Programmable Power Supply (PPS)	A power supply, operating in SPR Mode, whose output Voltage can be programmatically adjusted in small increments over its Advertised range. And also has a programmable output current fold back (note that the EPR AVS does not). The capabilities are exposed by the SPR Programmable Power Supply APDO (see Section 6.4.1.2.5).
Sink Directed Charge	A charging scheme whereby the Sink connects the Source to its battery through safety and other circuitry. When the SPR PPS Current Limit feature is activated, the Source automatically controls its output current by adjusting its output Voltage.
SPR PPS	A power supply operating in SPR PPS Mode whose output Voltage and output current can be programmatically adjusted in small increments over its Advertised range. It supports current limit unlike EPR AVS. The capabilities are exposed by the Programmable Power Supply APDOs (see Section 6.4.1.2.5).

(b). Section 2.9.2, Table 2-2, P77

From Text:

Available Current	Prog	Min Voltage	Max Voltage	PDP Range
3A	5V Prog	3.3V	5.9V	15 – 60W
	9V Prog	3.3V	11V	
	15V Prog	3.3V	16V	
	20V Prog	3.3V	21V	
5A[1]	20V Prog	3.3V	21V	60 – 100W

Available Current	Prog	Min Voltage	Max Voltage	PDP Range
[1] Requires 5A cable.				

To Text:

Table 2-1 PPS Voltage Power Ranges

Available Current	Prog	Min Voltage	Max Voltage	PDP Range
3A	~~5V Prog~~	~~3.3V~~	~~5.9V~~	~~15 – 60W~~ 16 – 60W
	9V Prog	~~3.3V~~ 5V	11V	
	15V Prog	~~3.3V~~ 5V	16V	
	20V Prog	~~3.3V~~ 5V	21V	
5A[1]	20V Prog	~~3.3V~~ 5V	21V	~~60~~ 61– 100W
[1] Requires 5A cable.				

(c). Section 6.4.1.2.5.1, P138

From Text:

Table 6 13 below describes the SPR Programmable Power Supply (1100b) APDO for a Source operating in SPR Mode and supplying 3.3V up to 21V.

To Text:

Table 6-13 below describes the SPR Programmable Power Supply (1100b) APDO for a Source operating in SPR Mode and supplying 5V up to 21V.

(d). Section 7.1.4.2.1, P278

From Text:

Section 7.1.14 lists transitions that are exempt from the ***vPpsSlewNeg*** and ***vPpsSlewPos*** limits.

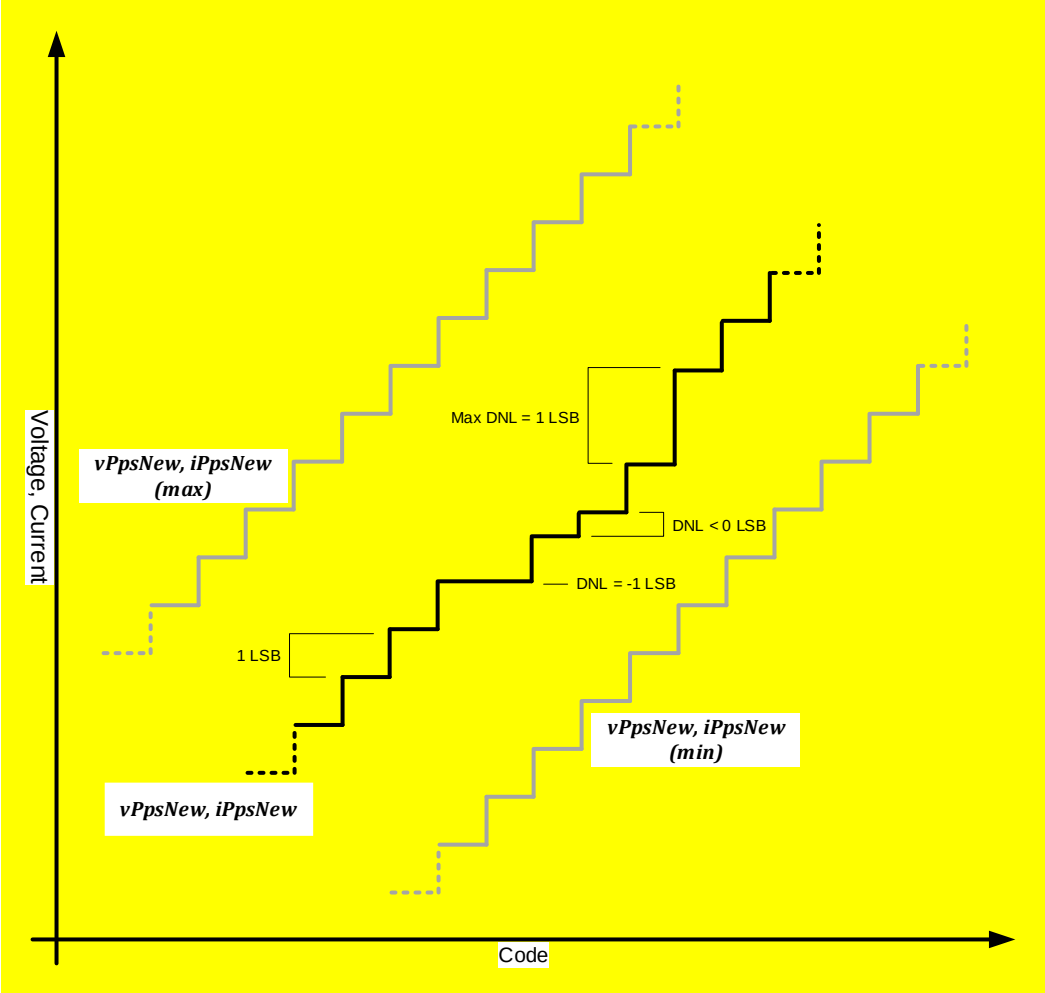
To Text:

Section 7.1.14 lists transitions that are exempt from the ***vPpsSlewNeg*** and ***vPpsSlewPos*** limits.
The PPS voltage and current discrete LSB steps have a DNL tolerance as shown in the figure below. In absolute terms the step size of the LSB for both voltage and current is defined by ***vPpsStep***, *and* ***iPpsCLStep*** for voltage and current, respectively. Several examples of valid LSB steps are shown on Figure 7-x below.

- The upper end of the DNL error (+1 LSB) shows the case where one step is effectively skipped.
- The lower end of the DNL error (-1 LSB) show the case where the voltage or current setpoint remained the same.

The ideal scenario for the DNL error (=0) matches the typical step size for the voltage or current.
The intent of DNL is to guarantee that the voltage/current have the correct directionality, and that the maximum step size is clearly defined. It should be noted that the Source should avoid scenarios where multiple consecutive steps have errors close to the Maximum and Minimum DNL.

Figure 7-x Allowed DNL errors and tolerance of Voltage and Current in PPS mode



(e) Section 7.1.4.2.2, P.281

From Text:

The Programmable Power Supply operating in SPR PPS Mode ***Shall*** limit its output current to the Operating Current value in the Programmable RDO when the Sink attempts to draw more current than the Output Current level. The programming step size for the Output Current is ***iPpsCLStep***. All programming changes of the Operating Current ***Shall*** settle to the new Operating Current value within ***tPpsCLProgramSettle***. The SPR PPS

Operating Current regulation accuracy during Current Limit is defined as ***iPpsCLNew***. The minimum programmable Current Limit level is ***iPpsCLMin***. A Source that supports SPR PPS ***Shall*** support Current Limit programmability between ***iPpsCLMin*** and the Maximum Current value in the SPR PPS APDO. A Source which receives a request for current below ***iPpsCLMin*** ***Shall*** reject the request.

To Text:

The Programmable Power Supply operating in SPR PPS Mode ***Shall*** limit its output current to the Operating Current value in the Programmable RDO when the Sink attempts to draw more current than the Output Current level. The programming step size for the Output Current is ***iPpsCLStep***. All programming changes of the Operating Current ***Shall*** settle to the new Operating Current value within ***tPpsCLProgramSettle***. The SPR PPS Operating Current regulation accuracy during Current Limit is defined as ***iPpsCLNew***. The minimum programmable Current Limit level is ***iPpsCLMin***. A Source that supports SPR PPS ***Shall*** support Current Limit programmability between ***iPpsCLMin*** and the Maximum Current value in the SPR PPS APDO. A Source which receives a request for current below ***iPpsCLMin*** ~~***Shall***~~ ***Should*** reject the request. A Source that accepts a request for current below ***iPpsCLMin Shall*** set its current limit at 1A.

(f) Section 7.1.4.2.2, P282

From Text:

The SPR PPS ***Shall*** maintain its output Voltage at the value requested in the PPS RDO for all static and dynamic load conditions except when in Current Limit operation. In response to any static or dynamic load condition during Current Limit operation that causes the SPR PPS output Voltage to drop below ***vPpsShutdown*** the Source ***May*** send ***Hard Reset*** Signaling and ***Shall*** discharge V_{BUS} to ***vSafe0V*** then resume default operation at ***vSafe5V***.
When the Sink attempts to draw more current than the Operating Current in the RDO, the Source ***Shall*** limit its output current. The current available from the Source during Current Limit mode shall meet ***iPpsCLNew*** plus ***iPpsCLOperating***. The Sink ***May Not*** reduce its Operating Current request in the RDO when the PPS Status OMF is set.
Current limiting ***Shall*** be performed by the SPR PPS Source. Sinks that rely on PPS Current Limiting ***Shall*** meet the requirements of Section 7.2.9. The Source ***Shall Not*** shutdown or otherwise disrupt the available output power while in Current Limit mode unless another protection mechanism as outlined in Section 7.1.7 is engaged to protect the Source from damage.
The relationship between SPR PPS programmable output Voltage and SPR PPS programmable Current Limit ***Shall*** be as shown in Figure 7-7. The transition between the Constant Voltage mode and the Current Limit mode occurs between points *a* and *b*. The PPS Status OMF shall be set or cleared within this region. In Current Limit mode when the load resistance changes the output current of the Source stay within ***iPpsCLOperating***, which is determined by point b (a measured value). As the load resistance decreases the output current should stay the same or increase slightly and as the load resistance increases the output current should stay the same or decrease slightly. The amount of allowable increase and decrease Shall Not exceed ***iPpsCLTolerance*** relative to a straight line drawn between points b and e as illustrated in Figure 7-8.
The proper behavior is represented by point *c*. Likewise, as the load resistance increases, the output current of the Source ***Shall Not*** increase. The proper behavior is represented by point *d*.

To Text:

The SPR PPS Source ***Shall*** maintain its output Voltage at the value requested in the PPS RDO for all static and dynamic load conditions except when in Current Limit operation. In response to any static or dynamic load condition during Current Limit operation that causes the SPR PPS output Voltage to drop below ***vPpsShutdown***

the Source ***May*** send ***Hard Reset*** Signaling and ***Shall*** discharge V_{BUS} to ***vSafe0V*** then resume default operation at ***vSafe5V***.

When the Sink attempts to draw more current than the Operating Current in the RDO, the Source ***Shall*** limit its output current. The current available from the Source during Current Limit mode shall meet ***iPpsCLNew*** ~~plus ***iPpsCLOperating***~~. The Sink ***May Not*** reduce its Operating Current request in the RDO when the PPS Status OMF is set.

Current limiting ***Shall*** be performed by the SPR PPS Source. Sinks that rely on PPS Current Limiting ***Shall*** meet the requirements of Section 7.2.9. The Source ***Shall Not*** shutdown or otherwise disrupt the available output power while in Current Limit mode unless another protection mechanism as outlined in Section 7.1.7 is engaged to protect the Source from damage.

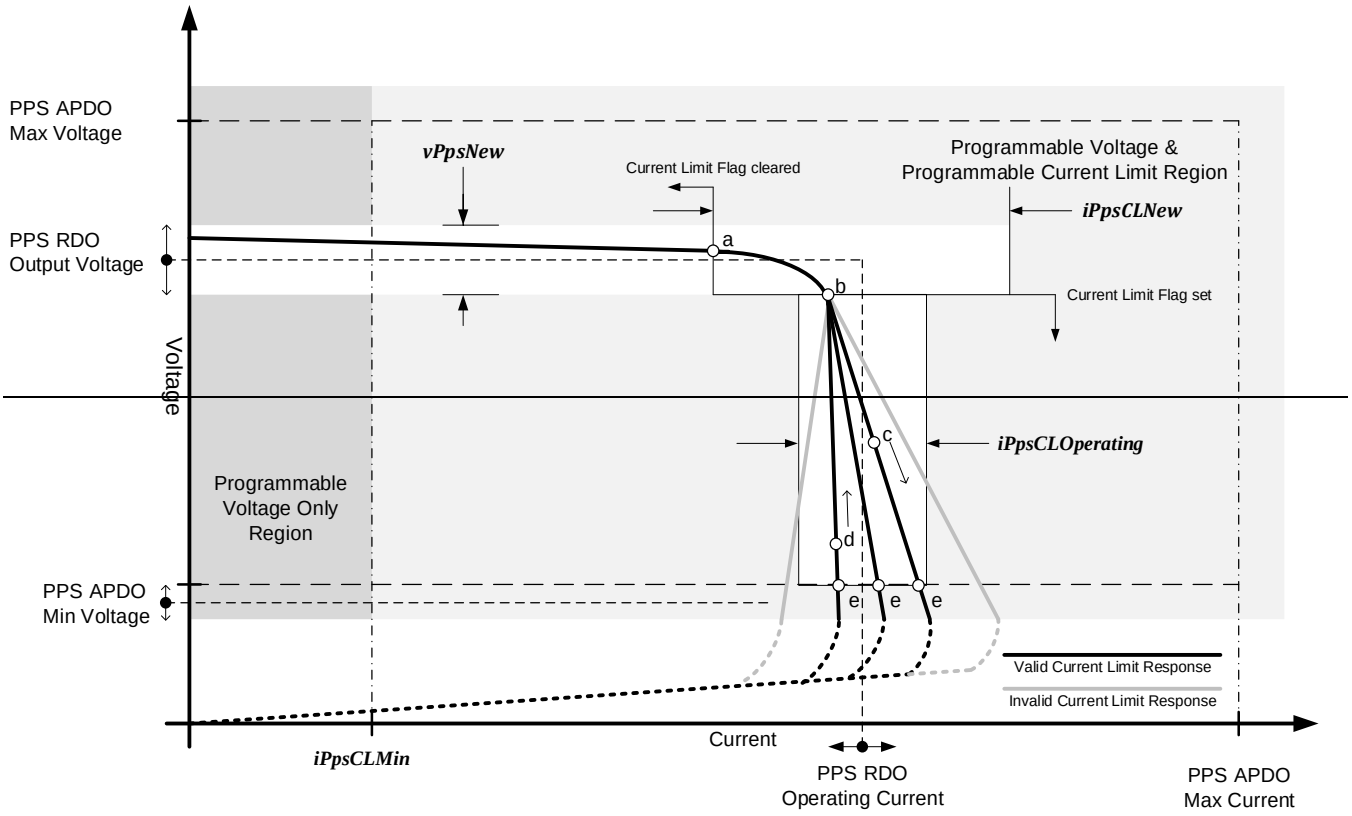
An SPR PPS Source that is operating in Current Limit ***Shall Not*** change its setpoint in a manner that exceeds ***iPpsCLLoadStepRate*** or ***iPpsCLLoadReleaseRate***.

The relationship between SPR PPS programmable output Voltage and SPR PPS programmable Current Limit ***Shall*** be as shown in Figure 7-7. The transition between the Constant Voltage mode and the Current Limit mode occurs between points *a* and *b*. The PPS Status OMF shall be set or cleared within this region. In Current Limit mode when the load resistance changes, the output current of the Source ~~stay within ***iPpsCLOperating***, which is determined by point b (a measured value). As the load resistance decreases the output current should stay the same or increase slightly and as the load resistance increases the output current should stay the same or decrease slightly. The amount of allowable increase and decrease Shall Not exceed ***iPpsCLTolerance*** relative to a straight line drawn between points b and c as illustrated in Figure 7-8~~***Shall*** stay within ***iPpsCLNew***. The proper behavior is represented by point *c*.

~~Likewise, as the load resistance increases, the output current of the Source ***Shall Not*** increase. **Error! Reference source not found.**Figure 7-8 illustrates examples of output current during Current Limit that both stay within or violate ***iPpsCLNew*** limits.~~
~~The proper behavior is represented by point *d*.~~

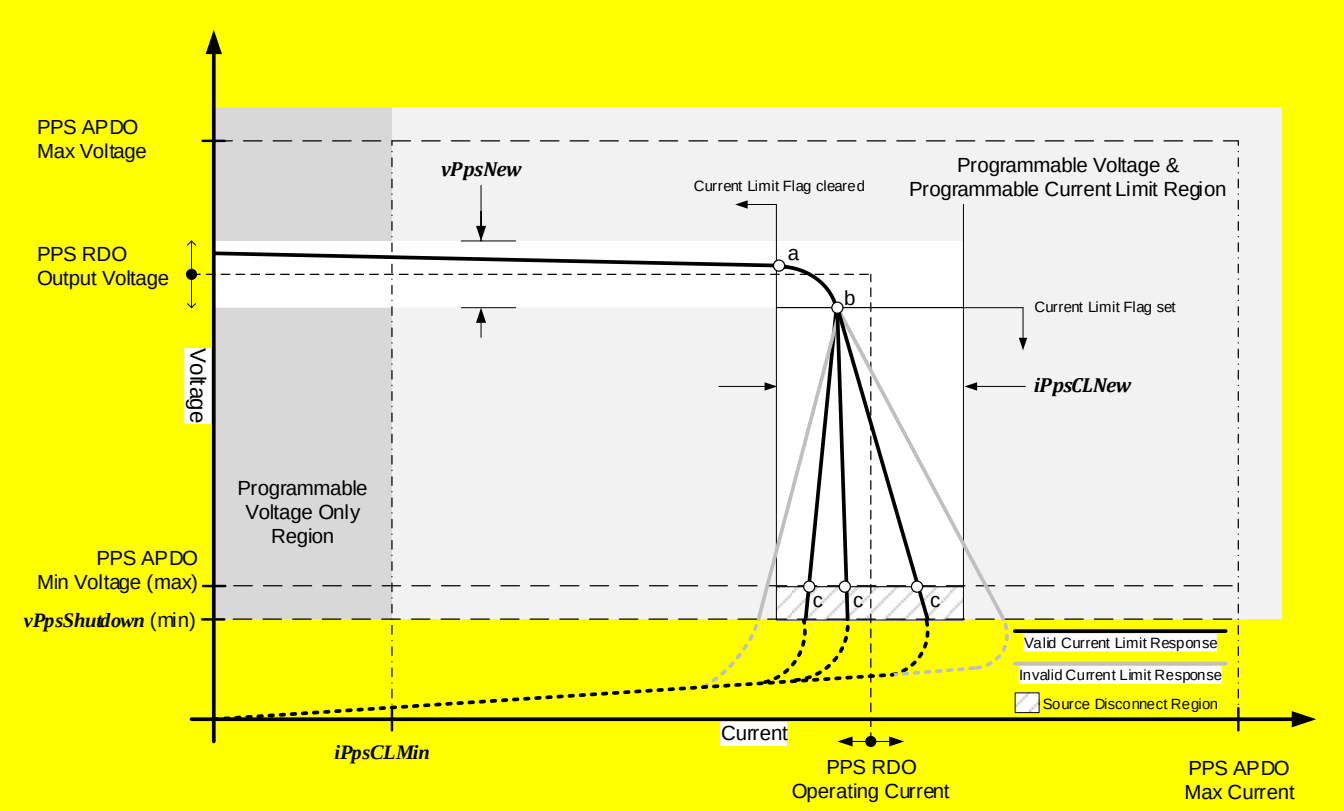
(g). Figure 7-7, P283

From Text:



- Point *a* represents entry into the transition region between Constant Voltage mode and Current Limit mode.
- Point *b* represents exit from the transition region between Constant Voltage mode and Current Limit mode.
- Point *b* is where the allowable increase in current up to ***iPpsCLOperating*** begins.
- Point *c* represents the behavior as the load resistance decreases during Current Limit mode. See Table 7-22 for the allowed change in Operating Current (***iPpsCLOperating***) during this behavior.
- Point *d* represents the behavior as the load resistance increases during Current Limit mode. See Table 7-22 for the allowed change in Operating Current (***iPpsCLOperating***) during this behavior.
- Point e represents the exit from the ***iPpsCLOperating*** region.

To Text:



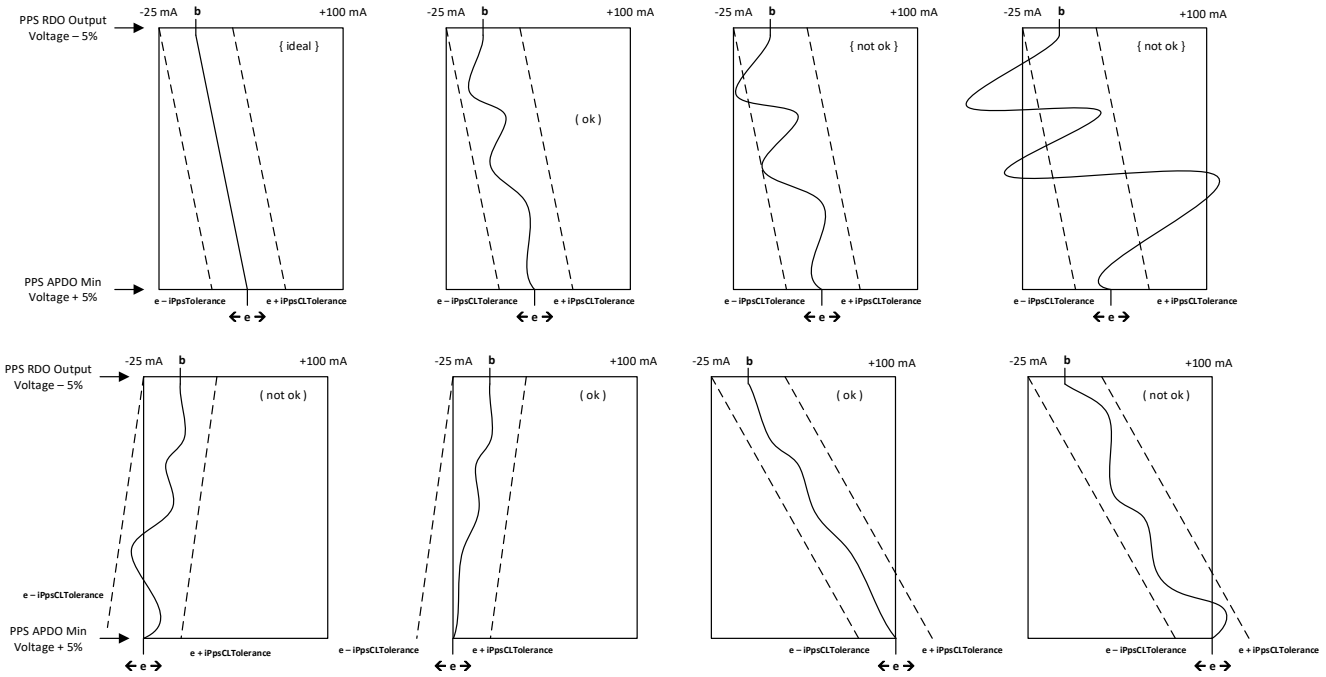
Notes:

- Point *a* represents entry into the transition region between Constant Voltage mode and Current Limit mode.
- Point *b* represents exit from the transition region between Constant Voltage mode and Current Limit mode.
- Point *c* represents the exit from the ***iPpsCLNew*** region as the voltage drops below the PPS APDO Min Voltage. The Source ***May*** disconnect at any point inside the tolerance range of the minimum voltage defined in the PPS APDO.
- ~~Point *b* is where the allowable increase in current up to ***iPpsCLOperating*** begins.~~
- ~~Point *c* represents the behavior as the load resistance decreases during Current Limit mode. See Table 7-22 for the allowed change in Operating Current (***iPpsCLOperating***) during this behavior.~~
- ~~Point *d* represents the behavior as the load resistance increases during Current Limit mode. See Table 7-22 for the allowed change in Operating Current (***iPpsCLOperating***) during this behavior.~~
- ~~Point e represents the exit from the ***iPpsCLOperating*** region.~~

(h). Figure 7-8, P284

From Text:

Figure 7-8 iPpsCLOperatingDetail



To Text:

Remove Figure

(i). Section 7.2.3.1, P300

From Text:

A Sink is not required to transition to Sink Standby when operating within the negotiated PPS APDO. A Sink ***May*** consume the Operating Current value in the PPS RDO during PPS output Voltage changes. However, prior to operating the SPR PPS in Current Limit, the Sink ***Shall*** program the PPS Operating Voltage to the lowest practical level that satisfies the Sink load requirement. Doing so will minimize the inrush current that occurs when the transition to Current Limit occurs. When operating with an SPR PPS that is in Current Limit, the Sink ***Shall Not*** change its load in a manner that exceeds ***iPpsCLLoadStepRate*** or ***iPpsCLLoadReleaseRate***. The load change magnitude ***Shall Not*** exceed ***iPpsCLLoadStep*** or ***iPpsCLLoadRelease***.

To Text:

A Sink is not required to transition to Sink Standby when operating within the negotiated PPS APDO. A Sink ***May*** consume the Operating Current value in the PPS RDO during PPS output Voltage changes. However, prior to operating the SPR PPS in Current Limit, the Sink ***Shall*** program the PPS Operating Voltage to the lowest practical level that satisfies the Sink load requirement. Doing so will minimize the inrush current that occurs when the transition to Current Limit occurs. When operating with an SPR PPS Source that is in Current Limit, the Sink ***Shall Not*** request a change to the Current Limit setpoint ~~its load in a manner~~ that exceeds ***iPpsCLLoadStepRate*** ~~or~~

~~***iPpsCLLoadReleaseRate***. The load change magnitude ***Shall Not*** exceed ***iPpsCLLoadStep*** or ***iPpsCLLoadRelease***.~~

(j). Section 7.4.1, Table 7-24, P352

From Text:

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
cSrcBulk[1]	Source bulk capacitance when a Port is powered from a dedicated supply.	10			µF	Section 7.1.2
cSrcBulkShared[1]	Source bulk capacitance when a Port is powered from a shared supply.	120			µF	Section 7.1.2
iPpsCLMin	SPR PPS Minimum Current Limit setting.	1			A	Section 7.1.4.2.2
iPpsCLNew	Current Limit accuracy					Section 7.1.4.2.2
	1A ≤ Operating Current ≤ 3A	-150		150	mA	
	Operating current > 3A	-5		5	%	
iPpsCLOperating	Total allowed change in Operating Current from point b in Figure 7-7 as the load resistance changes during Current Limit mode.	-25		100	mA	Figure 7-7
iPpsCLStep	SPR PPS Current Limit programming step size.		50		mA	Section 7.1.4.2.2
iPpsCLTolerance	Allowable deviation of the operating current along the load line between the point b and e as shown in Figure 7-8.	-25		25	mA	Figure 7-8
iPpsCLTransient	Allowed output current overshoot when a load increase occurs while in CL mode.			New load + 100	mA	Section 7.1.4.2.2
	Allowed output current undershoot when a load decrease occurs while in CL mode.	New load – 100			mA	
iPpsCVCLTransient	CV to CL transient current bounds assuming the Operating Voltage reduction of Section 7.2.3.1.	***iPpsCLNew*** - 100		New load + 500	mA	Section 7.1.4.2.2
tAvsTransient	he maximum time for the Adjustable Voltage Supply to be between ***vAvsNew*** and ***vAvsValid*** in response to a load transient.			5	ms	Section 7.1.8.2

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
tAvsSrcTransLarge	The time the Adjustable Voltage Supply set-point ***Shall*** transition between requested Voltages for steps larger than ***vAvsSmallStep***.	0		700	ms	Section 7.1.4.3.1
tAvsSrcTransSmall	The time the Adjustable Voltage Supply set-point ***Shall*** transition between requested Voltages for steps smaller than ***vAvsSmallStep***.	0		50	ms	Section 7.1.4.3.1
tNewSnk	Time allowed for an initial Source in Swap Standby to transition new Sink operation.			15	ms	Figure 7-28, Figure 7-29
tPpsCLCVTransient	CL to CV transient Voltage settling time.			25	ms	Section 7.1.4.2.2
tPpsCLProgramSettle	SPR PPS Current Limit programming settling time.			250	ms	Section 7.1.4.2.2
tPpsCLSettle	CL load transient current settling time.			250	ms	Section 7.1.4.2.2
tPpsCVCLTransient	CV to CL transient settling time.			250	ms	Section 7.1.8.1
tPpsSrcTransLarge	The time the Programmable Power Supply's set-point ***Shall*** transition between requested Voltages for steps larger than ***vPpsSmallStep***.	0		275	ms	Section 7.3.16 Section 7.3.17
tPpsSrcTransSmall	The time the Programmable Power Supply's set-point ***Shall*** transition between requested Voltages for steps less than or equal to ***vPpsSmallStep***.	0		25	ms	Section 7.3.16 Section 7.3.17
tPpsTransient	The maximum time for the Programmable Power Supply to be between ***vPpsNew*** and ***vPpsValid*** in response to a load transient when target load is greater than or equal to 60mA.			5	ms	Section 7.1.8.1
	The maximum time for the Programmable Power Supply to be between ***vPpsNew*** and ***vPpsValid*** in response to a load transient when target load is less than 60mA.			150	ms	Section 7.1.8.1

Parameter		Description	MIN	TYP	MAX	UNITS	Reference
tSrcFRSwap		Time from the initial Sink detecting that V_{BUS} has dropped below *vSafe5V* until the initial Sink/new Source is able to supply USB Type-C® Current (see *[USB Type-C 2.2]*)			150	µs	Section 7.1.13
tSrcReady	SPR Mode	Time from positive/negative transition start (t0) to when the Source is ready to provide the newly negotiated power level. Applies only to SPR mode voltage transitions.			285	ms	Figure 7-2, Figure 7-3
	EPR Mode	Time from positive/negative transition start (t0) to when the Source is ready to provide the newly negotiated power level. Applies to EPR mode voltage transitions and any voltage transition that either begins or ends in EPR mode.			720		
tSrcRecover	SPR Mode	Time allotted for the Source to recover.	0.66		1.0	s	Section 7.1.5
	EPR Mode		1.085		1.425		
tSrcSettle	SPR Mode	Time from positive/negative transition start (t0) to when the transitioning Voltage is within the range *vSrcNew*. Applies only to SPR mode voltage transitions.			275	ms	Figure 7-2
	EPR Mode	Time from positive/negative transition start (t0) to when the transitioning Voltage is within the range *vAvsNew*. Applies to EPR mode voltage transitions and any voltage transition that either begins or ends in EPR mode.			700		
tSrcSwapStdby		The maximum time for the Source to transition to Swap Standby.			650	ms	Table 7-9 Table 7-10
tSrcTransient		The maximum time for the Source output Voltage to be between *vSrcNew* and *vSrcValid* in response to a load transient when target load is greater or equal to than 60mA.			5	ms	Section 7.1.8

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
	The maximum time for the Source output Voltage to be between ***vSrcNew*** and ***vSrcValid*** in response to a load transient when target load is less than 60mA.			150	ms	Section 7.1.8
tSrcTransition	The time the Source ***Shall*** wait before transitioning the power supply to ensure that the Sink has sufficient time to prepare.	25		35	ms	Section 7.3
tSrcTurnOn	Transition time from ***vSafe0V*** to ***vSafe5V***.			275	ms	Table 7-12 Table 7-13
vAvsMaxVoltage	Maximum Voltage Field in the Adjustable Voltage Supply APDO.	APDO Max Voltage *0.95		APDO Max Voltage * 1.05	V	Section 7.1.4.3.1
vAvsMinVoltage	Minimum Voltage Field in the Adjustable Voltage Supply APDO.	APDO Min Voltage *0.95		APDO Min Voltage * 1.05	V	Section 7.1.4.3.1
vAvsNew	Adjustable RDO Output Voltage measured at the Source receptacle.	RDO Output Voltage *0.95	RDO Output Voltage	RDO Output Voltage *1.05	V	Section 7.1.8.2
vAvsSlewNeg	Adjustable Voltage Supply maximum slew rate for negative Voltage changes.			-30	mV/µs	Section 7.1.8.2
vAvsSlewPos	Adjustable Voltage Supply maximum slew rate for positive Voltage changes.			30	mV/µs	Section 7.1.8.2
vAvsSmallStep	Adjustable Voltage Supply step size defined as a small step relative to the previous ***vAvsNew***.	-1.0		1.0	V	Section 7.1.4.3.1
vAvsStep	Adjustable Voltage Supply Voltage programming step size.		100		mV	Section 7.1.8.2
vAvsValid	The range in addition to ***vAvsNew*** which the Adjustable Voltage Supply output is considered ***Valid*** during and after a transition as well as in response to a transient load condition.	-0.5		0.5	V	Section 7.1.8.2
vPpsCLCVTransient	CL to CV load transient Voltage bounds.	Operating Voltage * 0.95 – 0.1V		Operating Voltage * 1.05 + 0.1V	V	Section 7.1.4.2.2

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
vPpsMaxVoltage	Maximum Voltage Field in the Programmable Power Supply APDO.	APDO Max Voltage *0.95		APDO Max Voltage * 1.05	V	Section 7.1.4.2.1
vPpsMinVoltage	Minimum Voltage Field in the Programmable Power Supply APDO.	APDO Min Voltage *0.95		APDO Min Voltage * 1.05	V	Section 7.1.4.2.1
vPpsNew	Programmable RDO Output Voltage measured at the Source receptacle.	RDO Output Voltage *0.95	RDO Output Voltage	RDO Output Voltage *1.05	V	Section 7.1.8.1
vPpsShutdown	The Voltage at which the SPR PPS shuts down when operating in CL.	APDO Minimum Voltage * 0.85		APDO Minimum Voltage * 0.95	V	Section 7.1.4.2.2
vPpsSlewNeg	Programmable Power Supply maximum slew rate for negative Voltage changes			-30	mV/µs	Section 7.1.8.1
vPpsSlewPos	Programmable Power Supply maximum slew rate for positive Voltage changes			30	mV/µs	Section 7.1.8.1
vPpsSmallStep	PPS Step size defined as a small step relative to the previous ***vPpsNew***.	-500		500	mV	Section 7.1.4.2.1
vPpsStep	PPS Voltage programming step size.		20		mV	Section 7.1.8.1
vPpsValid	The range in addition to ***vPpsNew*** which the Programmable Power Supply output is considered ***Valid*** in response to a load step.	-0.1		0.1	V	Section 7.1.8.1
vSrcNeg	Most negative Voltage allowed during transition.			-0.3	V	Figure 7-10
vSrcNew	Fixed Supply output measured at the Source receptacle.	PDO Voltage *0.95	PDO Voltage	PDO Voltage *1.05	V	Figure 7-2 Figure 7-3
	Variable Supply output measured at the Source receptacle.	PDO Minimum Voltage		PDO Maximum Voltage	V	
	Battery Supply output measured at the Source receptacle.	PDO Minimum Voltage		PDO Maximum Voltage	V	
vSrcPeak	The range that a Fixed Supply or EPR AVS in Peak Current operation is allowed when overload conditions occur.	PDO Voltage *0.90		PDO Voltage *1.05	V	Table 6-10 Table 6-15 Figure 7-15

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
vSrcSlewNeg	Maximum slew rate allowed for negative Voltage transitions. Limits current based on a 3 A connector rating and maximum Sink bulk capacitance of 100 µF.			-30	mV/µs	Section 7.1.4.2 Figure 7-3
vSrcSlewPos	Maximum slew rate allowed for positive Voltage transitions. Limits current based on a 3 A connector rating and maximum Sink bulk capacitance of 100 µF.			30	mV/µs	Section 7.1.4 Figure 7-2
vSrcValid	The range in addition to *vSrcNew* which a newly negotiated Voltage is considered ***Valid*** during and after a transition as well as in response to a transient load condition. This range also applies to *vSafe5V*.	-0.5		0.5	V	Figure 7-2 Figure 7-3 Section 7.1.8
Note 1: The Source ***Shall*** charge and discharge the total bulk capacitance to meet the transition time requirements.						

To Text:

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
cSrcBulk[1]	Source bulk capacitance when a Port is powered from a dedicated supply.	10			µF	Section 7.1.2
cSrcBulkShared[1]	Source bulk capacitance when a Port is powered from a shared supply.	120			µF	Section 7.1.2
DNL (Differential Non-Linearity)	Deviation between ideal analog values corresponding to adjacent input digital values	-1	0	+1	LSB	Section 7.1.4.2.1
iPpsCLMin	SPR PPS Minimum Current Limit setting.	1			A	Section 7.1.4.2.2
iPpsCLNew	Current Limit accuracy					Section 7.1.4.2.2
	1A ≤ Operating Current ≤ 3A	-150		150	mA	
	Operating current > 3A	-5		5	%	
~~***iPpsCLOperating***~~	~~Total allowed change in Operating Current from point b in Figure 7-7 as the load resistance changes during Current Limit mode.~~	~~-25~~		~~100~~	~~mA~~	~~Figure 7-7~~
iPpsCLStep	SPR PPS Current Limit programming step size. (1 LSB)		50		mA	Section 7.1.4.2.2

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
iPpsCLLoadReleaseRate	Maximum load decrease slew rate during Current Limit setpoint changes.	-150			mA/µs	Section 7.1.4.2.2
iPpsCLLoadStepRate	Maximum load increase slew rate during Current Limit setpoint changes.			150	mA/µs	Section 7.1.4.2.2
~~***iPpsCLTolerance***~~	~~Allowable deviation of the operating current along the load line between the point b and c as shown in Figure 7-8.~~	~~-25~~		~~25~~	~~mA~~	~~Figure 7-8~~
iPpsCLTransient	Allowed output current overshoot when a load increase occurs while in CL mode.			New load + 100	mA	Section 7.1.4.2.2
	Allowed output current undershoot when a load decrease occurs while in CL mode.	New load – 100			mA	
iPpsCVCLTransient	CV to CL transient current bounds assuming the Operating Voltage reduction of Section 7.2.3.1.	***iPpsCLNew*** - 100		New load + 500	mA	Section 7.1.4.2.2
tAvsTransient	he maximum time for the Adjustable Voltage Supply to be between ***vAvsNew*** and ***vAvsValid*** in response to a load transient.			5	ms	Section 7.1.8.2
tAvsSrcTransLarge	The time the Adjustable Voltage Supply set-point ***Shall*** transition between requested Voltages for steps larger than ***vAvsSmallStep***.	0		700	ms	Section 7.1.4.3.1
tAvsSrcTransSmall	The time the Adjustable Voltage Supply set-point ***Shall*** transition between requested Voltages for steps smaller than ***vAvsSmallStep***.	0		50	ms	Section 7.1.4.3.1
tNewSnk	Time allowed for an initial Source in Swap Standby to transition new Sink operation.			15	ms	Figure 7-28, Figure 7-29
tPpsCLCVTransient	CL to CV transient Voltage settling time.			275	ms	Section 7.1.4.2.2
tPpsCLProgramSettle	SPR PPS Current Limit programming settling time.			250	ms	Section 7.1.4.2.2
tPpsCLSettle	CL load transient current settling time.			250	ms	Section 7.1.4.2.2
tPpsCVCLTransient	CV to CL transient settling time.			250	ms	Section 7.1.8.1

Parameter		Description	MIN	TYP	MAX	UNITS	Reference
tPpsSrcTransLarge		The time the Programmable Power Supply's set-point ***Shall*** transition between requested Voltages for steps larger than ***vPpsSmallStep***.	0		275	ms	Section 7.3.16 Section 7.3.17
tPpsSrcTransSmall		The time the Programmable Power Supply's set-point ***Shall*** transition between requested Voltages for steps less than or equal to ***vPpsSmallStep***.	0		25	ms	Section 7.3.16 Section 7.3.17
tPpsTransient		The maximum time for the Programmable Power Supply to be between ***vPpsNew*** and ***vPpsValid*** in response to a load transient when target load is greater than or equal to 60mA.			5	ms	Section 7.1.8.1
		The maximum time for the Programmable Power Supply to be between ***vPpsNew*** and ***vPpsValid*** in response to a load transient when target load is less than 60mA.			150	ms	Section 7.1.8.1
tSrcFRSwap		Time from the initial Sink detecting that V_{BUS} has dropped below ***vSafe5V*** until the initial Sink/new Source is able to supply USB Type-C® Current (see *Error! Reference source not found.*)			150	µs	Section 7.1.13
tSrcReady	SPR Mode	Time from positive/negative transition start (t0) to when the Source is ready to provide the newly negotiated power level. Applies only to SPR mode voltage transitions.			285	ms	Figure 7-2, Figure 7-3
	EPR Mode	Time from positive/negative transition start (t0) to when the Source is ready to provide the newly negotiated power level. Applies to EPR mode voltage transitions and any voltage transition that either begins or ends in EPR mode.			720		
tSrcRecover	SPR Mode	Time allotted for the Source to recover.	0.66		1.0	s	Section 7.1.5

Parameter		Description	MIN	TYP	MAX	UNITS	Reference
	EPR Mode		1.085		1.425		
tSrcSettle	SPR Mode	Time from positive/negative transition start (t0) to when the transitioning Voltage is within the range ***vSrcNew***. Applies only to SPR mode voltage transitions.			275	ms	Figure 7-2
	EPR Mode	Time from positive/negative transition start (t0) to when the transitioning Voltage is within the range ***vAvsNew***. Applies to EPR mode voltage transitions and any voltage transition that either begins or ends in EPR mode.			700		
tSrcSwapStdby		The maximum time for the Source to transition to Swap Standby.			650	ms	Table 7-9 Table 7-10
tSrcTransient		The maximum time for the Source output Voltage to be between ***vSrcNew*** and ***vSrcValid*** in response to a load transient when target load is greater or equal to than 60mA.			5	ms	Section 7.1.8
		The maximum time for the Source output Voltage to be between ***vSrcNew*** and ***vSrcValid*** in response to a load transient when target load is less than 60mA.			150	ms	Section 7.1.8
tSrcTransition		The time the Source ***Shall*** wait before transitioning the power supply to ensure that the Sink has sufficient time to prepare.	25		35	ms	Section 7.3
tSrcTurnOn		Transition time from ***vSafe0V*** to ***vSafe5V***.			275	ms	Table 7-12 Table 7-13
vAvsMaxVoltage		Maximum Voltage Field in the Adjustable Voltage Supply APDO.	APDO Max Voltage *0.95		APDO Max Voltage * 1.05	V	Section 7.1.4.3.1
vAvsMinVoltage		Minimum Voltage Field in the Adjustable Voltage Supply APDO.	APDO Min Voltage *0.95		APDO Min Voltage * 1.05	V	Section 7.1.4.3.1
vAvsNew		Adjustable RDO Output Voltage measured at the Source receptacle.	RDO Output Voltage *0.95	RDO Output Voltage	RDO Output Voltage *1.05	V	Section 7.1.8.2

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
vAvsSlewNeg	Adjustable Voltage Supply maximum slew rate for negative Voltage changes.			-30	mV/µs	Section 7.1.8.2
vAvsSlewPos	Adjustable Voltage Supply maximum slew rate for positive Voltage changes.			30	mV/µs	Section 7.1.8.2
vAvsSmallStep	Adjustable Voltage Supply step size defined as a small step relative to the previous ***vAvsNew***.	-1.0		1.0	V	Section 7.1.4.3.1
vAvsStep	Adjustable Voltage Supply Voltage programming step size.		100		mV	Section 7.1.8.2
vAvsValid	The range in addition to ***vAvsNew*** which the Adjustable Voltage Supply output is considered ***Valid*** during and after a transition as well as in response to a transient load condition.	-0.5		0.5	V	Section 7.1.8.2
vPpsCLCVTransient	CL to CV load transient Voltage bounds.	Operating Voltage * 0.95 – 0.1V		Operating Voltage * 1.05 + 0.1V	V	Section 7.1.4.2.2
vPpsMaxVoltage	Maximum Voltage Field in the Programmable Power Supply APDO.	APDO Max Voltage *0.95		APDO Max Voltage * 1.05	V	Section 7.1.4.2.1
vPpsMinVoltage	Minimum Voltage Field in the Programmable Power Supply APDO.	APDO Min Voltage *0.95		APDO Min Voltage * 1.05	V	Section 7.1.4.2.1
vPpsNew	Programmable RDO Output Voltage measured at the Source receptacle.	RDO Output Voltage *0.95	RDO Output Voltage	RDO Output Voltage *1.05	V	Section 7.1.8.1
vPpsShutdown	The Voltage at which the SPR PPS shuts down when operating in CL.	APDO Minimum Voltage * 0.85		APDO Minimum Voltage * 0.95	V	Section 7.1.4.2.2
vPpsSlewNeg	Programmable Power Supply maximum slew rate for negative Voltage changes			-30	mV/µs	Section 7.1.8.1
vPpsSlewPos	Programmable Power Supply maximum slew rate for positive Voltage changes			30	mV/µs	Section 7.1.8.1
vPpsSmallStep	PPS Step size defined as a small step relative to the previous ***vPpsNew***.	-500		500	mV	Section 7.1.4.2.1

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
vPpsStep	PPS Voltage programming step size. (1 LSB)		20		mV	Section 7.1.8.1
vPpsValid	The range in addition to *vPpsNew* which the Programmable Power Supply output is considered ***Valid*** in response to a load step.	-0.1		0.1	V	Section 7.1.8.1
vSrcNeg	Most negative Voltage allowed during transition.			-0.3	V	Figure 7-10
vSrcNew	Fixed Supply output measured at the Source receptacle.	PDO Voltage *0.95	PDO Voltage	PDO Voltage *1.05	V	Figure 7-2 Figure 7-3
	Variable Supply output measured at the Source receptacle.	PDO Minimum Voltage		PDO Maximum Voltage	V	
	Battery Supply output measured at the Source receptacle.	PDO Minimum Voltage		PDO Maximum Voltage	V	
vSrcPeak	The range that a Fixed Supply or EPR AVS in Peak Current operation is allowed when overload conditions occur.	PDO Voltage *0.90		PDO Voltage *1.05	V	Table 6-10 Table 6-15 Figure 7-15
vSrcSlewNeg	Maximum slew rate allowed for negative Voltage transitions. Limits current based on a 3 A connector rating and maximum Sink bulk capacitance of 100 µF.			-30	mV/µs	Section 7.1.4.2 Figure 7-3
vSrcSlewPos	Maximum slew rate allowed for positive Voltage transitions. Limits current based on a 3 A connector rating and maximum Sink bulk capacitance of 100 µF.			30	mV/µs	Section 7.1.4 Figure 7-2
vSrcValid	The range in addition to *vSrcNew* which a newly negotiated Voltage is considered ***Valid*** during and after a transition as well as in response to a transient load condition. This range also applies to *vSafe5V*.	-0.5		0.5	V	Figure 7-2 Figure 7-3 Section 7.1.8
Note 1: The Source ***Shall*** charge and discharge the total bulk capacitance to meet the transition time requirements.						

(k). Section 7.4.2, Table 7-25, P358

From Text:

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
cSnkBulk[1]	Sink bulk capacitance on V_{BUS} at Attach and during FRS after the old Source stops sourcing and prior to establishing an Explicit Contract (see Appendix E for an example).	1		10	µF	Section 7.2.2
cSnkBulkPd[1]	Bulk capacitance on V_{BUS} a Sink is allowed after a successful negotiation.	1		100	µF	Section 7.2.2
iLoadReleaseRate	Load release di/dt.	-150			mA/µs	Section 7.2.6
iLoadStepRate	Load step di/dt.			150	mA/µs	Section 7.2.6
iNewFrsSink	Maximum current the new Sink can draw during a Fast Role Swap until the new Source applies Rp. Matches the required USB Type-C® Current field of the Fixed Supply PDO of the old Source's ***Sink_Capabilities*** Message.			Default USB current or 1.5 or 3.0	A	Section7.1.13
iOvershoot	Positive or negative overshoot when a load change occurs less than or equal to ***iLoadStepRate***; relative to the settled value after the load change.	-230		230	mA	Section 7.2.6
iPpsCLLoadRelease	Maximum load release decrease during Current Limit.	-500			mA	Section 7.2.3.1
iPpsCLLoadReleaseRate	Maximum load decrease slew rate during Current Limit.	-150			mA/µs	Section 7.2.3.1
iPpsCLLoadStep	Maximum load step increase during Current Limit.			500	mA	Section 7.2.3.1
iPpsCLLoadStepRate	Maximum load increase slew rate during Current Limit.			150	mA/µs	Section 7.2.3.1
iSafe0mA	Maximum current a Sink is allowed to draw when V_{BUS} is driven to ***vSafe0V***.			1.0	mA	Figure 7-31 Figure 7-32
iSnkSwapStdby	Maximum current a Sink can draw during Swap Standby. Ideally this current is very near to 0 mA largely influenced by Port leakage current.			2.5	mA	Section 7.2.7
pHubSusp	Suspend power consumption for a hub. 25mW + 25mW per downstream Port for up to 4 ports.			125	mW	Section 7.2.3
pSnkStdby	Maximum power consumption while in Sink Standby.			2.5	W	Section 7.2.3
pSnkSusp	Suspend power consumption for a peripheral device.			25	mW	Section 7.2.3
tNewSrc	Maximum time allowed for an initial Sink in Swap Standby to transition to new Source operation.			275	ms	Section 7.2.7 Table 7-9 Table 7-10

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
tSnkFRSwap	Time during a Fast Role Swap when the new Sink can draw no more than ***pSnkStdby***.			200	µs	Section 7.1.13
tSnkHardResetPrepare	Time allotted for the Sink power electronics to prepare for a Hard Reset.			15	ms	Table 7-13
tSnkNewPower	Maximum transition time between power levels.			15	ms	Section 7.2.3
tSnkRecover	Time for the Sink to resume USB Default Operation.			150	ms	Table 7-12
tSnkStdby	Time to transition to Sink Standby from Sink.			15	ms	Section 7.2.3
tSnkSwapStdby	Maximum time for the Sink to transition to Swap Standby.			15	ms	Section 7.2.7
vEprMax	Highest Voltage an EPR Sink is expected to tolerate			55	V	
vSprMax	Highest Voltage an SPR Sink is expected to tolerate			24	V	
Note 1: If more bypass capacitance than ***cSnkBulk*** max or ***cSnkBulkPd*** max is required in the device, then the device ***Shall*** incorporate some form of V_{BUS} surge current limiting as described in ***[USB 3.2]*** Section 11.4.4.1.						

To Text:

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
cSnkBulk[1]	Sink bulk capacitance on V_{BUS} at Attach and during FRS after the old Source stops sourcing and prior to establishing an Explicit Contract (see Appendix E for an example).	1		10	µF	Section 7.2.2
cSnkBulkPd[1]	Bulk capacitance on V_{BUS} a Sink is allowed after a successful negotiation.	1		100	µF	Section 7.2.2
iLoadReleaseRate	Load release di/dt.	-150			mA/µs	Section 7.2.6
iLoadStepRate	Load step di/dt.			150	mA/µs	Section 7.2.6
iNewFrsSink	Maximum current the new Sink can draw during a Fast Role Swap until the new Source applies Rp. Matches the required USB Type-C® Current field of the Fixed Supply PDO of the old Source's ***Sink_Capabilities*** Message.			Default USB current or 1.5 or 3.0	A	Section7.1.13

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
iOvershoot	Positive or negative overshoot when a load change occurs less than or equal to *iLoadStepRate*; relative to the settled value after the load change.	-230		230	mA	Section 7.2.6
~~*iPpsCLLoadRelease*~~	~~Maximum load release decrease during Current Limit.~~	~~-500~~			~~mA~~	~~Section 7.2.3.1~~
~~*iPpsCLLoadReleaseRate*~~	~~Maximum load decrease slew rate during Current Limit.~~	~~-150~~			~~mA/µs~~	~~Section 7.2.3.1~~
~~*iPpsCLLoadStep*~~	~~Maximum load step increase during Current Limit.~~			~~500~~	~~mA~~	~~Section 7.2.3.1~~
~~*iPpsCLLoadStepRate*~~	~~Maximum load increase slew rate during Current Limit.~~			~~150~~	~~mA/µs~~	~~Section 7.2.3.1~~
iPpsCLLoadStep	Maximum Current setpoint change while operating in CL mode	-500		500	mA	Section 7.2.3.1
iSafe0mA	Maximum current a Sink is allowed to draw when V_{BUS} is driven to *vSafe0V*.			1.0	mA	Figure 7-31 Figure 7-32
iSnkSwapStdby	Maximum current a Sink can draw during Swap Standby. Ideally this current is very near to 0 mA largely influenced by Port leakage current.			2.5	mA	Section 7.2.7
pHubSusp	Suspend power consumption for a hub. 25mW + 25mW per downstream Port for up to 4 ports.			125	mW	Section 7.2.3
pSnkStdby	Maximum power consumption while in Sink Standby.			2.5	W	Section 7.2.3
pSnkSusp	Suspend power consumption for a peripheral device.			25	mW	Section 7.2.3
tNewSrc	Maximum time allowed for an initial Sink in Swap Standby to transition to new Source operation.			275	ms	Section 7.2.7 Table 7-9 Table 7-10
tSnkFRSwap	Time during a Fast Role Swap when the new Sink can draw no more than *pSnkStdby*.			200	µs	Section 7.1.13
tSnkHardResetPrepare	Time allotted for the Sink power electronics to prepare for a Hard Reset.			15	ms	Table 7-13
tSnkNewPower	Maximum transition time between power levels.			15	ms	Section 7.2.3
tSnkRecover	Time for the Sink to resume USB Default Operation.			150	ms	Table 7-12
tSnkStdby	Time to transition to Sink Standby from Sink.			15	ms	Section 7.2.3
tSnkSwapStdby	Maximum time for the Sink to transition to Swap Standby.			15	ms	Section 7.2.7
vEprMax	Highest Voltage an EPR Sink is expected to tolerate			55	V	

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
vSprMax	Highest Voltage an SPR Sink is expected to tolerate			24	V	
Note 1: If more bypass capacitance than ***cSnkBulk*** max or ***cSnkBulkPd*** max is required in the device, then the device ***Shall*** incorporate some form of V_{BUS} surge current limiting as described in ***[USB 3.2]*** Section 11.4.4.1.						

(l). Section 10.2, 804

From Text:

In order to meet the expectations of the user, the Maximum Current/Power in the Source Capabilities PDO or APDO for Sources with a PDP Rating of x Watts ***Shall*** be as follows:

- Maximum current for Normative and ***Optional*** Fixed/Variable supply PDOs ***Shall*** be either RoundUp(x/Voltage) or RoundDown(x/Voltage) to the nearest 10mA.
- Maximum current for Programmable Power Supply APDOs ***Shall*** be as defined in Table 10-7. Note that when the Constant Power bit is set in the APDO, the programmable power supply's output current is as defined in Table 10-7 however the programmable power supply will limit its output current so that the product of its actual output Voltage times the output current does not exceed the PDP.
- Maximum current for Programmable Power Supply APDOs not defined in Table 10-7 ***Shall*** be RoundDown (x/Max Voltage) to the nearest 50mA.
- If a 5V Prog, 9V Prog, 15V Prog or 20V Prog Programmable Power Supply APDO is advertised when not required by Table 10-7, then the maximum current ***Shall*** be RoundDown (x/Prog Voltage) to the nearest 50mA. When the PPS Power Limited bit is clear the Source ***Shall*** provide this current at Max Voltage.
- Maximum power for ***Optional*** Battery supply PDOs ***Shall*** be ≤ x.

To Text:

In order to meet the expectations of the user, the Maximum Current/Power in the Source Capabilities PDO or APDO for Sources with a PDP Rating of x Watts ***Shall*** be as follows:

- Maximum current for Normative and ***Optional*** Fixed/Variable supply PDOs ***Shall*** be either RoundUp(x/Voltage) or RoundDown(x/Voltage) to the nearest 10mA.
- Maximum current for Programmable Power Supply APDOs ***Shall*** be as defined in Table 10-7. Note that when the Constant Power bit is set in the APDO, the programmable power supply's output current is as defined in Table 10-7 however the programmable power supply will limit its output current so that the product of its actual output Voltage times the output current does not exceed the PDP.
- Maximum current for Programmable Power Supply APDOs not defined in Table 10-7 ***Shall*** be RoundDown (x/Max Voltage) to the nearest 50mA.
- If a ~~5V Prog,~~ 9V Prog, 15V Prog or 20V Prog Programmable Power Supply APDO is advertised when not required by Table 10-7, then the maximum current ***Shall*** be RoundDown (x/Prog Voltage) to the nearest 50mA. When the PPS Power Limited bit is clear the Source ***Shall*** provide this current at Max Voltage.
- Maximum power for ***Optional*** Battery supply PDOs ***Shall*** be ≤ x.

(m). Section 10.2.3.2, Table 10-7, P809

USB Power Delivery ENGINEERING CHANGE NOTICE

From Text:

PDP Rating (W)	5V fixed	9V fixed	15V fixed	20V fixed	5V Prog[5]	9V Prog[5]	15V Prog[5]	20V Prog[5]
x < 15W	PDP/5[4]	-	-	-	PDP/5[1]	-	-	-
15W	3A	-	-	-	3A	-	-	-
15 < x < 27W	3A[3]	PDP/9[4]	-	-	3A[2]	PDP/9[1]	-	-
27W	3A[3]	3A	-	-	-	3A	-	-
27 < x < 45W	3A[3]	3A[3]	PDP/15[4]	-	-	3A[2]	PDP/15[1]	-
45W	3A[3]	3A[3]	3A	-	-	-	3A	-
45 < x < 60W	3A[3]	3A[3]	3A[3]	PDP/20[4]	-	-	3A[2]	PDP/20[1]
60W	3A[3]	3A[3]	3A[3]	3A	-	-	-	3A
60 < x < 100W	3A[3]	3A[3]	3A[3]	PDP/20[4]	-	-	-	PDP/20[1]
100W	3A[3]	3A[3]	3A[3]	5A	-	-	-	5A

Notes:

1. The SPR PPS APDOs Maximum Current field ***Shall*** advertise RoundDown (PDP/Prog Voltage) to the nearest 50mA.
2. The SPR PPS APDOs Maximum Current field ***Shall*** advertise at least 3A, but ***May*** advertise up to RoundDown (PDP/Prog Voltage) to the nearest 50mA.
3. The Fixed PDOs Maximum Current field ***Shall*** advertise at least 3A, but ***May*** advertise up to RoundUp (PDP/Voltage.) to the nearest 10mA. Requires a 5A cable if over 3A is advertised.
4. The Fixed PDOs Maximum Current field ***Shall*** advertise either RoundDown (PDP/Voltage) or RoundUp (PDP/Voltage) to the nearest 10mA.
5. Applies to APDOs regardless of value of the PPS Power Limited bit.

To Text:

PDP Rating (W)	5V fixed	9V fixed	15V fixed	20V fixed	~~5V Prog[5]~~	9V Prog[5]	15V Prog[5]	20V Prog[5]
x < 15W	PDP/5[4]	-	-	-	~~PDP/5[1]~~	-	-	-
15W	3A	-	-	-	~~3A~~	-	-	-
15 < x < 27W	3A[3]	PDP/9[4]	-	-	~~3A[2]~~	PDP/9[1]	-	-
27W	3A[3]	3A	-	-	~~-~~	3A	-	-
27 < x < 45W	3A[3]	3A[3]	PDP/15[4]	-	~~-~~	3A[2]	PDP/15[1]	-
45W	3A[3]	3A[3]	3A	-	~~-~~	-	3A	-
45 < x < 60W	3A[3]	3A[3]	3A[3]	PDP/20[4]	~~-~~	-	3A[2]	PDP/20[1]
60W	3A[3]	3A[3]	3A[3]	3A	~~-~~	-	-	3A
60 < x < 100W	3A[3]	3A[3]	3A[3]	PDP/20[4]	~~-~~	-	-	PDP/20[1]
100W	3A[3]	3A[3]	3A[3]	5A	~~-~~	-	-	5A

PDP Rating (W)	5V fixed	9V fixed	15V fixed	20V fixed	~~5V Prog~~[5]	9V Prog[5]	15V Prog[5]	20V Prog[5]

Notes:
1. The SPR PPS APDOs Maximum Current field ***Shall*** advertise RoundDown (PDP/Prog Voltage) to the nearest 50mA.
2. The SPR PPS APDOs Maximum Current field ***Shall*** advertise at least 3A, but ***May*** advertise up to RoundDown (PDP/Prog Voltage) to the nearest 50mA.
3. The Fixed PDOs Maximum Current field ***Shall*** advertise at least 3A, but ***May*** advertise up to RoundUp (PDP/Voltage.) to the nearest 10mA. Requires a 5A cable if over 3A is advertised.
4. The Fixed PDOs Maximum Current field ***Shall*** advertise either RoundDown (PDP/Voltage) or RoundUp (PDP/Voltage) to the nearest 10mA.
5. Applies to APDOs regardless of value of the PPS Power Limited bit.

(n). Section 10.2.3.2.1, Table 10-8, P809

From Text:

	Fixed Nominal Voltage			
	5V Prog	9V Prog	15V Prog	20V Prog
Maximum Voltage	5.9V	11V	16V	21V
Minimum Voltage	3.3V	3.3V	3.3V	3.3V

To Text:

	Fixed Nominal Voltage			
	~~5V Prog~~	9V Prog	15V Prog	20V Prog
Maximum Voltage	~~5.9V~~	11V	16V	21V
Minimum Voltage	~~3.35V~~	~~3.35~~V	~~3.35~~V	~~3.35~~V

(o). Section 10.2.3.2.2, P809

From Text:

The following examples illustrate what a power adapter that Advertises a particular PDP Rating ***May*** offer:

1. PDP 15W
   - 5V @ 3A and 5V Prog @ 3A is the baseline.
2. PDP 25W
   - 5V @ 3A, 9V @ 2.8A, 5V Prog @ 3A and 9V Prog @ 2.8A is the baseline.
   - 5V @ 3A, 9V @ 2.8A, 5V Prog @ >3A up to 5A and 9V Prog @ 2.8A (with a 5A cable)
3. PDP 27W
   - 5V @ 3A, 9V @ 3A, 9V Prog @ 3A is the baseline.
   - 5V @ 3A, 9V @ 3A, 5V Prog @ 3A and 9V Prog @ 3A can offer 5V Prog, but it is covered by the 9V Prog.
   - 5V @ 3A, 9V @ 3A, 5V Prog @ >3A up to 5A and 9V Prog @ 3A (with a 5A cable)

4. PDP 36W
    - 5V @ 3A, 9V @ 3A, 15 @ 2.4A, 9V Prog @ 3 A and 15V Prog @ 2.4A is the baseline.
    - 5V @ 3A, 9V @ 3A, 15 @ 2.4A, 5V Prog @ >3A up to 5A, 9V Prog @ >3A up to 4A and 15V Prog @ 2.4A (with a 5A cable)
5. PDP 50W
    - 5V @ 3A, 9V @ 3A, 15 @ 3A, 20V @ 2.5A, 15V Prog @ 3A, and 20V Prog @ 2.5A is the baseline.

The first example is a simple single output Voltage supply. Both the Fixed and Programmable outputs supply 3A.
The second example illustrates that there are multiple ways to meet the requirements. The first sub-bullet is the power that the power rules require. The second sub-bullet illustrates that the power supply can offer more power at a particular Voltage so long as it does not violate the power rules. In this case it offers 25W at both 5V and 9V.
The third example illustrates that there are multiple ways a 27W PDP Rated power adapter can be implemented and meet the power rules. The first sub-bullet shows that the 9V Prog @ 3A fully covers the 5V Prog @3A range so it is not necessary to Advertise both. The second and third sub-bullets illustrate that the power adapter can Advertise lower Voltages at higher currents than required so long as the power does not exceed the PDP.
The fourth example illustrates as the PDP Rating goes higher there are more possible combinations that meet the power rules. Although there are multiple ways to meet the power rules, while operating on SPR Mode no more than a combination of seven SPR PDOs and APDOs can be offered. While operating in EPR Mode, in addition to the seven SPR PDOs and APDOs, no more than 6 additional EPR PDOs may be offered.
The fifth example shows that the 15V Prog @ 3A fully covers the 9V Prog @3A range so it is not necessary to advertise both.

To Text:

The following examples illustrate what a power adapter that Advertises a particular PDP Rating ***May*** offer:

~~1. PDP 15W~~
- ~~5V @ 3A and 5V Prog @ 3A is the baseline.~~

~~2. PDP 25W~~
- ~~5V @ 3A, 9V @ 2.8A, 5V Prog @ 3A and 9V Prog @ 2.8A is the baseline.~~
- ~~5V @ 3A, 9V @ 2.8A, 5V Prog @ >3A up to 5A and 9V Prog @ 2.8A (with a 5A cable)~~

3. PDP 27W
    - 5V @ 3A, 9V @ 3A, 9V Prog @ 3A is the baseline.
    - ~~5V @ 3A, 9V @ 3A, 5V Prog @ 3A and 9V Prog @ 3A can offer 5V Prog, but it is covered by the 9V Prog.~~
    - ~~5V @ 3A, 9V @ 3A, 5V Prog @ >3A up to 5A and 9V Prog @ 3A (with a 5A cable)~~
4. PDP 36W
    - 5V @ 3A, 9V @ 3A, 15 @ 2.4A, 9V Prog @ 3 A and 15V Prog @ 2.4A is the baseline.
    - 5V @ 3A, 9V @ 3A, 15 @ 2.4A, ~~5V Prog @ >3A up to 5A,~~ 9V Prog @ >3A up to 4A (with a 5A cable) and 15V Prog @ 2.4A.
5. PDP 50W
    - 5V @ 3A, 9V @ 3A, 15 @ 3A, 20V @ 2.5A, 15V Prog @ 3A, and 20V Prog @ 2.5A is the baseline.

~~The first example is a simple single output Voltage supply. Both the Fixed and Programmable outputs supply 3A.~~
~~The second example illustrates that there are multiple ways to meet the requirements. The first sub-bullet is the power that the power rules require. The second sub-bullet illustrates that the power supply can offer more power at a particular Voltage so long as it does not violate the power rules. In this case it offers 25W at both 5V and 9V.~~

The ~~third~~first example illustrates a basic example of a supply that can only support 5V and 9V. ~~Both fixed and programmable outputs provide 3A that there are multiple ways a 27W PDP Rated power adapter can be implemented and meet the power rules. The first sub-bullet shows that the 9V Prog @ 3A fully covers the 5V Prog @3A range so it is not necessary to Advertise both. The second and third sub-bullets illustrate that the power adapter can Advertise lower Voltages at higher currents than required so long as the power does not exceed the PDP.~~

The ~~fourth~~second example illustrates as the PDP Rating goes higher there are more possible combinations that meet the power rules. Although there are multiple ways to meet the power rules, while operating ~~on~~in SPR Mode no more than a combination of seven SPR PDOs and APDOs can be offered. ~~While operating in EPR Mode, in addition to the seven SPR PDOs and APDOs, no more than 6~~4 ~~additional EPR PDOs may be offered.~~

The ~~fifth~~third example shows that the 15V Prog @ 3A fully covers the 9V Prog @3A range so it is not necessary to advertise both.