USB Type-C ENGINEERING CHANGE NOTICE

Title: Requirements for USB4™ Re-timer based Active Cables
Applied to: USB Type-C Specification Release 2.0, August 2019

Brief description of the functional changes proposed:
Adds new section 6.6.5 to describe electrical requirements for retimer based active cables

Benefits as a result of the proposed changes:
Define requirements for retimer based active cables

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
No known impacts.

An analysis of the hardware implications:
No known issues.

An analysis of the software implications:
No known issues.

An analysis of the compliance testing implications:
A new compliance test will need to be written to test active cables, but no known changes to existing tests are anticipated.

USB Type-C ENGINEERING CHANGE NOTICE

Actual Change Requested

(a). Section 6 Active Cables Page 261

From Text:

6 Active Cables

Active cables shall minimally support *USB 3.2* Gen 2x1 and may support *USB 3.2* Gen 1x2 or Gen 2x2. As multi-lane *USB 3.2* and multi-lane *USB 3.2* repeaters become common, all active cables will be required to support two lanes. Active cables shall support *USB PD* eMarkers and may support Alternate Modes and advertise them as defined in Section 6.7.

Short active cables supporting lengths up to 5 meters are designed to 'just work' like passive cables with no discernable difference from the user's perspective.

To Text:

6 Active Cables

Active cables shall minimally support *USB 3.2* Gen 2x1 and may support *USB 3.2* Gen 1x2 or Gen 2x2. As multi-lane *USB 3.2* ~~and multi-lane *USB 3.2*~~ repeaters become common, all active cables will be required to support two lanes. Active cables shall support *USB PD* eMarkers and may support Alternate Modes and advertise them as defined in Section 6.7.
All USB4 active cables shall be interoperable with Thunderbolt™3 as defined in the USB4 Specification (Chapter 13) and the USB Type-C Cable and Connector Specification (Chapter 6.7 and Appendices E and F).

Short active cables supporting lengths up to 5 meters ~~are designed to 'just work'~~ shall work in both directions and orientations and should function like passive cables ~~with no discernable difference~~ from the user's perspective.

(b). Section 6.6.5, Page 308

From Text: Insert a new section at 6.6.5
Increment existing section at 6.6.5 (Return Loss) to 6.6.6

To Text: Insert the new section text below.

6.6.5 USB4 active cable electrical requirements

6.6.5.1 Background

This section describes the electrical requirements and compliance testing for Active Cables. The compliance testing is defined to ensure interoperability in terms of data integrity and electrical specifications enabling the Active Cable to reliably receive an input signal and output a valid signal at its other end.

The active cable types are:

1) Retimer based active cable (this section is covering Retimer based cable for USB4 only, USB3 retimer cable is defined in Section 6.6.4)

2) Linear Redriver (LRD) based active cable (USB3.2 and USB4) (electrical spec not defined yet)

3) Linear Optic based cable (electrical spec not defined yet)

6.6.5.2 Electrical requirements apply for all active cable types

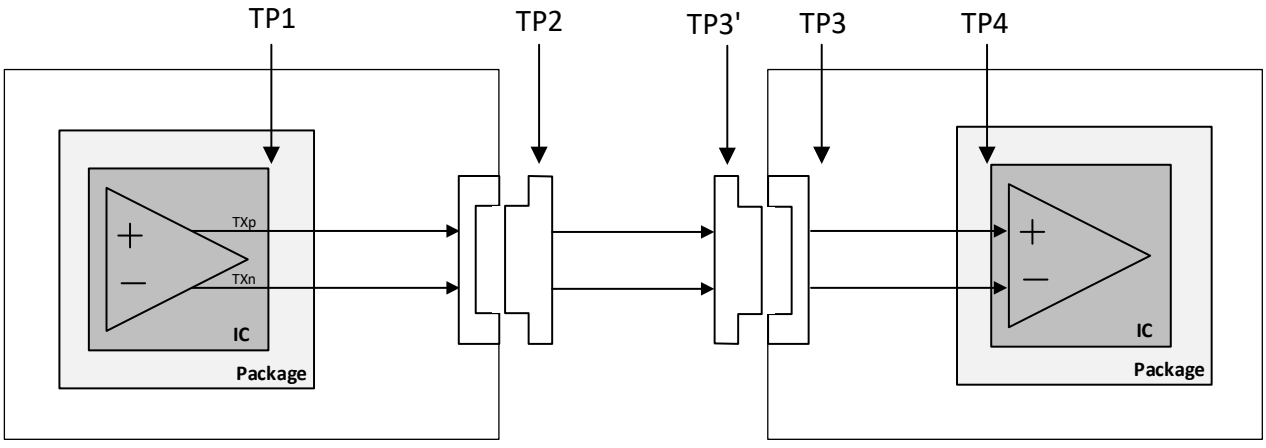
6.6.5.2.1 System compliance test point definition

All measurements shall be referenced to the following compliance points. Calibration shall be applied in cases where direct measurement is not feasible.

Test Point	Description	Comments
TP1	Transmitter IC output	Not used for electrical testing
TP2	Transmitter port connector output	Measured at the plug side of the connector
TP3	Receiver port connector output	Measured at the receptacle side of the connector. All the measurements at this point shall be done while applying reference equalization function
TP3'	Receiver port connector input	Measured at the plug side of the connector
TP4	Receiver IC input	Not used for electrical testing

Figure -1. Compliance Points Definition

Figure -2. Compliance Points Definition



6.6.5.2.2 Compliance Receptacle test boards

The USB Type-C high speed test fixture shall be used to enable cable compliance testing. The fixture shall

be comprised of a high-quality USB Type-C receptacle and a short PCB trace that may be connected to coaxial cable with SMA/SMP connector at its end. Because TP2 and TP3' reference points are located on the USB Type-C plug side of the connector, the loss and distortion of the receptacle fixture shall be calibrated such that all the measured values correspond to the standard reference points. The reference point TP3 is defined such that the insertion-loss from the connector pads to the compliance point is 0.5dB±0.25dB at 5GHz and 1dB±0.25dB at 10GHz. Extra loss and distortion elements shall be compensated by physical and/or mathematical means.

The target impedance of the fixture shall be 85 Ohms. AC coupling capacitors shall be placed on the receptacle test fixture following the Router Assembly requirements as specified in USB4 spec and CTS.

6.6.5.2.3 AC Coupling Capacitors

Active Cables shall include AC-coupling capacitance between 135nF and 265nF inside their plugs placed at the output transmit path and between 300nF and 363nF at the input receive path. Discharge resistors between 200Kohm and 242Kohm shall be placed at the input receive path. See Figure 3-3 in the USB4 Version 1.0 specification for a diagram of the AC-coupling capacitors and discharge resistors.
Active cable designs need to consider that a change of current consumption from VBUS as allowed by USB PD can add a considerable amount of common mode offset that may not be handled by the AC-coupling in this spec.

6.6.5.2.5 Differential Return-Loss mask - informative

Retimer and Redriver cable input and output return-loss measurements shall be referenced to a differential impedance of 85 Ω. When measured at TP3' and TP1 (respectively), the differential mode return loss recommended to not exceed the limits given in the following equation:

$$SDD22(f), SDD11(f) = \begin{cases} -12 & 0.05 < f_{GHz} \leq 3 \\ -7.5 + 7.5 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

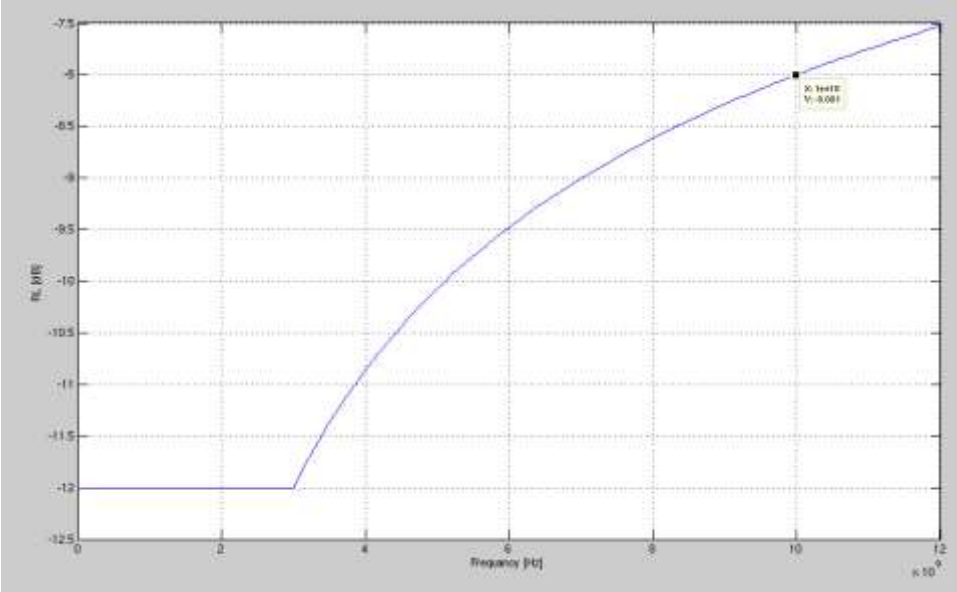


Figure 3 RX Differential Return-Loss Mask

6.6.5.3 Active Retiming Cable electrical specification

6.6.5.3.1 Background

This section describes the electrical requirements and compliance testing for USB4 Retimer based Active Cables.

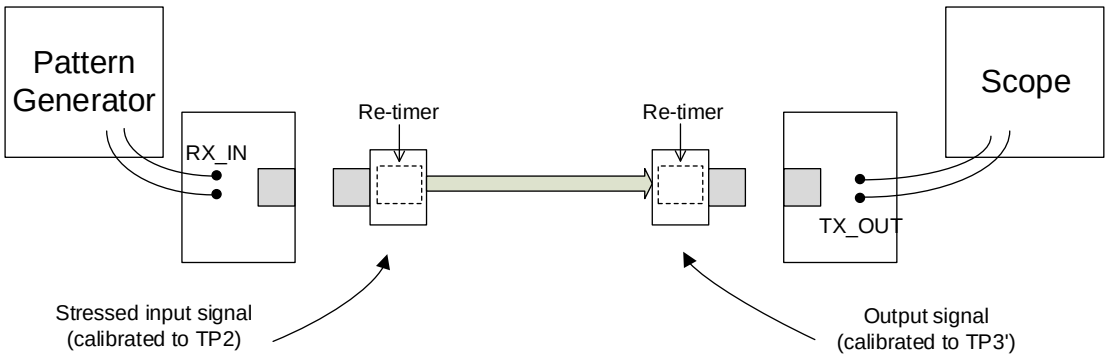
6.6.5.3.2 Active Retiming Cable Output Equalization

An Active Cable shall implement tunable 3-tap finite-impulse-response (FIR) equalization at its output. The transmit equalization shall support 16 preset configurations with different de-emphasis and pre-shoot settings as specified in the USB4 Base specification, and shall be measured at TP3'.

6.6.5.3.3 Active Retiming Cable High-Speed Specifications

Both ends of an Active Cable shall be tested for compliance. An Active cable is expected to reliably receive worst-case signal (referenced to TP2) and output the data at the other end with electrical characteristics that meet the requirements (referenced to TP3'). As shown in **Figure -4. Active Cable Compliance Test Setup**, a Compliance Receptacle shall be connected to both ends of the cable for calibrating the injected and measured signals to the corresponding TP2 and TP3' reference points.

Figure -4. Active Cable Compliance Test Setup



6.6.5.3.4 Active Retiming Cable Compliance Testing

Table -1. Active Retimer Cable Output Specifications Applied for All Speeds (at TP3') defines the Active Cable specifications for Gen 2 and Gen 3 systems at TP3'. These parameters shall be measured at the Active Cable's output while applying a stressed signal at the input as specified in **Table -2. Stressed Receiver Conditions for Gen 2 and Gen 3 Cable Compliance Testing (at TP2)**.

An Active Cable shall be tested by injecting several different periodic jitter components, one at a time. The test shall include sinusoidal jitter frequencies of 1MHz, 2 MHz, 10 MHz, 50MHz, and 100MHz. In all cases, the incoming signal shall include SSC modulation on top of the sinusoidal jitter component at the range of 300ppm to -5300ppm. PRBS31 pattern shall be used for Active Cable compliance testing. However, calibration of the stressed signal source may be performed with a periodic pattern shorter than PRBS31. AC common-mode noise shall be added at the pattern generator output to ensure worst-case transmitter characteristics. The total common-mode noise shall be 100mV peak-to-peak at TP2, where the added noise profile shall be sinewave at frequency not smaller than 400MHz. All the specified jitter values shall be calibrated while applying the reference CDR defined in the USB4 Base specification.

An Active Cable receiver may configure its Link Partner's TX equalizer during the Link establishment. The pattern generator shall support tunable 3-tap FIR at its output, which may be adjusted during the test by the receiver under test through out-of-band software channel.

Table -1. Active Retimer Cable Output Specifications Applied for All Speeds (at TP3')

Symbol	Description	Min	Max	Units	Comments
CABLE_BER	End to End bit error rate		1E-12		See note 1
AC_CM	Output AC Common Mode Voltage		100	mV pp	
LANE_TO_LANE_SKEW	Cable's Input-to-Output Skew between lanes		18	ns	
NRL	Noise Contributed by Integrated Return Loss				See 6.6.5.3.6

JTF_BW	Jitter tracking (forwarding) 3dB bandwidth from cable input to output		0.5	MHz	See Note 2
JTF_PEAKING	Jitter amplification from cable input to output		0.3	dB	Measured from 0 to 0.5 MHz. See Note 2
SSC_ VARIATION	SSC output to input down-spread variation	-0.3	0.3	dB	See Note 2
SSC_SLEW_RATE	SSC frequency slew rate (df/dt) during steady-state		1250	ppm/us	See Note 3
INIT_FREQ_VARIATION	Non-modulated transmit frequency accuracy during the initial stages of the training period	-300	300	ppm	See Note 4, 5
DELTA_FREQ_200ns	Transmit frequency variation over 200ns measurement windows following the switching from local to recovered clock		1400	ppm	See Note 4, 5
DELTA_FREQ_1000ns	Transmit frequency variation over 1us measurement windows following the switching from local to recovered clock		2200	ppm	See Note 4, 5
V_OUTPUT_DC_AC_CONN	Instantaneous DC+AC voltages at the cable output side of the AC coupling capacitors	-0.5 (min1) -0.3 (min2)	1.0	V	See Note 6
TJ	Total Jitter		0.32	UI pp	See Note 7, Note 9
UDJ	Deterministic jitter that is uncorrelated to the transmitted data		0.13	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter		0.06	UI pp	See Note 10
DCD	Deterministic Jitter Associated by Duty-Cycle-Distortion		0.03	UI pp	
Y1	Eye inner height at TP3' (one-sided voltage opening of the differential signal)	200		mV	Measured for 1E6 UI. See Note 8, Note 9, and the USB4 Base Specification
Y2	Eye outer height at TP3' (one-sided voltage opening of the differential signal)		650	mV	Measured for 1E6 UI. See Note 8, Note 9, and the USB4 Base Specification

Notes:

1. The cable BER requirement is referred to the raw data, without applying forward error correction nor pre-coding.
2. JTF_BW and JTF_PEAKING characterizes the corresponding input-to-output low-pass Jitter Transfer Function bandwidth and peaking. In addition, it is required that the cable will not change the SSC modulation depth by more than specified. For verifying that, the SSC down-spreading depth of the cable input and output shall be compared.
3. The SSC slew rate shall be extracted from the transmitted signal over measurement intervals of 0.5us. The SSC slew-rate shall be extracted from the transmitter phase after applying a 2nd order low-pass filter with 3dB point at 5 MHz. Steady-state clocking shall be applied from the point that SLOS training pattern is forwarded by the transmitter.
4. As shown in Figure-5. Example for Transmitter Frequency Variation during Clock Switching, the initial transmit frequency is not modulated. The transmit frequency variation following the switching from local to recovered clock shall be measured over time intervals of 200ns and 1us.
5. Measurement shall be performed over the transmitted signal. The signal phase shall be extracted while applying 2nd order low-pass filter with 3dB point at 5MHz.
6. The absolute single-ended voltage seen by the receiver. This requirement applies to all link states and during power-on, and power-off. (min1, max) is measured with a 200 KΩ receiver load, and (min2, max) is measured with a 50 Ω receiver load. The ground offset between the cable output and UFP is not included in V_OUTPUT_DC_AC_CONN.
7. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).
8. The output voltage is differential.
9. Transmit jitter shall be measured while applying the reference CDR described in the USB4 Base Specification. Note that the measured jitter includes residual SSC jitter passing the reference CDR.
10. UDJ_LF is the uncorrelated deterministic jitter measured after applying 2nd order Low-Pass-Filter with 3dB cut-off at 0.5 MHz on the measured jitter. This filter needs to be applied on top of the reference CDR rejection function. The measurement shall be performed while applying input stress signal with periodic jitter component of 100 MHz.

Figure -5. Example for Transmitter Frequency Variation during Clock Switching

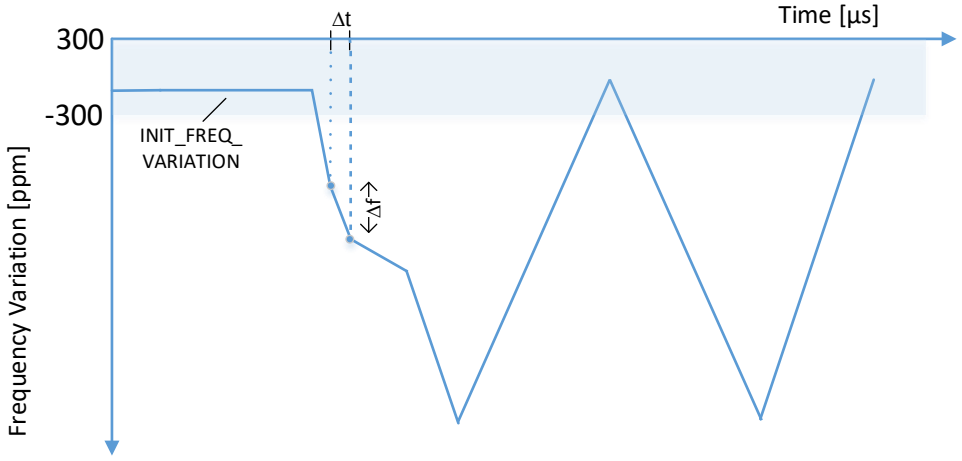
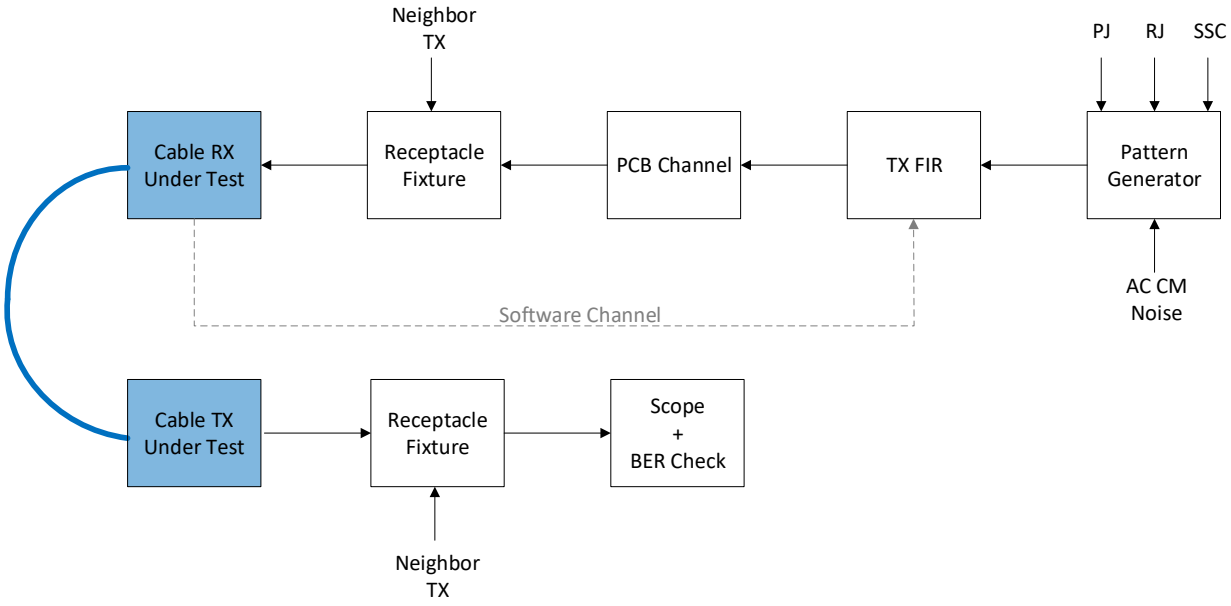


Table -2. Stressed Receiver Conditions for Gen 2 and Gen 3 Cable Compliance Testing (at TP2)

	Inner eye Voltage [mV peak]	Data Dependent Jitter (DDJ) [UI peak-to-peak]	Random Jitter [UI peak-to-peak]	Periodic Jitter [UI peak-to-peak]	Total Jitter [UI peak-to-peak]
Gen2	140	0.12	0.14	0.17	0.43
Gen3	120	0.15	0.14	0.17	0.46

Figure -6. Active Cable Test Setup



6.6.5.3.5 Active Retiming Cable Error-Bursts Testing

In order to facilitate proper FEC operation, an Active Cable receiver shall take steps to limit the probability that a burst of errors is restarted immediately after receiving one or more correct bits (see USB4 Base specification). The Cable receiver under test shall trigger on bit-errors and shall capture error events that follow.

The test setup shall be initialized with the same configuration used for testing the uncoded BER with periodic jitter component of 100MHz. As part of this setup, PRBS31 pattern is assumed and neither forward-error-correction nor pre-coding are applied. After initialization, the periodic jitter magnitude shall be increased to the point where uncoded BER of 1E-8 is observed. The receiver under test shall trigger on bit-error and shall capture error events that follow. An error event is defined as a mismatch between the received data and the reference PRBS31 pattern. At least 32 consecutive bits shall be examined for errors starting from the initial trigger. The probability for burst renewal shall be 5e-7 or less (i.e. one error burst restart per 2 million error captures). The following is an example analysis:

No burst restart: captured_data[31:0]=00000000000000000000001111111111

Burst restart: captured_data[31:0]=00000000000000000000111001111111

where '1' represents a bit error and '0' represents a correct bit, as expected from "exclusive or" (XOR) operation between the received bits and the synchronized reference PRBS31 pattern. captured_data[0] corresponds to the error event trigger.

Note: A burst of errors contains 1 or more consecutive bit errors.

6.6.5.3.6 Noise Contributed by Integrated Return Loss (NRL)

This section will be added in a future ECR.