USB Type-C ENGINEERING CHANGE NOTICE

Title: USB 3.2 Alignment Updates
Applied to: USB Type-C™ Specification Release 1.3

Brief description of the functional changes:
This ECN captures the necessary changes to align with the USB 3.2 update. The updates primarily focus on editorial content to inform that the second lane of the cable is now being used when in either USB Gen 1x2 or Gen 2x2 modes. A key part of this update is to normatively identify the Configuration Lane as the lane associated with TX1/RX1 of the plug/cable – USB 3.2 relies on this definition being here as opposed to independently defining it in USB 3.2. Also updated V_{BUS} and V_{CONN} to align with increased power defined in USB 3.2.

Benefits as a result of the changes:
Aligns the USB Type-C specification with USB 3.2 to aid developers to clearly understand the relationship between the two specifications. No substantive changes really needed to support USB 3.2 so the benefit is more for editorial harmony.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
No impact envisioned specific to this specification, clearly systems and devices are impacted by USB 3.2 if these are updated to implement dual-lane operation.

An analysis of the hardware implications:
No impact specific to this specification change.

An analysis of the software implications:
No impact specific to this specification change.

An analysis of the compliance testing implications:
No impact specific to this specification change.

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Actual Change

The following is the new or edited content for the USB Type-C spec ... it is presented as tracked changed text for the sections included below.

In addition to the changes captured below, the following list of editorial find and replace updates are needed throughout the document:

- **All references to USB 3.1 should be changed to USB 3.2 expect where the USB 3.1 references still need to apply for legacy cable and connector purposes.**
- **All references for USB 3.1 specific to legacy cable and connector specifications should be changed as needed to reference the USB 3.1 Legacy Cable and Connector specification.**

1.3 Related Documents

USB 3.2 *Universal Serial Bus Revision 3.2 Specification*
This includes the entire document release package.
http://www.usb.org/developers/docs

USB 3.1 Legacy Cable and Connector Specification, Revision 1.0
http://www.usb.org/developers/docs

1.5 Terms and Abbreviations

Term	Description
Configuration Lane	The USB 3.2 Configuration Lane is used to establish and manage dual-lane SuperSpeed USB operation. The Configuration Lane is specifically the SuperSpeed USB TX1/RX1 differential signal set in the cable/plug.
Dual-lane (x2)	USB 3.2 dual-lane operation is defined as simultaneously signaling on both sets of SuperSpeed USB transmit and receive differential pairs (TX1/RX1 and TX2/RX2 in the cable/plug).
Single-lane (x1)	USB 3.2 single-lane operation is defined as signaling on only one set of SuperSpeed USB transmit and receive differential pairs (TX1/RX1 in the cable/plug).
x1	See Single-lane.
x2	See Dual-lane.

2.1 Introduction

The USB Type-C™ receptacle, plug and cable provide a smaller, thinner and more robust alternative to legacy USB interconnect (Standard and Micro USB cables and connectors). This solution targets use in very thin platforms, ranging from ultra-thin notebook PCs down to smart phones where existing Standard-A and Micro-AB receptacles are deemed too large, difficult to use, or inadequately robust. Some key specific enhancements include:

- The USB Type-C receptacle may be used in very thin platforms as its total system height for the mounted receptacle is under 3 mm
- The USB Type-C plug enhances ease of use by being plug-able in either upside-up or upside-down directions
- The USB Type-C cable enhances ease of use by being plug-able in either direction between host and devices

While the USB Type-C interconnect no longer physically differentiates plugs on a cable by being an A-type or B-type, the USB interface still maintains such a host-to-device logical relationship. Determination of this host-to-device relationship is accomplished through a Configuration Channel (CC) that is connected through the cable. In addition, the Configuration Channel is used to set up and manage power and Alternate/Accessory Modes.

Using the Configuration Channel, the USB Type-C interconnect defines a simplified 5 volt VBUS-based power delivery and charging solution that supplements what is already defined in the *USB 3.2 Specification*. More advanced power delivery and battery charging features over the USB Type-C interconnect are based on the *USB Power Delivery Specification*. As a product implementation improvement, the USB Type-C interconnect shifts the *USB PD* communication protocol from being communicated over VBUS to being delivered across the USB Type-C Configuration Channel.

The USB Type-C receptacle, plug and cable designs are intended to support future USB functional extensions. As such, consideration was given to frequency scaling performance, pin-out arrangement and the configuration mechanisms when developing this solution. The definition of future USB functional extensions is not in the scope of this specification but rather will be provided in future releases of the base USB Specification, i.e., beyond the existing *USB 3.2 Specification*.

2.3 Configuration Process

The USB Type-C receptacle, plug and cable solution incorporates a configuration process to detect a downstream facing port to upstream facing port (Source-to-Sink) connection for VBUS management and host-to-device connected relationship determination.

The USB Type-C port configuration process is used for the following:

- Source-to-Sink attach/detach detection

- Plug orientation/cable twist detection
- Initial power (Source-to-Sink) detection and establishing the data (Host-to-Device) relationship
- USB Type-C VBUS current detection and usage
- *USB PD* communication
- Discovery and configuration of functional extensions

2.3.2 Plug Orientation/Cable Twist Detection

The USB Type-C plug can be inserted into a receptacle in either one of two orientations, therefore the CC pins enable a method for detecting plug orientation in order to determine the lane ordering of the SuperSpeed USB data signal pairs functionally connected through the cable and identifying the Configuration Lane for dual-lane operation when supported. This allows for signal routing, if needed, within a host or device to be established for a successful connection.

2.3.4 USB Type-C VBUS Current Detection and Usage

With the USB Type-C connector solution, a Source (host or downstream hub port) may implement higher source current over VBUS to enable faster charging of mobile devices or powering devices that require more current than is specified in the *USB 3.2 Specification*. All USB host and hub ports advertise via the CC pins the level of current that is presently available. The USB device port is required to manage its load to stay within the current level offered by the host or hub, including dynamically scaling back the load if the host or hub port changes its advertisement to a lower level as indicated over the CC pins.

Three current level advertisements at 5V VBUS are defined by USB Type-C Current:

- Default values when configured for high-power operation as defined by a USB Specification (500 mA for USB 2.0 ports; 900 mA or 1,500 mA for USB 3.2 ports operating in single-lane or dual-lane, respectively)
- USB Type-C Current @ 1.5 A
- USB Type-C Current @ 3.0 A

There is a clear functional distinction between advertising Default versus the USB Type-C Current at either 1.5 A or 3.0 A.

- Default is intended for host operation in providing bus power to a connected device where the host manages the device's current consumption for the low-power, high-power and suspend states as defined in the USB base specifications.

- USB Type-C Current at either 1.5 A or 3.0 A is primarily intended for charging applications. The Sink can vary its current draw up to the advertised limit. Offering USB Type-C Current at either 1.5 A or 3.0 A is allowed for a host providing bus power to a device. The host needs to assume that the device will continuously draw up to the offered limit.

3.7.2.2.3 Integrated Crosstalk between SuperSpeed Pairs (Normative)

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The port-to-port crosstalk (TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) is specified to support the usages in which all the four SuperSpeed pairs transmit or receive signals simultaneously, for example in SuperSpeed USB dual-lane operation.

4.1 Signal Summary

Table 4-1 summarizes the list of signals used on the USB Type-C connectors.

Table 4-1 USB Type-C List of Signals

Signal Group	Signal	Description
USB 3.1	**SSTXp1, SSTXn1** **SSRXp1, SSRXn1** **SSTXp2, SSTXn2** **SSRXp2, SSRXn2**	SuperSpeed USB serial data interface defines 1 differential transmit pair and 1 differential receive pair per lane. On a USB Type-C receptacle, two sets of SuperSpeed USB signal pins are defined to support dual-lane operation.
USB 2.0	**Dp1, Dn1** **Dp2, Dn2**	*USB 2.0* serial data interface defines a differential pair. On a USB Type-C receptacle, two set of *USB 2.0* signal pins are defined to enable plug flipping feature
Configuration	**CC1, CC2** (receptacle) **CC** (plug)	CC channel in the plug used for connection detect, interface configuration and VCONN
Auxiliary signals	**SBU1, SBU2**	Sideband Use
Power	**VBUS**	USB cable bus power
	VCONN (plug)	USB plug power
	GND	USB cable return current path

4.2.1 SuperSpeed USB Pins

SSTXp1, SSTXn1 **SSTXp2, SSTXn2**	These pins are required to implement the system's transmit path of a *USB 3.2* SuperSpeed interface. The transmitter differential pair in a port are routed to the receiver differential pair in the port at the opposite end of the path. The *USB 3.2 Specification* defines all electrical characteristics, enumeration, protocol, and management features for this interface. Two pairs of pins are defined to enable dual-lane operation – see Section 4.5.1.1 for further definition.
SSRXp1, SSRXn1 **SSRXp2, SSRXn2**	These pins are required to implement the system's receive path of a *USB 3.2* SuperSpeed interface. The receiver differential pair in a port are routed to the transmitter differential pair in the port at the opposite end of the path. The *USB 3.2 Specification* defines all electrical characteristics, enumeration, protocol, and management features for this interface. Two pairs of pins are defined to enable dual-lane operation – see Section 4.5.1.1 for further definition.

4.4.3 VCONN

VCONN is provided by the Source to power cables with electronics in the plug. VCONN is provided over the CC pin that is determined not to be connected to the CC wire of the cable.

Initially, VCONN shall be sourced on all Source USB Type-C receptacles that utilize the SSTX and SSRX pins during specific connection states as described in Section 4.5.2.2. Subsequently, VCONN may be removed under some circumstances as described in Table 4-4. VCONN may also be sourced by USB Type-C receptacles that do not utilize the SSTX and SSRX pins as described in Section 4.5.2.2. *USB PD* VCONN_Swap command also provides the Source a means to request that the attached Sink source VCONN.

Table 4.4 USB Type-C Source Port's VCONN Requirements Summary

D+/D–	SSTX/SSRX, VPD	> 3 A	VCONN Requirements
No	No	No	Not required to source VCONN
Yes	No	No	Not required to source VCONN
Yes	Yes	No	Required to source 1 W for x1 implementations and 1.5 W for x2 implementations. VCONN power may be removed after the source has read the cable's eMarker and has determined that it is not an active cable nor a VPD.
No	No	Yes	Required to source 100 mW. VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	No	Yes	Required to source 100 mW. VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	Yes	Yes	Required to source 1 W for x1 implementations and 1.5 W for x2 implementations. VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity and that it is not an active cable nor a VPD.

Table 4-5 provides the voltage and power requirements that shall be met for VCONN. See Section 4.9 for more details about Electronically Marked Cables. See Section 5.1 regarding optional support for an increased VCONN power range in Alternate Modes.

Table 4-5 VCONN Source Characteristics

	Minimum	Maximum	Notes
Voltage	3.0 V	5.5 V	
Power for Sources with SuperSpeed Signals	x1 1 W		Source may latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage. Source may disable VCONN per Table 4-4. Alternate modes may require higher power.
	x2 1.5 W		
Power for Sources with VPD support	1 W		Source may latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage.
Power for Sources in USB Suspend or without SuperSpeed Signals	100 mW		Minimum power Source must provide in USB Suspend or without SuperSpeed signals. Source may disable VCONN per Table 4-4.
Rdch	30 Ω	6120 Ω	Discharge resistance applied in UnattachedWait.SRC between the CC pin being discharged and GND.

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Table 4-6 provides the requirements that shall be met for cables that consume VCONN power.

Table 4-6 Cable VCONN Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0	5.5V	Voltage range at which this Table applies
Inrush Capacitance		10 µF	A cable shall not present more than the equivalent inrush capacitance to the VCONN source. The active cable is responsible for discharging its capacitance.
Power for Electronically Marked Passive Cables		20mW	See Section 4.9. Measured with no USB PD traffic at least 500ms after VCONN applied Note: 75mW max allowed for the first 500ms after VCONN applied.
Power for Active Cables when connected to a Source with SuperSpeed Signals		x1 1.0 W	See Section 5.2.
		x2 1.5 W	
Power for Active Cables when connected to a Source without SuperSpeed Signals or in USB Suspend		70mW	Maximum power for active cables in USB suspend or when connected to a Source without SuperSpeed signals. Measured with no USB PD traffic at least 500ms after VCONN applied Note: 100 mW max allowed for the first 500 ms after VCONN applied.
tVCONNDischarge		230ms	Time from cable disconnect to vVCONNDischarge met.
vVCONNDischarge		800mV	VCONN voltage after tVCONNDischarge
vRaReconnect	800mV		Voltage at which the cable shall reapply Ra on the falling edge of VCONN.

4.5.1.1 USB Data Bus Interface and USB Type-C Plug Flip-ability

Since the USB Type-C plug can be inserted in either right-side-up or upside-down position, the hosts and devices that support USB data bus functionality must operate on the signal

pins that are actually connected end-to-end. In the case of USB 2.0, this is done by shorting together the two D+ signal pins and the two D− signal pins in the host and device receptacles. In the case of SuperSpeed USB signals in a single-lane implementation, it requires the functional equivalent of a switch in both the host and device to appropriately route the SuperSpeed TX and RX signal pairs to the connected path through the cable. For a SuperSpeed USB dual-lane implementation, the host or device resolves the lane ordering.

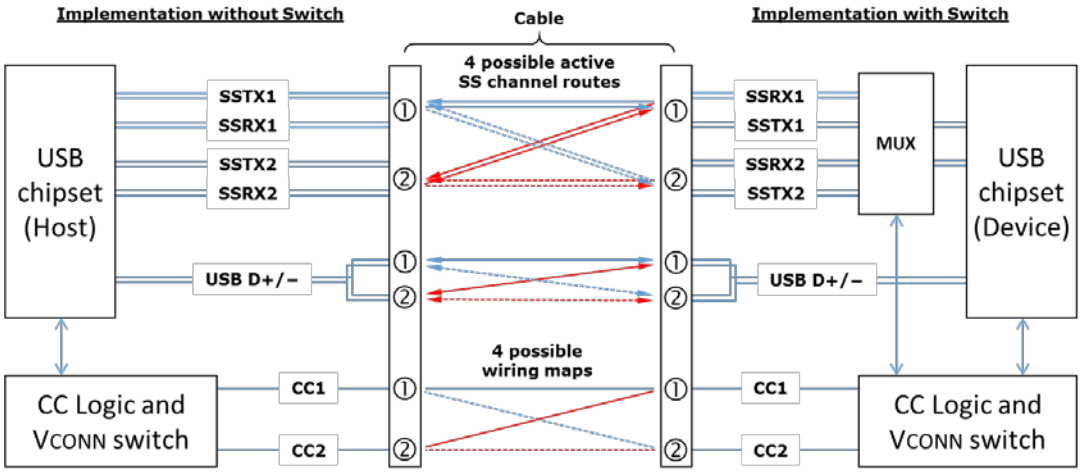
Figure 4-3 illustrates the logical data bus model for a USB Type-C-based Host connected to a USB Type-C-based Device. As illustrated, the device is shown as only capable of SuperSpeed USB single-lane operation. The USB cable that sits between a host and device can be in one of four possible connected states when viewed by the host:

- Un-flipped straight through – Position ① ⇔ Position ①
- Un-flipped twisted through – Position ① ⇔ Position ②
- Flipped straight through – Position ② ⇔ Position ②
- Flipped twisted through – Position ② ⇔ Position ①

To establish the proper routing of the active USB data bus from host to device, the standard USB Type-C cable is wired such that a single CC wire is position aligned with the first USB SuperSpeed signal pairs (SSTXp1/SSTXn1 and SSRXp1/SSRXn1) – in this way, the CC wire and SuperSpeed USB data bus wires that are used for single-lane operational signaling within the cable track with regard to the orientation and twist of the cable. By being able to detect which of the CC pins (CC1 or CC2) at the receptacle is terminated by the device, the host is able to determine which SuperSpeed USB signals are to be used for the single-lane connection and the host can use this to control the functional switch for routing the SuperSpeed USB signal pairs. Similarly in the device, detecting which of the CC pins at the receptacle is terminated by the host allows the device to control the functional switch that routes its SuperSpeed USB signal pairs.

For a dual-lane implementation, the SuperSpeed USB signal pairs in the cable/plug aligned with the CC wire/pin is Lane 0 and shall be identified as the Configuration Lane. The second SuperSpeed USB signal pairs (SSTXp2/SSTXn2 and SSRXp2/SSRXn2) in the cable/plug is Lane 1 of a dual-lane configuration.

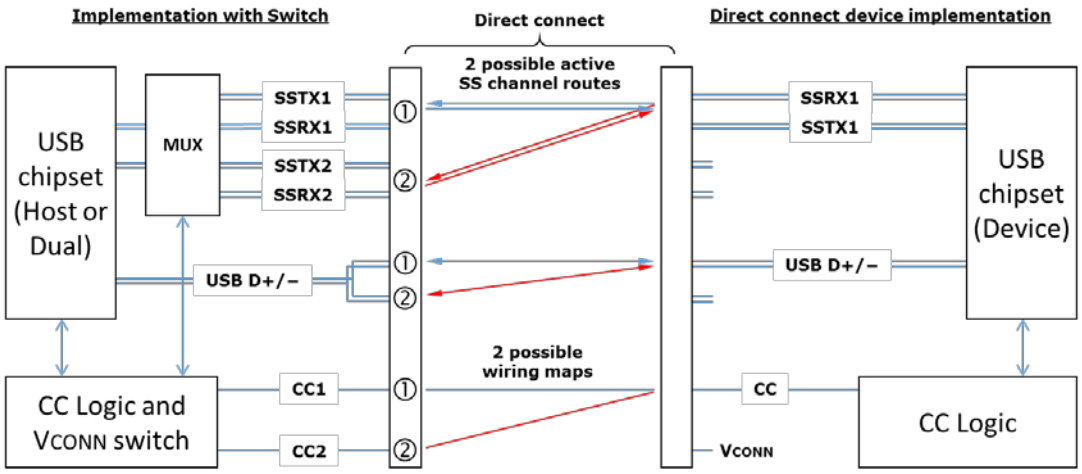
Figure 4-3 Logical Model for Single-lane Data Bus Routing across USB Type-C-based Ports



While Figure 4-3 illustrates the functional model as a host connected to a device, this model equally applies to a USB hub's downstream ports as well.

Figure 4-4 illustrates the logical data bus model for a USB Type-C-based Device (implemented with a USB Type-C plug either physically incorporated into the device or permanently attached as a captive cable) connected directly to a USB Type-C-based Host. As illustrated, the device is shown as only capable of SuperSpeed USB single-lane operation. For the device, the location of the SuperSpeed USB data bus, *USB 2.0* data bus, CC and VCONN pins are fixed by design. Given that the device pin locations are fixed, only two possible connected states exist when viewed by the host.

Figure 4-4 Logical Model for USB Type-C-based Ports for the Single-lane Direct Connect Device



The functional requirements for implementing SuperSpeed USB data bus routing for the USB Type-C receptacle are not included in the scope of this specification. There are multiple host, device and hub architectures that can be used to accomplish this which could include either discrete or integrated switching, and could include merging this functionality with other USB 3.1 design elements, e.g. a bus repeater.

4.6.2.1 USB Type-C Current

Default USB voltage and current are defined by the *USB 2.0* and *USB 3.2* specifications. All USB Type-C Current advertisements are at the USB VBUS voltage defined by these specifications.

The USB Type-C Current feature provides the following extensions:

- Higher current than defined by the *USB 2.0*, the *USB 3.2* or the *BC 1.2* specifications
- Allows the power source to manage the current it provides

The USB Type-C connector uses CC pins for configuration including an ability for a Source to advertise to its port partner (Sink) the amount of current it can supply:

- Default values when configured for high-power operation as defined by the USB Specification (500 mA for USB 2.0 ports; 900 mA or 1,500 mA for USB 3.2 ports in single-lane or dual-lane operation, respectively)
- 1.5 A
- 3.0 A

The relationship of USB Type-C Current and the equivalent USB PD Power (PDP) value is shown in Table 4-18.

Table 4-18 USB Type-C Current Advertisement and PDP Equivalent

USB Type-C Current		PDP Equivalent
Default	500 mA (USB 2.0)	2.5 W
	900 mA (USB 3.2 single-lane)	4.5 W
	1,500 mA (USB 3.2 dual-lane)	7.5 W
1.5 A		7.5 W
3.0 A		15 W