USB Type-C ENGINEERING CHANGE NOTICE

Title: Active Cables Phase 1
Applied to: USB Type-C Specification Release 1.3

Brief description of the functional changes proposed:
This ECN adds technical definition to the USB Type-C spec that covers active cable requirements for short range cables, e.g. cables that are implemented as electrical cables (no optical) up to the practical lengths that still allow for USB PD and USB 2.0 to fully function as intended without cable-specific assistance.

Benefits as a result of the proposed changes:
Allows longer cables.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
None

An analysis of the hardware implications:
Only to the new active cables. Required host to support PD3 for best benefit.

An analysis of the software implications:
None

An analysis of the compliance testing implications:

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Actual Change Requested

Changes captured using track changes to the following sections or added new sections.

1.3 Related Documents

USB 2.0 *Universal Serial Bus Revision 2.0 Specification*
This includes the entire document release package.
http://www.usb.org/developers/docs

USB 3.2 *Universal Serial Bus Revision 3.2 Specification*
This includes the entire document release package.
http://www.usb.org/developers/docs

USB PD *USB Power Delivery Specification, Revision 2.0, Version 1.3, January 12, 2017*
USB Power Delivery Specification, Revision 3.0, Version 1.1, January 12, 2017 (including errata and ECNs through June 12, 2017)
http://www.usb.org/developers/docs

USB BB *USB Billboard Device Class Specification, Revision 1.21, September 8, 2016*
http://www.usb.org/developers/docs

USB BC *Battery Charging Specification, Revision 1.2 (including errata and ECNs through March 15, 2012), March 15, 2012*
http://www.usb.org/developers/docs

1.5 Terms and Abbreviations

Term	Description
Accessory Mode	A reconfiguration of the connector based on the presence of Rd/Rd or Ra/Ra on CC1/CC2, respectively.
Active cable	~~A cable with a USB Type-C Plug on each end at least one of which is a Cable Plug supporting SOP'. It is an Electronically Marked Cable see Section 4.9.~~ Active cables are USB Full-Featured Type-C Cables that incorporate repeaters in the USB3.2 data path. All active cables, regardless of length, ~~shall be~~are expected to comply~~iant~~ with this specification, the USB 3.2 Appendix E, and the USB3.2 active cable CTS. Active cables may incorporate repeaters in both ends of the cable, one end, or anywhere in the cable.~~An Electronically Marked Cable with additional electronics to condition the data path signals.~~
Alternate Mode	Operation defined by a vendor or standards organization that is associated with a SVID assigned by the USB-IF. Entry and exit into and from an Alternate Mode is controlled by the *USB PD* Structured VDM Enter Mode and Exit Mode commands.

Term	Description
Alternate Mode Adapter (AMA)	A USB PD Device which supports Alternate Modes and acts as a UFP.
Audio Adapter Accessory Mode	The Accessory Mode defined by the presence of Ra/Ra on CC1/CC2, respectively. See Appendix A.
BFSK	Binary Frequency Shift Keying used for USB PD communication over VBUS.
BMC	Biphase Mark Coding used for USB PD communication over the CC wire.
Cable Port Partner	The USB Type-C DRP, DFP, UFP connected to the cable plug.
Captive cable	A cable that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end.
CC	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable.
Debug Accessory Mode (DAM)	The Accessory Mode defined by the presence of Rd/Rd or Rp/Rp on CC1/CC2, respectively. See Appendix B.
Debug and Test System (DTS)	The combined hardware and software system that provides a system developer debug visibility and control when connected to a Target System in Debug Accessory Mode.
Default VBUS	VBUS voltage as defined by the USB 2.0 and ~~USB 3.1~~ USB 3.2 specifications. Note: where used, 5 V connotes the same meaning.
DFP	Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically the ports on a host or the ports on a hub to which devices are connected. In its initial state, the DFP sources VBUS and VCONN, and supports data. A charge-only DFP port only sources VBUS.
Direct connect	The host's DFP is connected directly with no USB hub in between, either via a cable or without (e.g., thumb drive), to the device's UFP.
DRD (Dual-Role-Data)	The acronym used in this specification to refer to a USB port that can operate as either a DFP (Host) or UFP (Device). The role that the port initially takes is determined by the port's power role at attach. A Source port takes on the data role of a DFP and a Sink port takes on the data role of a UFP. The port's data role may be changed dynamically using USB PD Data Role Swap.
DRP (Dual-Role-Power)	The acronym used in this specification to refer to a USB port that can operate as either a Source or a Sink. The role that the port offers may be fixed to either a Source or Sink or may alternate between the two port states. Initially when operating as a Source, the port will also take on the data role of a DFP and when operating as a Sink, the port will also take on the data role of a UFP. The port's power role may be changed dynamically using USB PD Power Role Swap.
DR_Swap	USB PD Data Role Swap.

Term	Description
Electronically Marked Cable	A USB Type-C cable that uses *USB PD* to provide the cable's characteristics.
eMarker	The element in an Electronically Marked Cable that returns information about the cable in response to a *USB PD* Discover Identity command.
Initiator	The port initiating a Vendor Defined Message. It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Initiator will be a host.
Internal Temperature	Temperature measured inside an active cable's plug. It is not the skin temperature. There is a relationship between the plug's Internal Temperature and the skin temperature, but that relationship is design dependent.
Local Plug	The cable plug being referred to.
~~Medium Active Cable (MAC)~~	~~A cable with a USB Type-C Plug on each end at least one of which is a Cable Plug supporting SOP'. Cable length 5 to 15 m.~~
~~Master Plug~~	~~OIAC plug defined as the master for USB PD communication at time of manufacture.~~
~~Optically Isolated Active Cable (OIAC)~~	~~A cable with a USB Type-C Plug on each end with one Cable Plug supporting SOP' and the other supporting SOP". Electrically isolated between the two plugs.~~
Passive cable	A cable that does not incorporate any electronics to condition the data path signals. A passive cable may or may not be electronically marked.
Port Partner	Refers to the port (device or host) a port is attached to.
Power Bank	A device with a battery whose primary function is to charge or otherwise extend the runtime of other USB Type-C devices.
Powered cable	A cable with electronics in the plug that requires VCONN indicated by the presence of Ra between the VCONN pin and ground.
PR_Swap	*USB PD* Power Role Swap.
Re-driver	Re-driver refers to an analog component that operates on the signal without re-timing it. This may include equalization, amplification, and transmitter. The re-driver does not include a CDR. Re-drivers are beyond the scope of this document.
~~Remote Plug~~	~~A remote cable plug in the context of OIAC plugs is the plug at the other end of the Optically Isolated Active Cable~~
Repeater	*Repeater* refers to any active component that acts on a signal in order to increase the physical lengths and/or interconnect loss over which the signal can be transmitted successfully. The category of repeaters includes both re-timers and re-drivers.
Responder	The port responding to the Initiator of a Vendor Defined Message (VDM). It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Responder will be a device.

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Term	Description
Re-timer	*Re-timer* refers to a component that contains a clock-data recovery (CDR) circuit that "retimes" the signal. The re-timer latches the signal into a synchronous memory element before re-transmitting it. It is used to extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the re-timer. Re-timers are defined in USB 3.2 Appendix E.
SBU	Sideband Use.
~~Short Active Cable (SAC)~~	~~A cable with a USB Type-C Plug on each end at least one of which is a Cable Plug supporting SOP'. Cable length up to 5m.~~
SID	A Standard ID (SID) is a unique 16-bit value assigned by the USB-IF to identify an industry standard.
Sink	Port asserting Rd on CC and when attached is consuming power from VBUS; most commonly a Device.
Skin Temperature	The temperature of a plug's over-mold.
~~Slave Plug~~	~~OIAC plug defined as the Slave for USB PD communication at time of manufacture.~~
Source	Port asserting Rp on CC and when attached is providing power over VBUS; most commonly a Host or Hub DFP.
SVID	General reference to either a SID or a VID. Used by *USB PD* Structured VDMs when requesting SIDs and VIDs from a device.
Target System (TS)	The system being debugged in Debug Accessory Mode.
~~Transaction Translator (TT)~~	~~An optional functional component of an OIAC cable plug. The *Transaction Translator* responds to Super Speed transactions and translates them to high/full/low-speed transactions to support high/full/low-speed devices attached to an OIAC cable.~~
Type-A	A general reference to all versions of USB "A" plugs and receptacles.
Type-B	A general reference to all versions of USB "B" plugs and receptacles.
Type-C Plug	A USB plug conforming to the mechanical and electrical requirements in this specification.
Type-C Port	The USB port associated to a USB Type-C receptacle. This includes the USB signaling, CC logic, multiplexers and other associated logic.
Type-C Receptacle	A USB receptacle conforming to the mechanical and electrical requirements of this specification.
UFP	Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks VBUS and supports data.
USB 2.0 Type-C Cable	A USB Type-C to Type-C cable that only supports *USB 2.0* data operation. This cable does not include *USB 3.2*~~USB 3.1~~ or SBU wires.
USB 2.0 Type-C Plug	A USB Type-C plug specifically designed to implement the USB 2.0 Type-C cable.

Term	Description
USB Full-Featured Type-C Cable	A USB Type-C to Type-C cable that supports *USB 2.0* and *USB 3.2*~~USB 3.1~~ data operation. This cable includes SBU wires and is~~.~~ an Electronically Marked Cable.
USB Full-Featured Type-C Plug	A USB Type-C plug specifically designed to implement the USB Full-Featured Type-C cable.
USB Safe State	The USB Safe State as defined by the *USB PD* specification.
VPD charge-through	A mechanism for a VCONN-Powered USB Device to pass power and CC communication from one port to the other without any reregulation. This will be defined in a future specification.
VCONN-Powered Accessory (VPA)	An accessory that is powered from VCONN to operate in an Alternate Mode. VPAs cannot implement the charge-through mechanism described for VPDs, and instead must intermediate by negotiating USB Power Delivery with both the connected host and source in order to enable similar functionality.
VCONN-Powered USB Device (VPD)	A USB direct-connect or captive-cable device that can be powered solely from either VCONN or VBUS. VPDs may optionally support the VPD charge-through capability.
VCONN_Swap	*USB PD* VCONN Swap.
VDM	Vendor Defined Message as defined by the *USB PD* specification.
VID	A Vendor ID (VID) is a unique 16-bit value assigned by the USB-IF to identify a vendor.
vSafe0V	VBUS “0 volts” as defined by the *USB PD* specification.
vSafe5V	VBUS “5 volts” as defined by the *USB PD* specification.

Table 5-1 Cable VCONN Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0	5.5V	Voltage range at which this Table applies
Inrush Capacitance		10 µF	A cable shall not present more than the equivalent inrush capacitance to the VCONN source. The active cable is responsible for discharging its capacitance.
Power for Electronically Marked Passive Cables		20mW	See Section 4.9. Measured with no USB PD traffic at least 500ms after VCONN applied Note: 75mW max allowed for the first 500ms after VCONN applied.
~~**Power for Active Cables**~~		~~1.0 W~~	~~See Section 5.2.~~
~~**Power for Active Cables in USB Suspend**~~		~~70mW~~	~~Maximum power for active cables in USB suspend.~~ ~~Measured with no USB PD traffic at least 500ms after VCONN applied~~
USB 3.2 Power for Active Cables in U-states		Table 5-10	U0, U1, U2, U3, Rx.Detect, and eSS.Disabled.
tVCONNDischarge		230ms	Time from cable disconnect to vVCONNDischarge met.
vVCONNDischarge		800mV	VCONN voltage after tVCONNDischarge
vRaReconnect	800mV		Voltage at which the cable shall reapply Ra on the falling edge of VCONN.

Text Replaces Section 5.2:

5.2 Active Cables

Active cables are designed to 'just work' like passive cables with no discernable difference from the user's perspective. Active cables shall minimally support USB 3.2 Gen 2x1. As multi-lane USB 3.2 and multi-lane USB 3.2 repeaters become common, all active cables will be required to support two lanes. Active cables shall support USB PD eMarkers and may support Alternate Modes and advertise them as defined in Section 5.2.6.

Active cables are specified to ensure that they may be freely and transparently introduced into the USB ecosystem.

Table 5-4 Summary of Active Cable Features

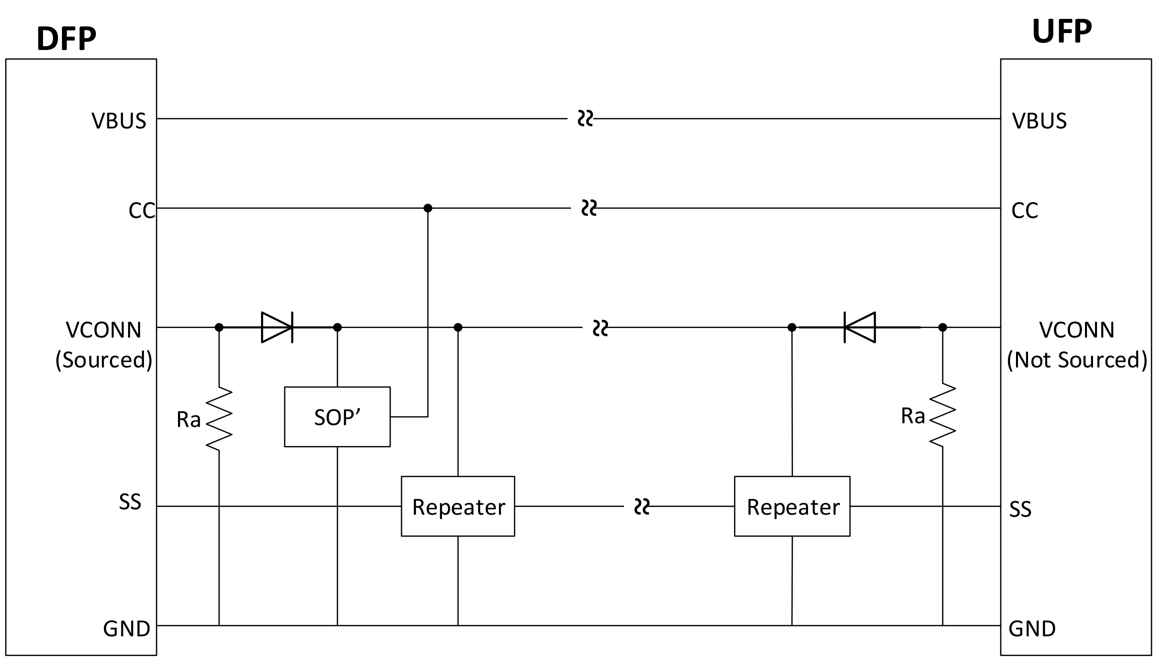
Length	USB PD	VBUS	VCONN Wiring	CC	USB 2.0	USB 3.2	SBU
< 5 m	SOP' Required (SOP" Optional)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	(Repeater) Gen 2x1 Gen 1x2 Gen 2x2	Passive

All active cables, regardless of length, shall be compliant with this specification, the USB 3.2 including Appendix E, and the USB3.2 active cable CTS.

5.2.1 USB PD Support

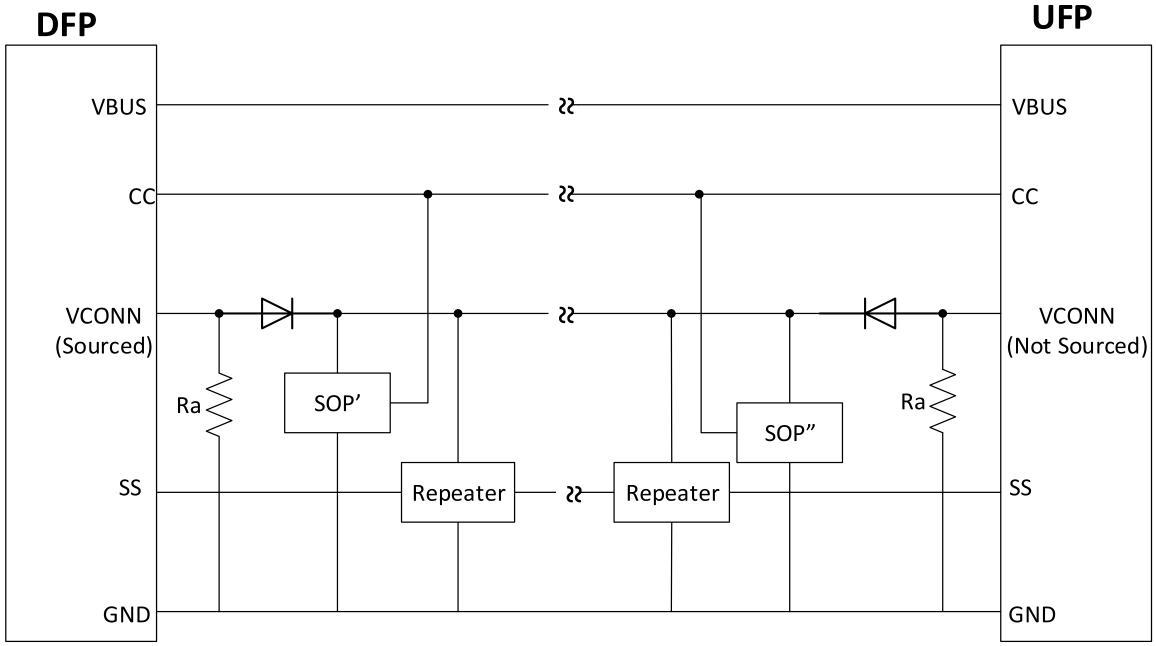
Active cables shall be electronically marked per Figure 5-7.

Figure 5-7 Electronically Marked Active Cable with SOP' Only



Active cables may optionally be electronically marked on both ends of the cable as illustrated in Figure 5-8.

Figure 5-8 Electronically Marked Active Cable with SOP' and SOP"



5.2.2 Active Cable USB PD Requirements

Active cables shall support the following USB PD Structured VDMs.

5.2.2.1 SOP' and SOP" Requirements

Active cables shall respond to ***Discover_Identity*** and ***Get_Status*** on SOP'. When the SOP'' Controller Present bit is set in the Active Cable VDO, they shall respond ***Get_Status*** on SOP'' as well.

5.2.2.2 Discovering Cable Characteristics

The USB PD ***Discover_Identity*** Command is used to discover the characteristics of the active cable. This command shall only be sent to SOP'. All active cables shall respond to the ***Discover_Identity*** Command with Active Cable VDOs that returns information about the cable.

5.2.2.3 Cable Status

The USB PD ***Get_Status*** Command is used to discover the current state of the active cable. Cable status shall be reported on SOP' and shall also be reported on SOP" when the SOP'' Controller Presence bit is set in the Active Cable VDO. The Status returns:

- Internal temp of the plug
- Thermal shutdown indicator

5.2.2.4 Active Cable's Behavior in Response to Power Delivery Events

5.2.2.4.1 Data Role Swap

Active cables are transparent to the USB PD Data Role swap.

5.2.2.4.2 Power Role Swap

Active cables shall maintain USB 3.2 signaling during a USB PD Power Role swap. During a power role swap, both the original Source and the new Source supply power to the USB interface. The original Source continues to supply VCONN power during and after the Power Role Swap, so the Active Cable never loses power.

5.2.2.4.3 VCONN Swap

Active cables shall maintain USB 3.2 signaling during a USB PD VCONN swap. During a VCONN Swap the original VCONN Source continues to supply VCONN for some time after the new VCONN Source begins to supply VCONN. This ensures that VCONN is never dropped.

5.2.2.4.4 Fast Role Swap

Active cables will drop USB 3.2 signaling as a side-effect of a Fast Role Swap if VCONN is not maintained during the Fast Role Swap.

5.2.3 Active Cable Power Requirements

5.2.3.1 VBUS Requirements

All active cables shall meet the limits of the IR Drop on VBUS and ground defined in Section 4.4.1.

Active cables shall provide VBUS and support at least 3 A and optionally 5 A current.

5.2.3.2 VCONN Requirements

Active Cables shall:

- Be capable of being powered from VCONN from only one port.
- Meet the VCONN sink requirement defined in Table 4-5 and Table 5-10.
- Connect VCONN as shown in Figure 2-1 or Figure 2-2.

5.2.4 Mechanical

All active cables shall meet the mechanical requirements defined in the Section 3.8.

5.2.4.1 Thermal

5.2.4.1.1 Thermal Shutdown

All active cables shall implement a temperature sensor and place the USB 3.2 signals in the eSS.Disabled state when the plug skin temperature reaches the maximum defined in Table 4-1. Active cables shall indicate they are in thermal shutdown if queried via the USB PD ***Get_Status*** command.

5.2.4.1.2 Maximum Skin Temperature

Active cable plug's skin temperature shall not exceed a maximum operating temperature of 30 °C above the ambient temperature for a plastic/rubber housing and 15 °C for a metal housing in any operating mode.

5.2.4.1.3 Thermal Reporting

Active cables shall implement reporting their maximum internal operating temperature in the USB PD ***Discover_ID*** Command. Active cables shall implement reporting their current internal operating temperature in the USB PD ***Get_Status*** Command on SOP' and SOP" when supported. Active cables shall update their reported Internal Temperature at least every 500 ms.

The plug's Internal Temperature is reported in °C and shall be monotonic. It is not the plug's skin temperature, but cable manufacturers shall correlate the maximum internal operating temperature with the maximum plug skin temperature to ensure shutdown when the maximum plug skin temperature is reached.

Sources and/or Sinks may take action to reduce VBUS current to reduce the cable plug internal operating temperature to below the reported maximum operating temperature. It is recommended Sources and/or Sinks poll the plug's Internal Temperature every 2 seconds.

Table 5-6 Cable Temperature Requirements

Temperature Requirements	
Maximum Internal to Skin Temperature Offset	Design specific
Maximum Internal Operating Temperature	Design specific
Maximum Skin Temperature Plastic/Rubber[1]	80 °C
Maximum Skin Temperature Metal[1]	55 °C
Note 1: IEC 69950-1 reduced by 5 °C	

5.2.4.2 Plug Spacing

Active cables will support the USB Type-C vertical and horizontal spacing defined Section 3.x when functioning in USB 3.2 x1 operation. However, this spacing may impose thermal constraints. Appendix D provides system design guidance to minimize the thermal impact due to connector spacing. It is recommended that products designed for USB 3.2 x2 operation with multiple adjacent USB Type-C connectors follow the design guidance in Appendix D to minimize the likelihood the active cable will go into thermal shutdown.

5.2.5 Electrical Requirements

5.2.5.1 Shielding Effectiveness Requirement

All active cables shall meet the shielding effectiveness requirement defined in Section 3.7.6 and Figure 3-56.

5.2.5.2 Low Speed Signal Requirements

5.2.5.2.1 CC Channel Requirements

Active cables shall meet the Low-Speed Signal Requirements in Section 3.7.2.1.

5.2.5.2.2 SBU Requirements

Active cables SBU wires shall meet the requirements defined in Table 5-7 and shall meet the crosstalk requirements both near-end and far-end between the low speed signals as defined in 3.7.2.3.

Active cable SBU end-to-end connections shall meet the requirements defined in Table 5-7 when Vconn is present. SBUs have no guaranteed performance when Vconn is not provided to the cable. The Host or Device shall not provide any signal beyond what is defined in Table 5-7 when VCONN has not been provided.

Table 5-7 Active Cable SBU Characteristics

Name	Description	Min	Max	Units
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wire		26	ns
rCable_SBU	DC resistance of SBU wires in the cable in USB		40	Ω
vCable_SBU	Cable voltage swing on SBU wires	−0.3	4.0	V
Insertion Loss[1]	Cable insertion Loss		5 @ 0.5MHz 7 @ 1MHz 12 @ 10MHz 13 @ 25MHz 15 @ 50MHz 16 @ 100MHz	dB
iCableSBU	Maximum end-to-end current	-25	+25	mA

Notes:

1. Measurement referenced to 50 Ohms.

5.2.5.3 USB 2.0

Active cables shall meet the USB 2.0 requirements defined in Section 3.7.2.3 and 3.7.2.4.

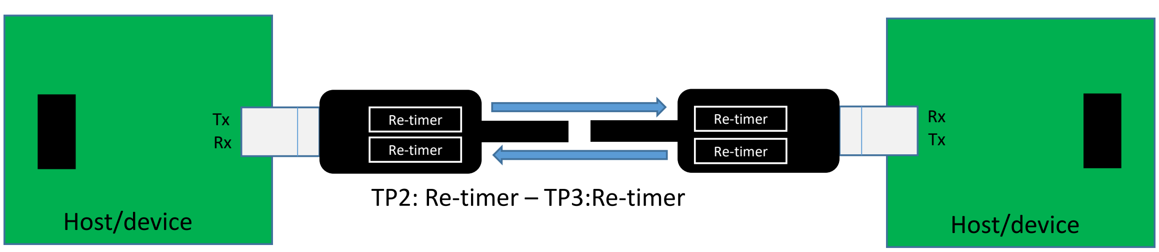
5.2.5.4 USB 3.2

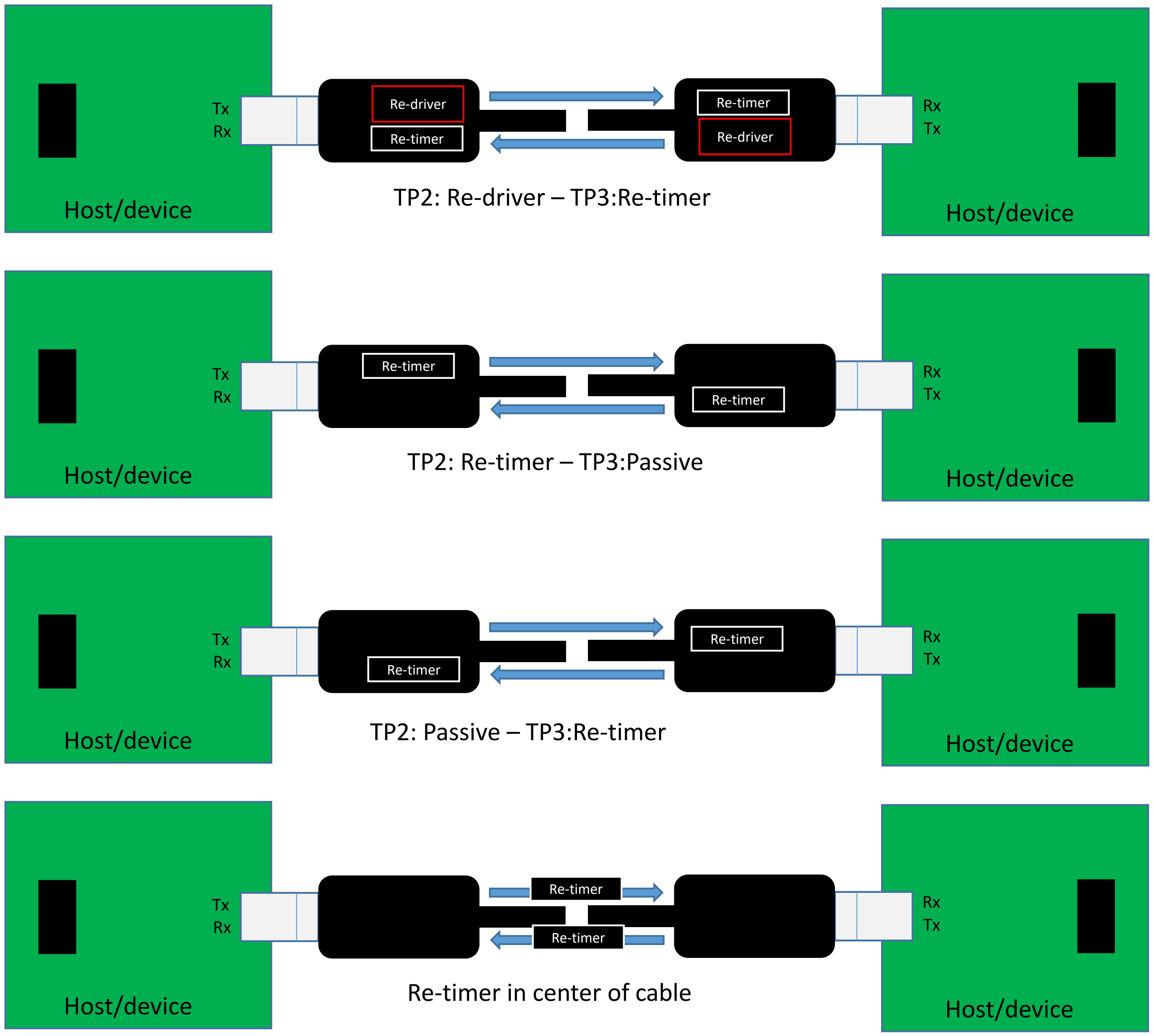
Active cables shall meet the requirements in this section regardless of length. Active cables shall incorporate AC-coupling from the plug to repeater on both the SSTX and SSRX USB 3.2 signals. Active cables shall provide a discharge path for discharging the AC-coupling capacitors in the cable on unplug per USB3.2.

5.2.5.4.1 USB 3.2 Active Cable Architectures

Active cables may have the following combinations of re-timers and re-drivers. Active cables without at least one re-timer are out of scope. Active cables without re-timers connected to TP3 are out of scope.

Figure 5-8 Active Cable Topologies





5.2.5.4.2 USB 3.2 Power-on and Rx.Detect

Active cables shall present a high impedance to ground of ZRX-HIGH-IMP-DC-POS when not powered. Active cables shall present a high impedance to ground of ZRX-HIGH-IMP-DC-POS at initial power-on. The active cable shall perform far-end receiver termination detection on both cable ends upon receiving VCONN. Upon detecting a far-end low-impedance receiver termination (RRX-DC), the active cable shall enable its low-impedance receiver termination (RRX-DC) to mirror the presence of the Host/Device. The active cable shall perform far-end receiver termination detection per USB3.2.

An active cable shall complete power-on and far-end receiver termination detection through the cable within tFWD_RX.DETECT.

Table 5-8 Active Cable Power-on Requirements

Parameter	Minimum	Maximum	Units
ZRX-HIGH-IMP-DC-POS	per USB 3.2	per USB 3.2	
RRX-DC	per USB 3.2	per USB 3.2	
tFWD-RX.DETECT		42	ms

5.2.5.4.3 USB 3.2 U0 Delay

Repeaters in active cables shall meet the U0 delay requirements defined in USB 3.2 Appendix E.

5.2.5.4.4 USB 3.2 U-State Power Requirements

Active cables shall meet the VCONN power requirements in Table 5-10. These requirements are for the entire cable not just a cable plug.

Table 5-10 USB 3.2 U-State Requirements

State	Requirement	Maximum Power Consumption VCONN	Target Power Consumption VCONN	Power Consumption Notes
U0	Required	1.0W 1-lane 1.5W 2-lane		Applies to POLLING.LFPS, TRAINING, and RECOVERY states.
U1	Logically required	≤U0 power		Forwarding U1 LFPS is required
U2	Logically required	≤U1 power		Forwarding U2 LFPS is required
U3	Required	5mW	2mW	eMarker in sleep.
Rx.Detect	Required	5mW	2mW	Rx.Detect period may be lengthened when no USB3.2 terminations have been detected. eMarker in sleep.
eSS.Disabled	Required	5mW	1mW	USB3.2 is disabled. eMarker in sleep.

Note: Ra must be completely removed or very high impedance to meet the power requirements in U3, Rx.Detect, and eSS.Disabled.

5.2.5.4.5 USB 3.2 U-State Exit Latency

Active cables shall meet the U-state exit latency defined in USB 3.2 Appendix E.

5.2.5.4.6 USB 3.2 Signal Swing

An active cable transmitter only has to drive 8.5 dB insertion loss at 5 GHz to the Host/Device controller receiver for USB 3.2 Gen 2. A Host/Device controller transmitter must drive a total loss of 23 dB at 5 GHz to the far side for USB 3.2 Gen 2. The difference in loss budget allows the active cable transmitter swing to be reduced. An active cable receiver can assume a larger receiver swing than in the Host/Device for the same reason.

Figure 5-8 defines the SuperSpeed electrical test points and is copied from the USB3.2 specification. Figure 5-9 indicates the test points and test equipment connections.

Figure 5-8 SuperSpeed Electrical Test Points

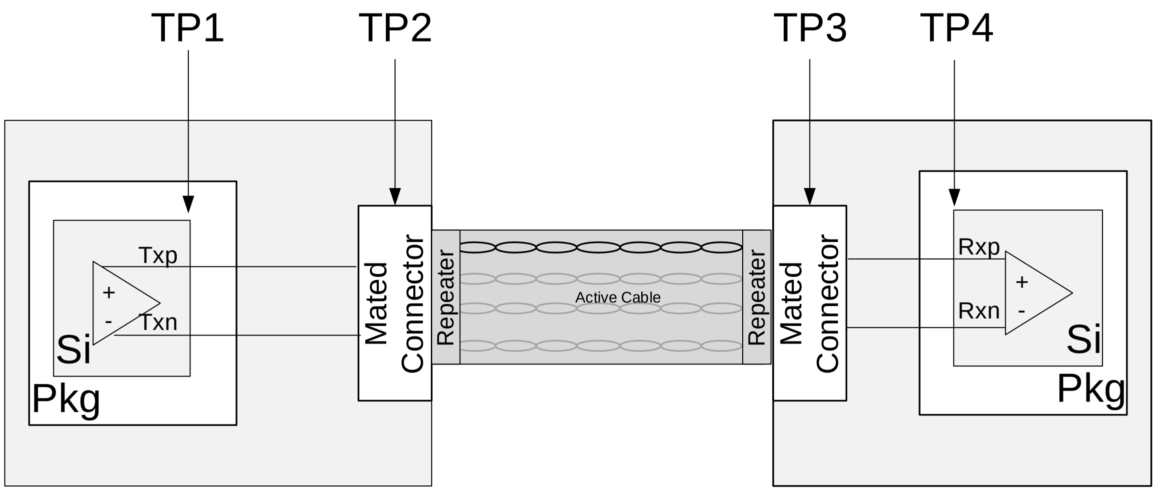
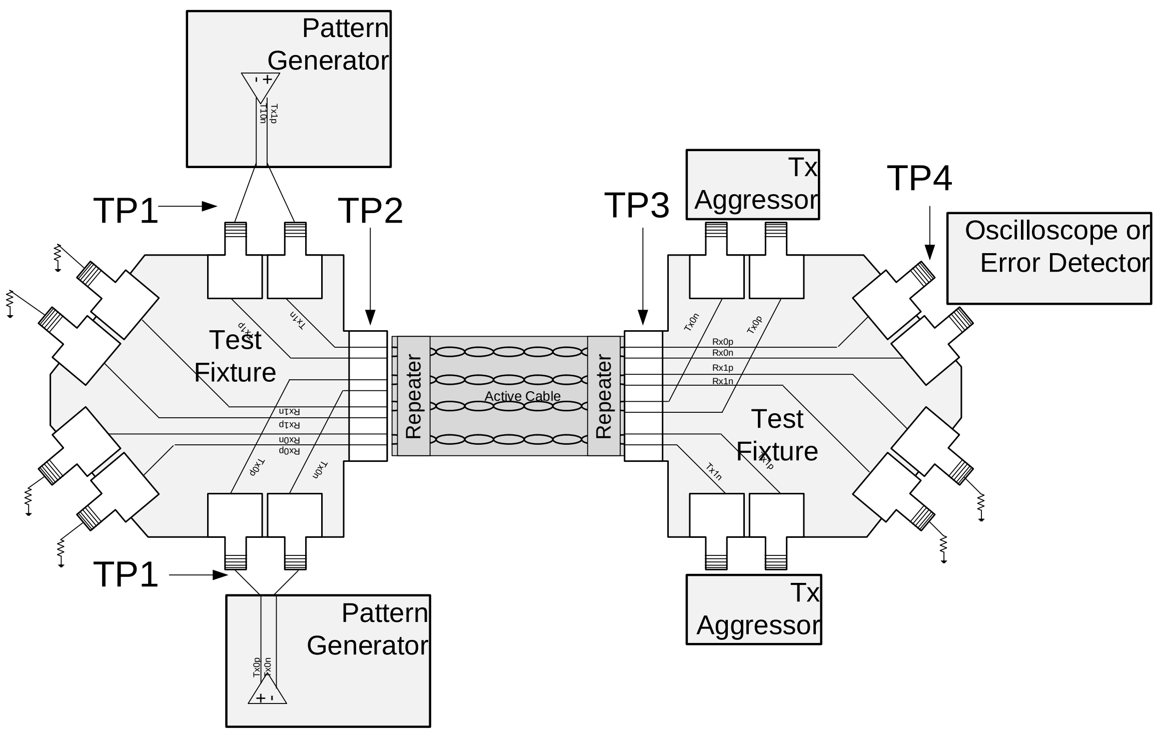


Figure 5-9 SuperSpeed Compliance Test Setup



5.2.5.4.6.1 TP1 – Active Cable Input Stressed Source

The active cable input stressed source is generated at TP1 per Table 5-11 for amplitude and per Table 5-12 for jitter. SSC shall be present in the stressed signal at TP1. Table 5-11 is a subset of the USB3.2 Table 6-18. Table 5-12 is a subset of USB3.2 Table 6-28. If any discrepancy exists between this specification and the USB3.2 specification, the USB3.2 specification shall take precedence.

The maximum swing with the maximum de-emphasis and pre-shoot shall be tested with the minimum loss compliance test board. The minimum swing with the minimum de-emphasis and pre-shoot shall be tested with the maximum loss compliance test board. The input jitter composition is the same for both the minimum and maximum swing stressed sources.

The active cable shall function over the range of parameter in USB3.2 Table 6-17 and Table 5-11.

Table 5-11 Active Cable USB 3.2 Stressed Source Swing, TP1

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX-DE-RATIO}$	Tx de-emphasis	USB3.2 Table 6-17	−3.1+/-1.0	dB	Nominal is 3.5 dB for Gen 1 operation. Gen 2 transmitter equalization requirements are described in USB3.2 Section 6.7.5.2.
$V_{PRESHOOT}$	Tx Preshoot	USB3.2 Table 6-17	2.2+/-1.0	dB	Gen 2 transmitter equalization requirements are described in USB3.2 Section 6.7.5.2.

Table 5-12 Active Cable USB 3.2 Stressed Source Jitter, TP1

Symbol	Parameter	Gen 1 (5GT/s)	Gen 2 (10GT/s)	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.0100	UI rms	1
J_{Rj_p-p}	Random Jitter peak- peak at 10^{-12}	0.17	0.14	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3

Notes:

1. All parameters measured at TP1. The test point is shown in Figure 5-8 & 5-9.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test.
5. The JTOL specs for Gen 2 comprehend jitter peaking with re-timers in the system and has a 25dB/decade slope.

5.2.5.4.6.2 TP2 – Active Cable Input (Informative)

The values in Table 5-13 indicate the informative input signal swings at TP2 for an active cable. Table 5-13 is included to provide guidance beyond the normative requirements of Table 5-11 and Table 5-12. An active cable can be fully compliant with the normative requirements of this specification and not meet all the values in Table 5-13. Similarly, an active cable that meets all the values in Table 5-13, is not guaranteed to be in fully compliance with the normative part of this specification.

Table 5-13 Active Cable USB 3.2 Input Swing at TP2 (Informative)

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p Tx voltage swing	250 (min) 1000 (max)	250 (min) 850 (max)	mV	Nominal is 550mV p-p
$V_{TX\text{-}DE\text{-}RATIO}$	Tx de-emphasis	0 (min) 4.0 (max)	2.1 (min) 4.1 (max)	dB	There is no de-emphasis requirement for Gen1.
$V_{PRESHOOT}$	Tx Preshoot	NA	1.2 (min) 3.2 (max)	dB	Applicable to USB3.2 gen2 operation only

5.2.5.4.6.3 TP3 – Active Cable Output (Informative)

The values in Table 5-14 indicate the informative output signal swings at TP3 for an active cable. Table 5-14 is included to provide guidance beyond the normative requirements of Table 5-14 and 5-15. An active cable can be fully compliant with the normative requirements of this specification and not meet all the values in Table 5-14. Similarly, an active cable that meets all the values in Table 5-14, is not guaranteed to be in full compliance with the normative part of this specification.

Table 5-14 Active Cable USB 3.2 Output Swing at TP3 (Informative)

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
$V_{RX\text{-}DIFF\text{-}PP\text{-}POST\text{-}EQ}$	Differential Rx peak-to-peak voltage	300 (min) 850 (max)	300 (min) 850 (max)	mV	Measured after the Rx EQ function (Section **Error! Reference source not found.**). Nominal is 0.5 V p-p
$V_{TX\text{-}DE\text{-}RATIO\text{-}GEN1}$	Tx de-emphasis	0 (min) 4.0 (max)	NA	dB	No preshoot allowed
$V_{TX\text{-}DE\text{-}RATIO}$ + $V_{PRESHOOT\text{-}GEN2}$	Tx de-emphasis + Tx Preshoot	NA	0 (min) 3.0 (max)	dB	Sum of the de-emphasis and preshoot. There is no de-emphasis and pre-shoot requirement.

5.2.5.4.6.4 TP4 – Active Cable Output

The active cable transmitter output is defined at TP4 for both high and low loss channels. The requirements for TP4 are defined in the USB3.2 specification Table 6-20. The input signal for the test shall be applied at TP1 per Section 5.2.5.4.6.1.

The low loss test board shall be used to test the maximum output swing. The maximum loss test board shall be used to test the minimum output swing. Jitter must be met with both test boards.

The active cable bit-error-rate shall be tested at TP4 and meet or exceed a BER of 10^{-12}. The error detector used shall have the ability to remove SKP ordered sets.

5.2.5.5 Return Loss

To be defined in a future update.

5.2.6 Active Cables that Support Alternate Modes

Active cables may support Alternate Modes. Active cables that support Alternate Modes shall be discoverable via USB PD. They shall use the standard USB PD mechanisms to discover, enter and exit Alternate Modes.

5.2.6.1 Discover SVIDs

Active cables that support an Alternate Mode shall report support for SVIDs on SOP' only.

5.2.6.2 Discover Modes

Active cables that support an Alternate Mode shall report support for Modes on SOP' only.

5.2.6.3 Enter/Exit Mode

Enter and ***Exit*** mode shall be communicated on SOP' and on SOP'' when the SOP'' Controller Present bit is set in the Active Cable. It is recommended that ***Enter*** mode be sent initially to SOP' and then SOP" if supported and then SOP. It is recommended ***Exit*** mode be sent initially to SOP and then to SOP" if supported and then SOP'.

5.2.6.4 Power in Alternate Modes

The power dissipation in an active cable's Alternate Mode shall maintain the plug's Maximum Skin Temperature below the requirement defined in Table 5-6.

Alternate Modes should reduce power in active cables in sleep states for best user experience.

New Appendix:

D Thermal Design Considerations

D.1. Introduction

USB Type C active cables use active circuitry to realize a longer link than passive cables and to maintain the electrical performance at high speed data transmission (USB3.2 Gen 2 single-lane or USB3.2 Gen 1 or Gen 2 two-lane). The additional power dissipation due to active components in the plug over-mold, creates a thermal challenge to passively dissipate power from its active components off limited outer surface area of cable over-mold. Furthermore, the VBUS current, up to 5A for power delivery, generates joule heat from the conductors along VBUS and GND lines, including copper wires, solder joints, contact pins insides connectors and copper traces on paddle board.

This appendix provides some case studies to show the thermal impacts of certain factors affecting the maximum over-mold surface temperature T_S such as IC power inside over-mold (P_0), thermal boundary, VBUS current level, and port to port spacing. The case study provided is for a specific mechanical design of the cable. When a different mechanical design (geometry or material, etc.) are used, these impacts need further investigation. The methodology of the study is thermal modelling. The modelling results has been validated for some cases (1.5W P_0 and 5A VBUS) with lab test results within +/- 3 °C, but not for all cases. Note that this appendix is not a full factorial or complete Design of Experiment (DOE) study and whether there is interaction among any of these factors are not covered here.

To meet thermal requirements specified in Section 5.2.4.1, as well as the junction temperature T_J requirement of any active components, an active cable should be carefully designed to facilitate the desired heat flow paths. A desirable thermal resistance between powered IC to over-mold surface is achieved when neither T_S nor T_J exceeds their specifications. This appendix focuses solely on T_S as output of the study, as the T_J requirement varies depending on the IC requirements.

It is recommended that system integrator such as host or device designer should take into consideration the heat transferred to or from an active cable in the system level thermal analysis.

Nomenclature used in this white paper:

T_A = ambient temperature (°C)

T_J = junction temperature (°C)

T_S = plug over-mold outer surface maximum temperature (°C)

T_{MB} = motherboard/thermal boundary temperature (°C)

P_0 = active component power (W) inside the over-mold that directly plugged in the host or device at each end of cable

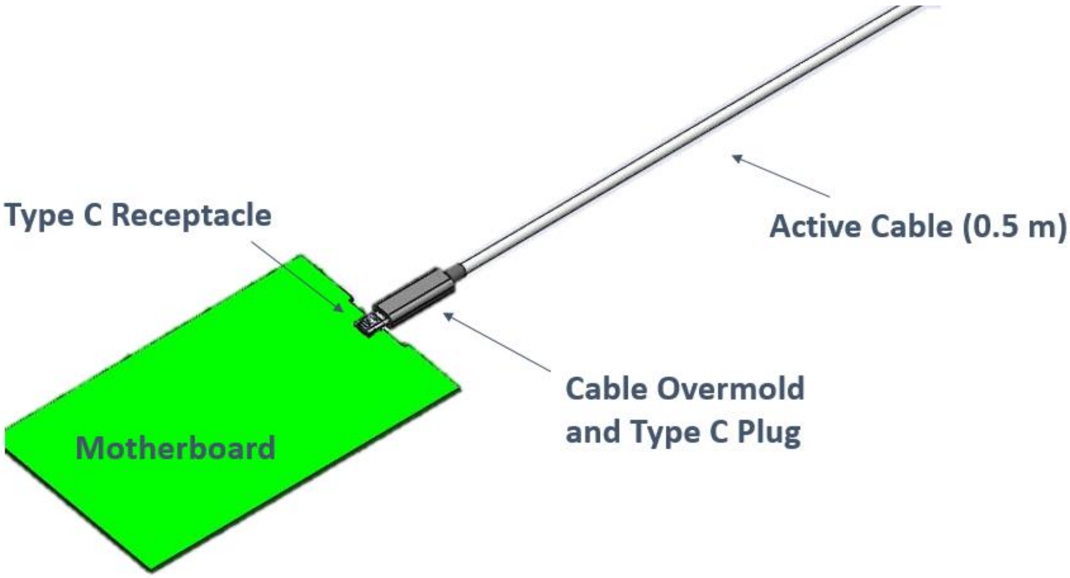
D.2. Model

D.2.1. Assumptions

A system model was built which includes a half active cable with one over-mold on the end, a mated pair of connectors (plug and receptacle) and a motherboard as its host or device side thermal boundary. The model assumes the cable is symmetric with VCONN power to be equally divided and each end of cable consumes half of VCONN power for the active components.

It is a Computational Fluid Dynamics (CFD) model with heat transfer of conduction, natural convection and radiation. Emissivity of the plug over-mold and cable jacket is assumed to be 0.92 and the connector metal surfaces is assumed to be 0.05.

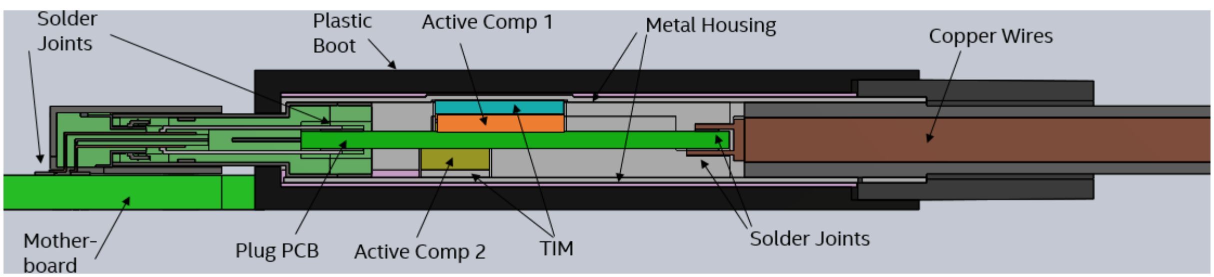
Figure D-1. Active Cable Model (Single Port, Top Mount Receptacle)



D.2.2. Model Architecture

The specific system and cable architecture used in the model is shown below.

Figure D-2. Model Architecture



The simplified cable model uses a pure copper cable, representing a typical short active cable, with total cross section of the copper conductors being about 3.8 mm^2.

The cable model incorporates a plastic boot for the over-mold which allows a higher surface temperature threshold than some other materials such as metal or glass. The over-mold length in the study was 35 mm.

In this specific cable design, two active components are surface mounted on plug PCB (or paddle board). Thermal Interface Material (TIM) are placed between “hot components” and “heat spreading material” such as metal housings to reduce thermal resistance between component junctions to ambient. Metal shells help to reduce T_S by spreading heat across the over-mold surface and avoid hot spots.

The plug PCB and motherboard are assumed to be FR4 based material. The motherboard is a bulk model assumed to be at a constant temperature without a point heat source on it. The receptacle is top mounted on the motherboard in single port and horizontal stacked cases, Figure D-; and is vertically mounted in vertical stack up cases, Figure D- and Figure D-.

D.2.3. Heat Sources

Main heat sources include:

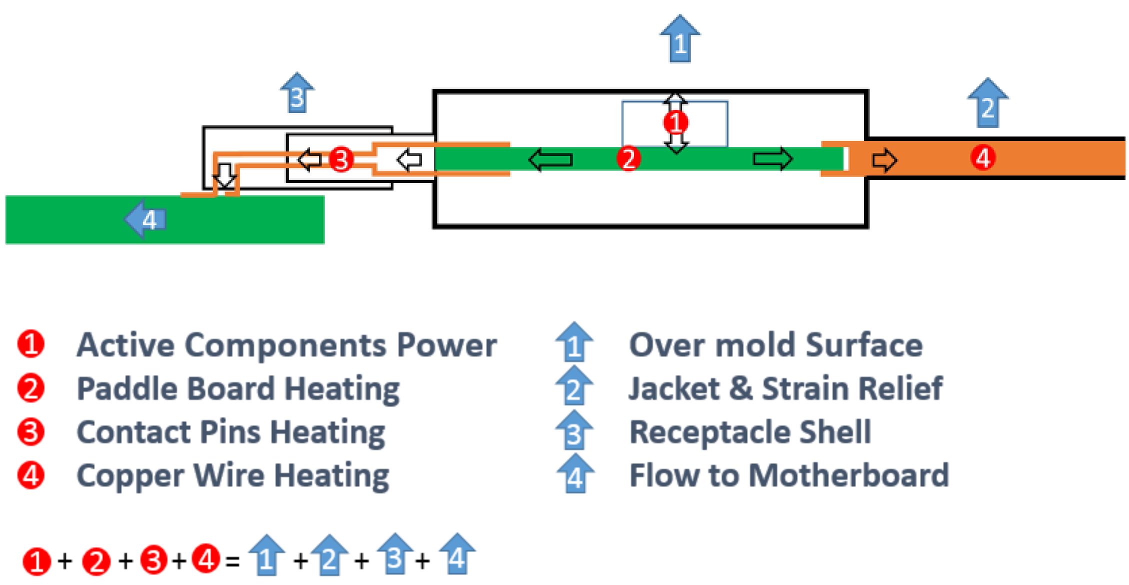
- Active component power such as re-timer, voltage regulator, etc.; the overall power inside over-mold is P_O, which is about half of VCONN power consumed by the full cable;

- Joule heat from the any conductor that carries high current, e.g. raw cable VBUS and GND copper wire, the plug PCB copper traces, contact pins of connectors, etc.

D.2.4. Heat Flow

The main power sources and heat flow paths are illustrated in Figure D-3. The overall heat generated from the cable is mainly dissipated from over-mold surfaces, cable jacket and path to motherboard. The higher thermal resistance of one heat path, the more heat it will "push off" to other heat paths and the more risk that active component junction is overheated. Since heat flow to motherboard is not a desired path from the perspective of system design, cable and over-mold design are critical to achieve balanced heat dissipation paths so not to violate either T_S or T_J requirements.

Figure D-3. Heat Sources and Heat Flow Paths



The overall heat generated from the cable should be consistent with the overall power dissipated by the cable. An example of half a 1.0 m active cable consuming 1.5 W and sourcing 5 A VBUS is shown below:

Table 5-2. Heat Sources and heat Dissipation Example (1.5W Cable and 5A)

(a) Heat Sources

Index	Heat Sources	Power (W)
1	Active Components	0.750
2	Pin Heating	0.330
3	PCB heating	0.135
4	Cable Heating	0.805
	Total Power Generation	2.020

(b) Heat Dissipation

Index	Heat Dissipation	Power (W)
1	Plug Surface	0.500
2	Cable & SR	1.120
3	Receptacle	0.050
4	Flow to Motherboard	0.350
	Total Power Dissipation	2.020

D.3. USB 3.2 Single Lane Active Cable

Based on the assumption that V_{CONN} power consumption is equally split between two ends of the cable and the 1W maximum V_{CONN} power dissipation in the USB Type-C active cable (See Table 4-5), active component power in each end or over-mold power (P_O) can go up to 0.5 W in a USB 3.2 active cable.

D.3.1. USB 3.2 Active Cable Design Considerations

The active cable designer should design for T_S less than 30 °C above T_A in the condition where thermal boundary T_{MB} is of 25 °C above T_A per Section 5.2.

D.3.1.1. USB 3.2 Active Cable in a Single Port Configuration

An active cable connected to a single port in a host or device can take full advantage of the overall plug surface area for heat dissipation. Table 5-1 shows that when P_O is 0.5 W, it is achievable to keep the plug over-mold surface temperature T_S of a single cable below the requirement, at both 3A and 5A V_{BUS}, assuming the motherboard temperature is no higher than (T_A +25) °C.

Table 5-1. USB3.2 Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary

	3 A V_{BUS}	5 A V_{BUS}
T_S (°C)	57	60

D.3.1.2. USB 3.2 Active Cable in a Multiple Port Configuration

When multi-port connector spacing is small, there is heat transfer between cables resulting in heat dissipation through natural convection being less effective than in the single port case. Radiation is also less effective due to the proximity of hot surfaces. This section lists a few typical 3-port configuration to show the impacts of receptacle spacing to the thermal performance of an active cable. For (a) and (b) minimum spacing center to center is 7 mm; for (c) it is 12.85 mm.

Figure D-4. Vertically Stacked Horizontal Connectors 3x1 Configuration (VERT)

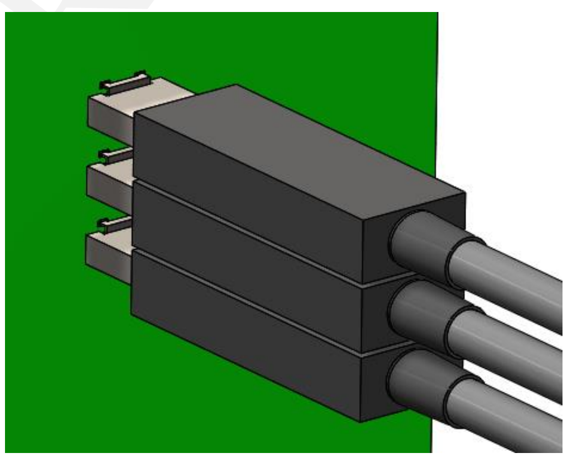


Figure D-5. Horizontally Stacked Vertical Connectors 1x3 Configuration (HZ90)

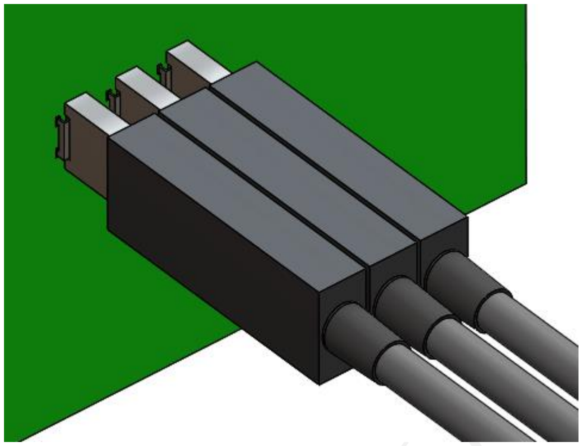
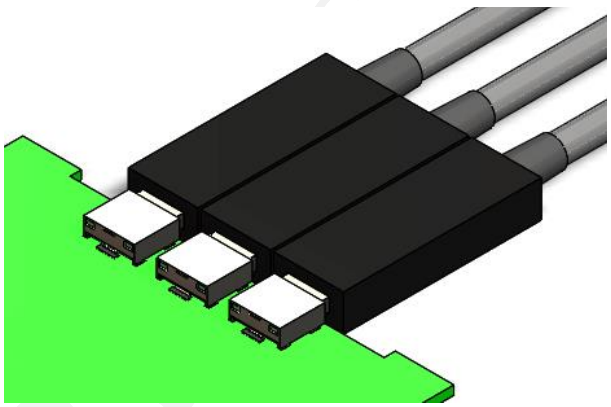


Figure D-6. Horizontally Stacked Horizontal Connector 1x3 Configuration (HORZ)

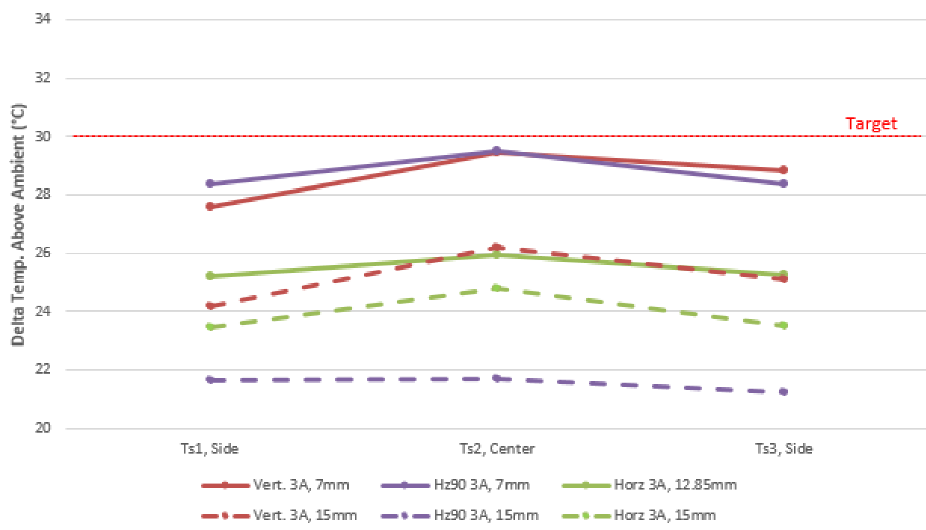


D.3.1.2.1. USB 3.2 3A Active Cable in a 3-Port Configuration

When three active cables are stacked up, the port in the center position is usually in the worst situation for heat transfer. Figure D- shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three USB 3.2 3A cables are plugged on a 60 °C motherboard in 35°C ambient.

In all 3-port configurations listed in Figure D-, Figure D-, and Figure D-, it is achievable to keep the all three plug over-mold surface temperature T_S below the requirement, at 3A V_{BUS}, assuming the motherboard temperature is no higher than (T_A +25) °C. Specific cable design should be tested and validated because the margin of center port in VERT and HZ90 is less than 1 °C at minimum port spacing in thermal modelling.

Figure D-7. USB3.2 3A Active Cable in a 3-Port Configuration



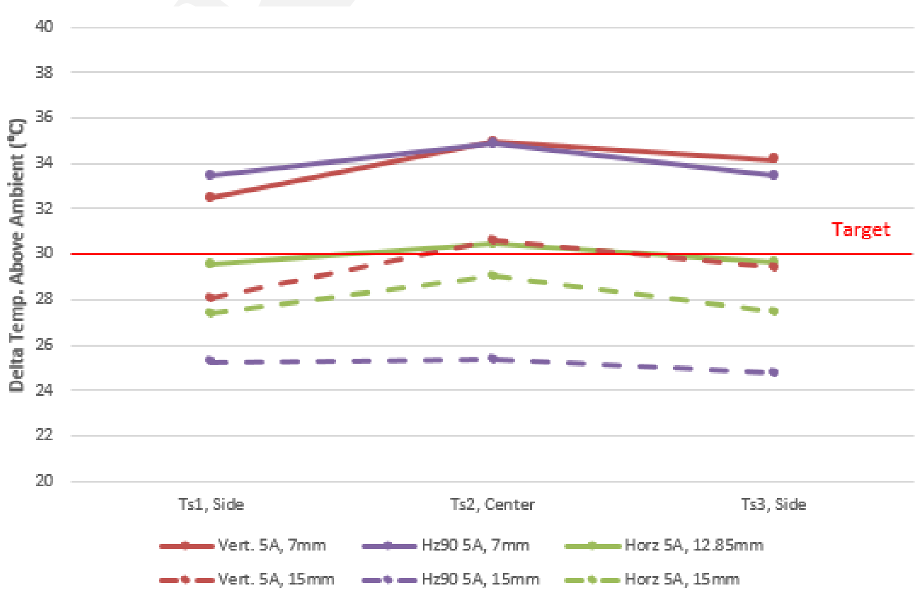
D.3.1.3. USB 3.2 5A Active Cable in a 3-Port Configuration

Figure D- shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three USB 3.2 5A cables are plugged on a 60 °C motherboard in 35 °C ambient.

All solid lines indicate the minimum spacing cases and dash lines the enlarged spacing cases. Center port is the worst case in all configurations. Three 5A cables at VERT and HZ90 configurations at minimum spacing could exceed the (T_A +30 °C) specification by up to 5 °C. HORZ configuration marginally meet spec on side ports but failed on center port.

Enlarging spacing between ports greatly reduce T_S. Especially in HZ90 configuration, spacing from 7 mm to 15 mm reduced T_S by about 8 °C.

Figure D-8. USB 3.2 5A Active Cable in a 3-Port Configuration



D.4. USB 3.2 Host and Device Design Considerations

Multi-port USB3.2 systems should follow the connector minimum spacing requirement defined in USB Type C Specification Rev. 1.3 Sec. 3.10.2.

From heat flow schematics (sec. D.2.4), when flow path 1 (over-mold surface dissipation) is less effective due to the limited spacing between cables, more heat would flow to motherboard and cable. It is recommended that system designer evaluate the heat flow to the system in a system level thermal analysis and provide a heat solution at the system level to reduce the motherboard temperature at these ports if necessary.

D.4.1. Heat Spreading or Heat Sinking from Host or Device

Proper thermal solutions may be needed on host or device to meet cable thermal requirements. Below are examples of placement of thermal interface material on host or device USB Type-C receptacle connector to spread heat or conduct heat away from chassis. This is to help either direct heat away from active components inside cable plug or limit amount of heat from flowing from host or device into the cable plug. Both would prevent the increased junction temperature of active components and increased cable plug surface temperature over the finger touch temperature limit. The heat management solution shown below are not limited to certain type or size.

Figure D-9. Example: Additional Heat Spreader on Receptacle in Host or Device

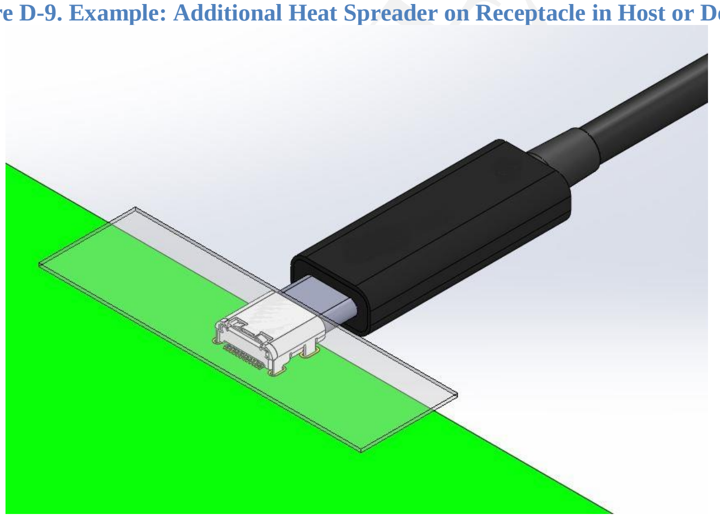
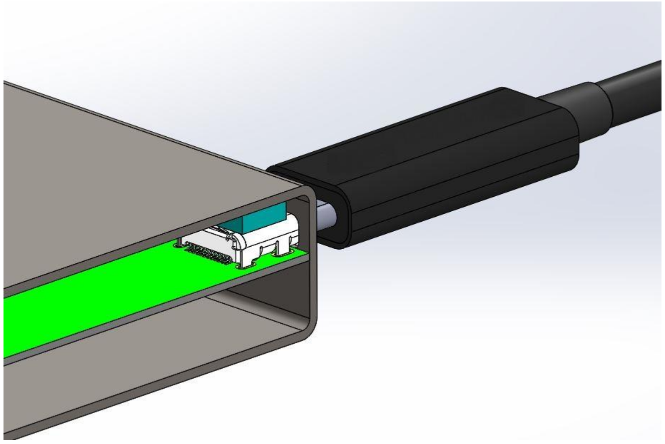


Figure D-10. Example: Heat Sinking by Chassis of Host or Device



D.4.2. Motherboard Temperature Control

Motherboard as a thermal boundary for the cable, could impact the thermal performance of cable greatly. Lowered mother temperature especially the area local around the receptacles could help reduce plug surface temperature T_S and component junction temperature T_J. See more discussion in Section D.5.1.1.1.

D.4.3. Wider Port Spacing for Multiport Application

Wider spacing between receptacle connectors, especially when no additional heat sinking is available, is recommended for multiport application. Section D.3.1.2.1 and section D.3.1.3 show the impact from adjustment of port spacing.

D.4.4. Power Policies

(To be added)

D.5. Two Lane Active Cables

USB3.2 defines two lanes of SuperSpeed data and in two-lane operation typically has higher active component power consumption than USB3.2 single-lane Gen 2 active cables. Higher power could heat up the over-mold and raise T_S above user comfort zone when plugging or unplugging the cable.

USB3.2 two-lane active cable may consume up to 1.5 W of power from V_{CONN}. This compares with the 1 W allowed for USB 3.2 single-lane active cables.

Section D.5.1 shows T_S resulting from 0.75 W over-mold power P_O in a 1.5 W two-lane USB 3.2 active cable for a certain design, in both single-port and multiple-port configurations. Results reveals that thermal solution is necessary to meeting cable design requirements especially in multiple-port configuration.

Both over-mold power P_O and thermal boundary of the cable T_{MB} have impacts on T_S. The correlation of three are studied in Section D.5.1.1.2 which helps system and cable designer to take both factors into consideration.

D.5.1. USB 3.2 Cable Design Considerations

The cable designer should design for T_S of the over-mold less than 30 °C above T_A in the condition where thermal boundary T_{MB} is of 25 °C above T_A per Section 5.2.

D.5.1.1.1. USB 3.2 Active Cable in a Single Port Configuration

An active cable connected to a single port in a host or device can take full advantage of the overall plug surface area for heat dissipation. Table 5-2. USB3.2 Active Cable Design Single Port Case Study 35C Ambient and 60C Thermal Boundary shows that when P_O is 0.75 W, it is achievable to keep the plug over-mold surface temperature T_S of a single cable below (T_A +30) °C at both 3A and 5A V_{BUS}, assuming the motherboard temperature is no higher than (T_A +25) °C.

Table 5-2. USB3.2 Active Cable Design Single Port Case Study 35C Ambient and 60C Thermal Boundary

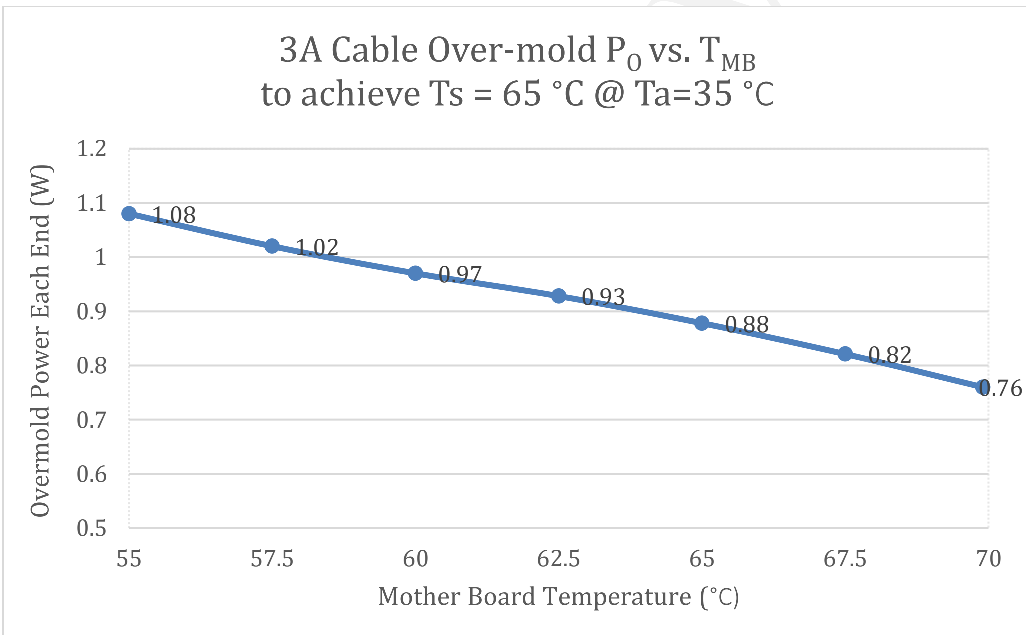
	3A Vbus	5A Vbus
T_S (°C)	61	64

In 5A Vbus case, T_S is much closer to specified limit than 3A V_{BUS} case (Section D.3.1.1), so test and verification of thermal design is highly recommended.

D.5.1.1.2. Impact of Over-mold Power P_O and Thermal Boundary Temperature T_{MB}

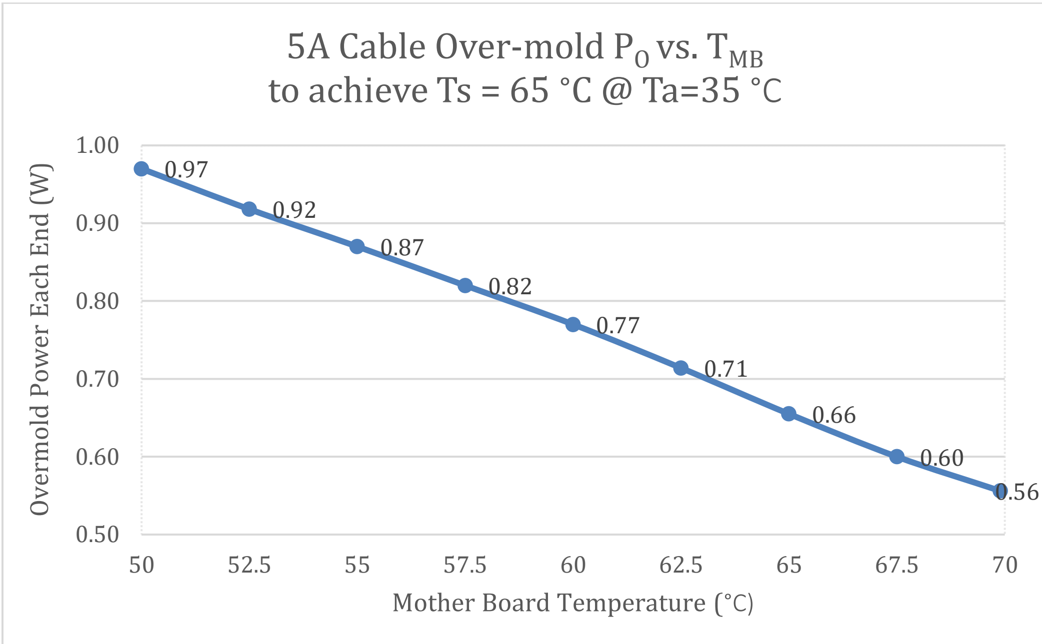
In Figure D- below, the area under graph indicate the combination of over-mold power P_O and thermal boundary temperature T_{MB} that can achieve Ts < (T_A +30) °C in a single port configuration in a 3A V_{BUS} application.

Figure D-11. Impact of Over-mold Power P_O and Thermal Boundary Temperature TMB at 3A VBUS in a Single Port Configuration



In Figure D-1 below, the area under graph indicate the combination of over-mold power P_O and thermal boundary temperature T_{MB} that can achieve Ts < (T_A +30) °C in a single port configuration in a 5A V_{BUS} application.

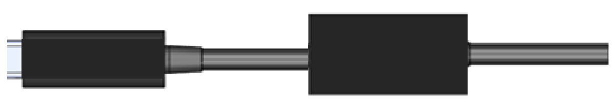
Figure D-1. Impact of Over-mold Power PO and Thermal Boundary Temperature TMB at 5A VBUS in a Single Port Configuration



D.5.1.1.3. Dongle Cable

When overall active component power is higher than the maximum over-mold power P_O that could meet T_S requirement, cable may be re-designed to move the thermal load away from the USB Type-C plug over-mold such as in a dongle Cable in Figure D-

Figure D-13. USB 3.2 Active Cable Dongle Design (One End Shown)



The cable should be designed so that the over-mold directly plugged in the host or device dissipates no more than maximum P_O and extra heat is migrated to another part of the cable such as a dongle, so neither extra heat will flow into host and device, nor over-mold surface temperature is too hot for users to touch.

D.5.1.2. USB 3.2 Active Cable in a Multi-Port Configuration

Multi-port connector spacing results in less effective heat dissipation by natural convection and radiation. This section lists a few typical 3-port configuration to show the impacts of receptacle spacing to the thermal performance of USB3.2 active cables. Naming of configurations used in this section are the same as in Section D.3.1.2.

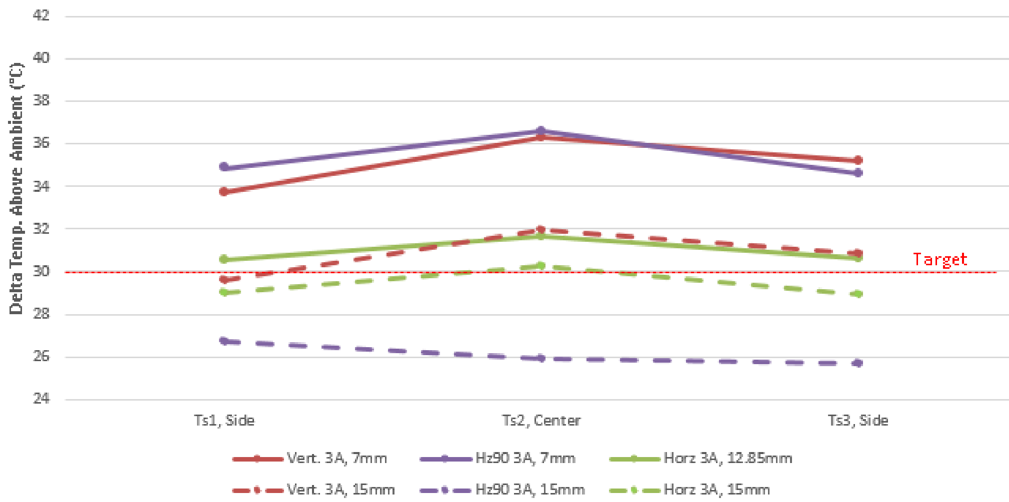
D.5.1.2.1. USB 3.2 3A Active Cable in a 3-Port Configuration

Figure D- shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three USB 3.2 3A VBUS and 1.5 W cables are plugged on a 60 °C motherboard in 35 °C ambient. The port in the center position is usually in the worst situation for heat transfer.

All solid lines indicate the minimum spacing cases and dash lines the enlarged spacing cases. Center port is the worst case in all configurations. T_S of center port in VERT and HZ90 configurations at minimum spacing could be more than 6 °C over the (T_A +30 °C) specification and in HORZ configuration about 2 °C over specification.

Enlarging spacing between ports could greatly reduce T_S. Especially in HZ90 configuration, spacing from 7 mm to 15 mm reduced T_S by about 11 °C, which help to reduce T_S to meet specification.

Figure D-14. USB 3.2 3A Active Cable in a 3-Port Configuration



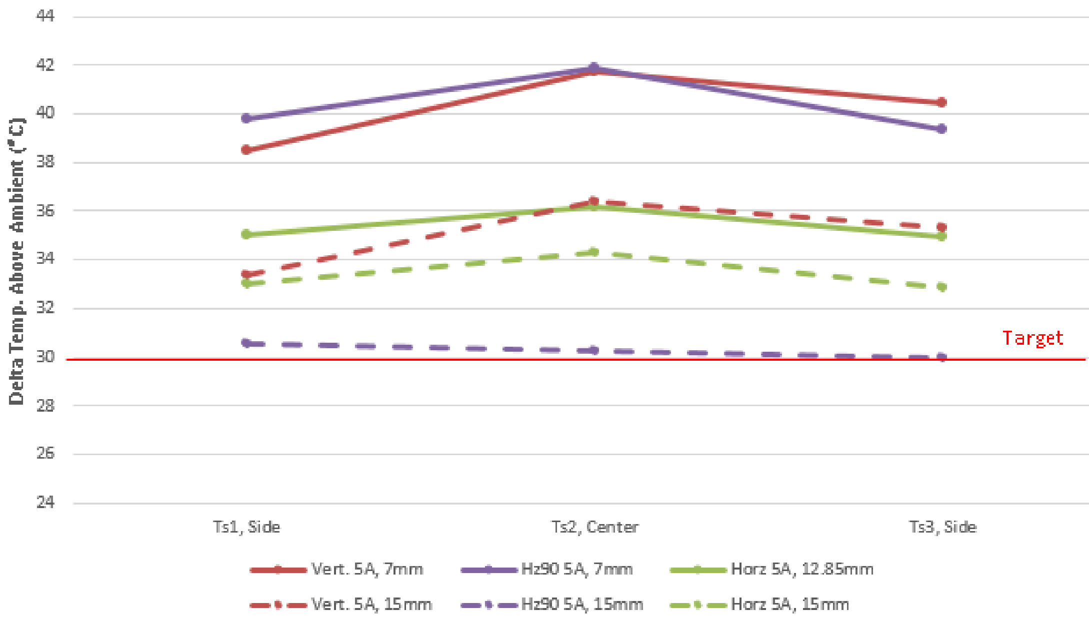
D.5.1.2.2. USB 3.2 5A Active Cable in a 3-Port Configuration

Figure D- shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three USB 3.2 5A VBUS and 1.5 W cables are plugged on a 60 °C motherboard in 35 °C ambient. The T_S port in the center position is still the highest of all three in all cases.

In all 3-port configurations listed in Figure D-, Figure D-, and Figure D-, plug over-mold surface temperature T_S of all three ports have exceeded the requirement, at 5A VBUS, assuming the motherboard temperature is at (T_A +25) °C. T_S of center port in VERT and HZ90 configurations at minimum spacing are the highest, near 12 °C over the (T_A +30 °C) specification and in HORZ configuration about 6 °C over specification.

Enlarging spacing between ports could help reduce T_S. The largest reduction is seen in HZ90 configuration, which is near 12 °C and it brings T_S back close to target, when spacing is enlarged from 7 mm to 15 mm. However, when port spacing is not sufficient to bring T_S down to desired range, further design options in cable and host/device should be investigated.

Figure D-15. USB 3.2 5A Active Cable in a 3-Port Configuration



D.5.2. USB 3.2 Host and Device Design Considerations

Host and device designers should consider solutions to reduce T_{MB} as well as provide more heat sinking capability at system level as described in Section D.4.