

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: PCIe PERST# Behavior Correction
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:

Removes some inaccuracies in description of PERST# propagation.

Benefits as a result of the changes:

More accurate description of how PERST# is asserted and de-asserted.
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An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
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None

An analysis of the hardware implications:
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None

An analysis of the software implications:
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None

An analysis of the compliance testing implications:
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None

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Actual Change

(a). Section 11.1.1.4 PERST

Make the following changes:

11.1.1.4 PERST

11.1.1.4.1 PERST Tunneled Packets

PERST Active and PERST Inactive Tunneled Packets are used to propagate PCIe PERST# assertion and de-assertion. A Router shall send PERST Active and PERST Inactive packets only from a Downstream PCIe Adapter. The payload for a PERST Active Tunneled Packet and a PERST Inactive Tunneled Packet shall consist of one DW that contains a value of 0000 0000h.

~~11.1.1.4.2 PERST Propagation~~

~~By default, a Device Router asserts PERST# on all physical PCIe ports and internal PCIe ports.~~

11.1.1.4.3 PERST Activation in a Host Router

Upon detecting an assertion of PERST# ~~on a Downstream PCIe Adapter~~, a Host Router shall:

1. Discard any queued Tunneled Packet in the PCIe Adapter Layer.
2. Send at least three PERST Active Tunneled Packets on ~~all the~~ Downstream PCIe Adapters ~~that have the if its Path Enable bit is~~ set to 1b.

11.1.1.4.4 PERST Activation in a Device Router

~~When a Device Router enters Uninitialized Unplugged state, it shall assert PERST# on its internal PCIe upstream port.~~

~~When a Device Router receives a PERST Active Tunneled Packet, or the Path Enable bit in the Upstream PCIe Adapter is set to 0b, it shall:~~

1. Discard any Tunneled Packets that are queued in a PCIe Adapter Layer.
2. Send at least 3 PERST Active Tunneled Packets on all Downstream PCIe Adapters that have the *Path Enable* bit set to 1b.
3. ~~The Router shall also a~~Assert PERST# on its internal PCIe upstream port ~~all physical PCIe ports and to the internal PCIe Port.~~

~~While PERST# is asserted, a Downstream PCIe Adapter Layer shall discard any received PCIe Tunneled Packets. The Adapter Layer shall not send any PCIe tunneled Packets except for the PERST Active Tunneled Packets.~~

11.1.1.4.5 PERST Inactivation in a Host Router

Upon detecting a de-assertion of PERST# ~~on a Downstream PCIe Adapter~~, a Host Router shall send at least 3 PERST Inactive Tunneled Packets on ~~all the~~ Downstream PCIe Adapters ~~that have the if its Path Enable bit is~~ set to 1b.

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

11.1.1.4.6 PERST Inactivation in a Device Router

After receiving a PERST Active Tunneled Packet, ~~or after the *Path Enable* bit the Upstream PCIe Adapter is set from 0b to 1b~~, if a Device Router receives any PCIe Tunneled Packet other than a PERST Active Tunneled Packet on its Upstream PCIe Adapter, it shall:

1. Send at least 3 PERST Inactive Tunneled Packets on all Downstream PCIe Adapters that have the *Path Enable* bit set to 1b.
2. De-assert PERST# on ~~its internal PCIe upstream port all PCIe physical ports and to the internal PCIe Port.~~

After PERST# is de-asserted, a Downstream PCIe Adapter Layer shall not forward to the internal PCIe Port any Ordered Sets, packets, or events that were received before or during PERST# assertion.

(b). Section 11.3.2 Path Tear-Down

Make the following changes:

- If the PCIe Adapter is an Upstream PCIe Adapter, drive PERST# ~~to default~~ as defined in Section 11.1.1.4.3.