USB4 Re-timer 0.96 ENGINEERING CHANGE NOTICE FORM

Title: SSC Clock Switch Timing Change
Applied to: USB4 Re-timer Specification Version 0.96

Brief description of the functional changes:
Changes the timing requirement of the SSC Clock Switch to allow a smoother (df/dt) transition.

Benefits as a result of the changes:
Allows clock transition within the df/dt requirements.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
None

An analysis of the hardware implications:
None

An analysis of the software implications:
None

An analysis of the compliance testing implications:
Increase the timeout for SSC Clock Switch.

USB4 Re-timer 0.96 ENGINEERING CHANGE NOTICE FORM

Actual Change

(a). Table 4-6 Re-timer Timing Parameters, Page 41

From Text:

tSwitchSSC	The time to perform clock switch during exit from a CLx state, with an SSC receive clock.	--	60	µs

To Text:

tSwitchSSC	The time to perform clock switch during exit from a CLx state, with an SSC receive clock.	--	75~~60~~	µs