USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: TBT3-Compatible Response to LTTPR DPCD Register
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:
If LTTPR is not supported by the DP OUT Adapter, a DP IN Adapter terminates locally the AUX READ Transactions to LTTPR DPCD address space and responds with data equal to 0h.

Benefits as a result of the changes:
Improved interoperability with a TBT3 device that doesn't support LTTPR and has an active DP Cable connected to it's DP OUT Adapter.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
None

An analysis of the hardware implications:
Need to block the above read transactions and generate AUX Response.

An analysis of the software implications:
None

An analysis of the compliance testing implications:
Update the CTS to check the scenario.

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Actual Change

(a). Section 13.8.1.1

13.8.1.1 DP IN Adapter Requirements

A DP IN Adapter operating in TBT3-Compatible mode follows the requirements listed in Section 10.4.4.2.1 except the following:

- The Link Status DPCD registers, as defined in Table 10-9, shall be mapped statically as Internal registers.
- DPCD address 00600h is mapped as Internal register.
- An AUX Read Transaction to the LTTPR DPCD Field, addresses F0000h-F02FFh, are mapped as Internal registers. A DP IN Adapter shall set the data of the AUX Response to 0h.

A DP IN Adapter operating in TBT3-compatible mode follows the requirements listed in Section 10.4.4.5 except the following:

- DSC Support field in the DSC SUPPORT DPCD register shall always be set to 0b.
- FEC_CAPABLE field in FEC_CAPABILITY DPCD register shall always be set to 0b.
- ~~PHY_REPEATER_CNT field in PHY_REPEATER_CNT DPCD register shall always be set to 0b.~~