USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: TBT3 CM Buffer Allocation
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:

Describes the static TBT3 CM Buffer allocation per link and Path.

Benefits as a result of the changes:

The spec is aligned to the current ecosystem.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

None

An analysis of the hardware implications:

None

An analysis of the software implications:

None

An analysis of the compliance testing implications:

None

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Actual Change

(a). Section 13.3

13.3.4 Buffer Allocation

This section only applies to a Device Router that supports TBT3-Compatibility on its UFP.

A TBT3 Connection Manager sets the buffer allocation in a static manner, according to Table 13-11.

Table 13-11. Buffer Allocation by TBT3 Connection Manager

	Dual Lane Link	**Single Lane Link**
Control	Assumes 2 buffers	
PCIe Path	32 buffers	16 buffers
Host-to-Host Path	14 buffers	6 buffers
DP Aux Path	1 buffer	
DP Main-Link Path	The remaining buffers = Total Buffers – 50[1]	The remaining buffers = Total Buffers – 26[1]
Note 1: A TBT3 CM assumes two DP Tunnels through a port, therefore it will keep 2 buffers for DP Aux Path.		