USB4™ Designated Vendor Specific Extended Capability (DVSEC) for Power Management

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1 Preface

1.1 Scope of Document

This document is targeted at USB4 host developers and should be read in conjunction with the Connection Manager Notes in the USB4 Specification and the USB4 Connection Manager Guide.

1.2 Related Documents

Universal Serial Bus (USB4™) Specification, Version 1.0 with Errata and ECN through October 15, 2020 (USB4 Specification)

USB4 Connection Manager (CM) Guide, Revision 1.0, [to be published] – (Connection Manager Guide)

PCI Express® Base Specification, Revision 4, Version 1, September 27, 2017 (PCIe Specification)

1.3 Terms and Abbreviations

This specification uses the same terms and abbreviations as defined in the USB4 Specification.

1.4 Documentation Conventions

1.4.1 Capitalization

Some terms are capitalized to distinguish their definition in the context of this document from their common English meaning. Words not capitalized have their common English meaning.

1.4.2 Italic Text

Italic text is used to identify variable names, register field and packet field names, or reference document titles.

1.4.3 Numbers and Number Bases

Hexadecimal numbers are written with a lower case “h” suffix, e.g. FFFFh and 01h. Hexadecimal numbers larger than four digits are represented with a space dividing each group of four digits, e.g. 1EFF FFFF FFFFh. Binary numbers are written with a lower case “b” suffix, e.g. 1001b and 01b. Binary numbers larger than four digits are written with a space dividing each group of four digits, e.g. 1010 1000 1100b.

All other numbers are decimal.

1.4.4 Bit, Byte, DW, and Symbol Conventions

A bit, byte, DW, or Symbol residing in location n within an array is denoted as bit[n], byte[n], DW[n], or Symbol[n].

A sequence of bits, bytes, DWs, or Symbols residing in locations n to m (inclusive) within an array is denoted as bit[m:n], byte[m:n], DW[m:n], or Symbol[m:n].

1.4.5 Word Usage

The word “shall” is used to indicate mandatory requirements. Mandatory requirements are strictly to be followed in order to conform to this specification and no deviation is permitted.

The phrase “it is recommended” is used to convey that, among several possibilities, one is preferred but not necessarily required.

The word “may” is used to indicate a course of action permissible within the limits of the specification. The word “can” is used only for statements of possibility or capability (i.e. “can” equals “is able to”).

1.4.6 Reserved Values and Fields

Reserved is a keyword indicating reserved bits, bytes, words, fields, and code values that are set-aside for future standardization. The use and interpretation of these may be specified by future extensions to this specification and, unless otherwise stated, shall not be utilized or adapted by vendor implementation. A reserved bit, byte, work or field shall be set to zero by the sender and shall be ignored by the receiver. Reserved field values shall not be sent by the sender and, if received, shall be ignored by the receiver.

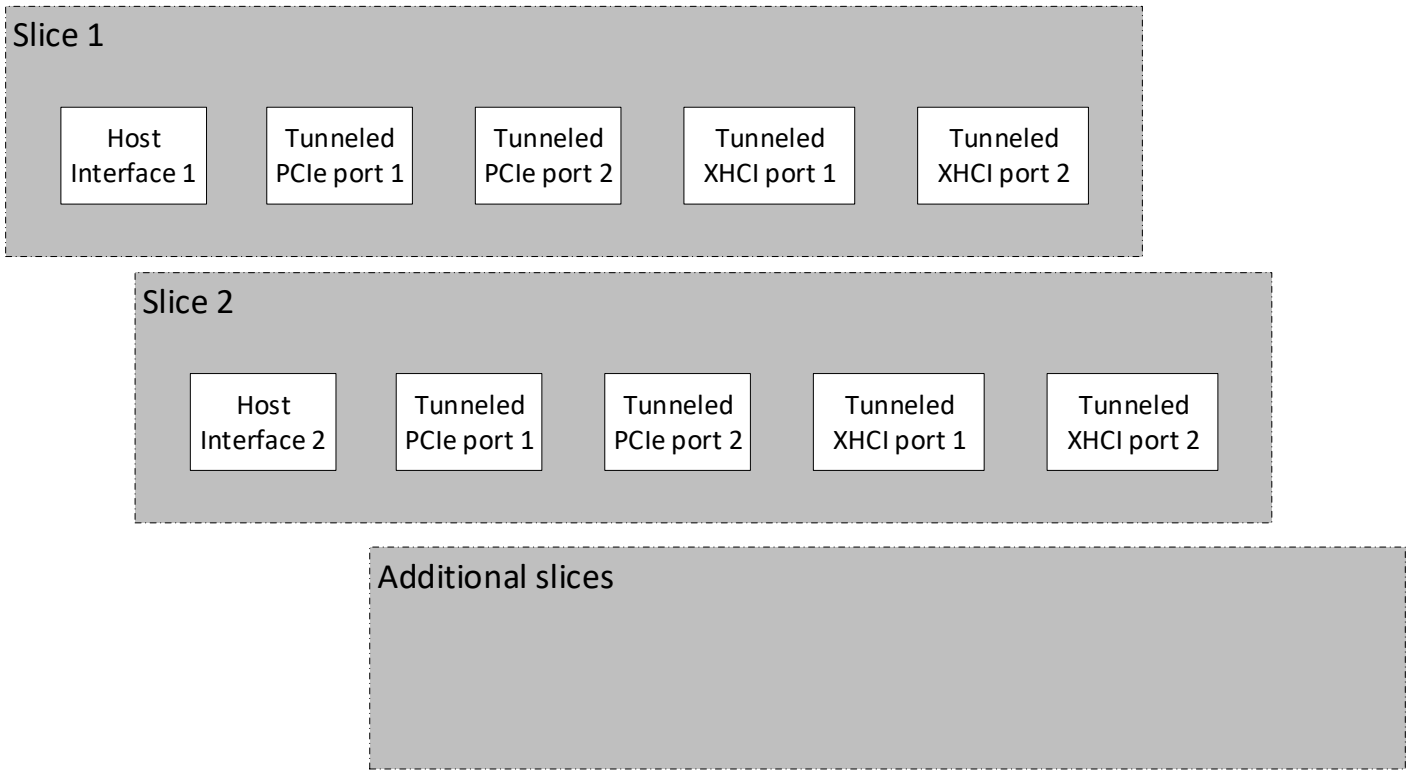
2 Introduction

The PCIe specification defines a “Designated Vendor Specific Extended Capability” (DVSEC), which is an extended capability that is used by a vendor to define a configuration register structure that can be implemented by all vendors, while providing a consistent hardware/software interface. This document defines the USB4™ DVSEC registers and is applicable for connection managers that use a PCIe-based host interface.

Platforms with USB4 can have multiple ports requiring multiple instances of USB4 host interfaces. With an Operating System-owned connection manager, there is a load order dependency between the bring up of connection manager and the enumeration of the devices behind the tunneled ports. Specifically, the connection manager will have to load (or resume) first to setup the tunneled paths, followed by the enumeration of devices behind the tunneled ports. The power dependency will have to be maintained during boot up and during exit from low power states.

The USB4 DVSEC helps define a power relation between two or more tunneled ports that do not appear within a tree topology and could be peer devices of the USB4 host interface. USB4 solutions that choose to implement a USB4 DVSEC shall also implement the PCIe Device Serial Number Extended Capability as defined in the PCIe specification and ensure that all PCIe DN bridges and endpoints of the same enclosure return the same Device Serial Number. When possible, the recommendation is to implement the USB4 DVSEC in the DN bridge of the PCIe switch that connects to the relevant endpoint (PCIe/Host Interface/xHCI).

Figure 2-1. Example Topology of a USB4 Host Controller with Multiple Host Interfaces



3 USB4 DVSEC Header

Figure 3-1. USB4 DVSEC Header

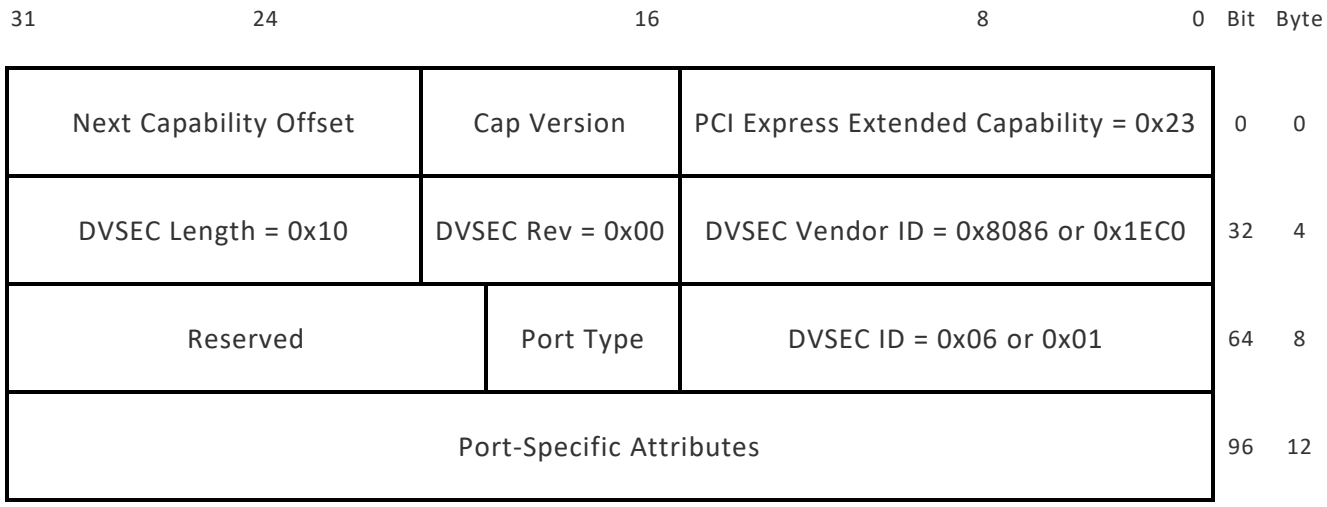


Table 3-1. USB4 DVSEC Header Fields

Bits	Field	Type	Description
15:0	*PCI Express Extended Capability*	RO	This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Designated Vendor-Specific Extended Capability is 0023h.
19:16	*Cap Version*	RO	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Shall be 1h for this version of the specification.
31:20	*Next Capability Offset*	RO	This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus shall always be either 000h (for terminating list of Capabilities) or greater than 0FFh.
47:32	*DVSEC Vendor ID*	RO	This field is the Vendor ID associated with the vendor that defined the contents of this capability. Shall be 0x8086 (if the vendor intends to use the Intel VID) or 0x1ECO (if the vendor intends to use the USBIF VID).
51:48	*DVSEC Rev*	RO	This field is a vendor-defined version number that indicates the version of the DVSEC structure. Software needs to qualify the DVSEC Vendor ID and DVSEC ID before interpreting this field. Shall be 0h.
63:52	*DVSEC Length*	RO	This field indicates the number of bytes in the entire DVSEC structure, including the PCI Express Extended Capability header, the DVSEC Header 1, DVSEC Header 2, and DVSEC vendor-specific registers.

Bits	Field	Type	Description
			Shall be 10h.
79:64	*DVSEC ID*	RO	This field is a vendor-defined ID that indicates the nature and format of the DVSEC structure. Software needs to qualify the DVSEC Vendor ID before interpreting this field. Shall be set to 06h if the DVSEC vendor ID field is set to 0x8086. Shall be set to 01h if the DVSEV vendor ID field is set to 0x1EC0.
82:80	*Port Type*	RO	0x0 - Native Host Interface 0x1 - PCIe Tunneled Port 0x2 - USB Tunneled Port 0x3-0x7 - Reserved
95:83	*Reserved*	RO	Reserved.
127:96	*Port-Specific Attributes*	RO	Port specific attributes (see Sections 4, 5, and 6).

4 NHI-Specific Attributes

NHI (Native Host Interface) attributes are applicable for USB4 DVSEC with Port Type = 0x0 (see Table 3-1).

Figure 4-1. NHI-Specific Attributes

Table 4-1. NHI-Specific Attribute Fields

Bits	Field	Type	Description
2:0	NHI_Instance#	RO	NHI instance number.
31:3	Reserved	RO	Reserved.

5 PCIe-Specific Attributes

PCIe attributes are applicable for USB4 DVSEC with Port Type = 0x1 (see Table 3-1). Along with the mapping of the port to the corresponding NHI#, the attributes also provide hints to system software for efficient enumeration of downstream devices.

Figure 5-1. PCIe-Specific Attributes

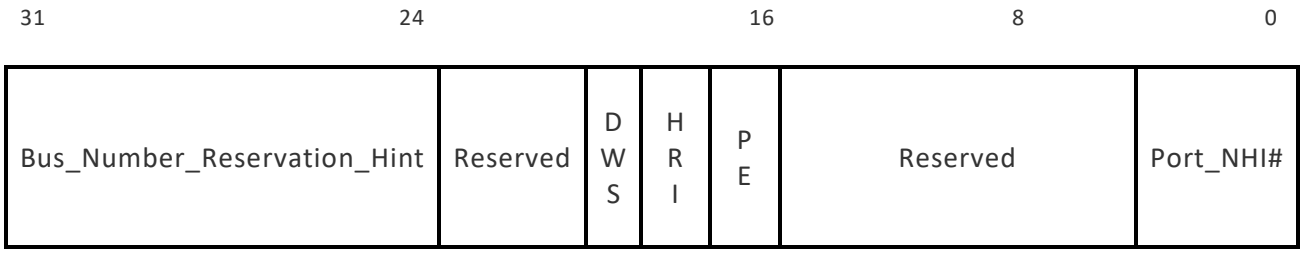


Table 5-1. PCIe-Specific Attribute Fields

Bits	Field	Type	Description
2:0	*Port_NHI#*	RO	Port mapping to NHI instance# 0x0 - 0x6 mapped to NHI# accordingly 0x7 Not mapped to NHI
15:3	*Reserved*	RO	Reserved.
17:16	*Port_Expandability (PE)*	RO	0x0: Not implemented 0x1: Non-Expandable port 0x2: Expandable (or daisy chain capable) port with resource requirements that can change at run time. 0x3: Reserved This field is applicable to root ports or switch downstream ports. This field provides hints to system software to determine if this port is expandable or not. This hint allows the system software to appropriately reserve resources based on the port type.
19:18	*Host_Router_Indication (HRI)*	RO	00: Not implemented 01: Host - Indicates a port that is physically a part of the host system 10: Reserved 11: Host External facing - indicates a port that is external facing port, accessible to users, of a host system
20:20	*D3Cold_Wake_Support (DWS)*	RO	0: Not implemented 1: D3Cold wake supported This field is applicable to root ports or switch downstream ports. This field indicates D3Cold wake support for hierarchy underneath.
23:21	*Reserved*	RO	Reserved.

Bits	Field	Type	Description
31:24	*Bus_Number_Reservation_Hint*	RO	0x00: Not implemented 0x01-0xFE: Number of buses required 0xFF: unknown This field is applicable to root ports or switch downstream ports. This hint allows system software to determine number of buses to reserve for the hierarchy underneath.

6 USB-Specific Attributes

USB attributes are applicable for USB4 DVSEC with Port Type = 0x2 (see Table 3-1). The number of the xHCI ports may be increased to more than eight by increasing the DVSEC length accordingly.

Figure 6-1. USB-Specific Attributes

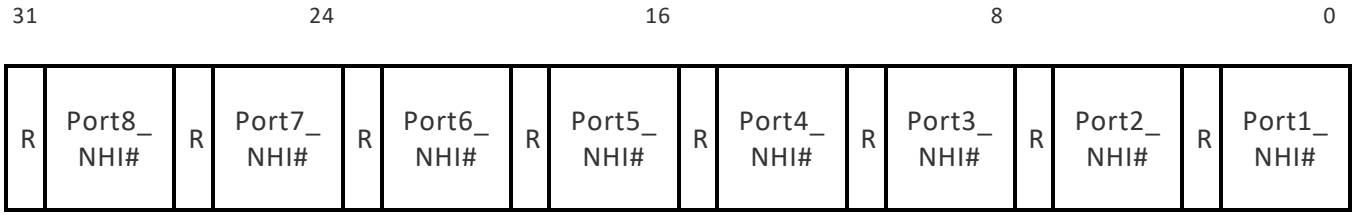


Table 6-1. USB-Specific Attribute Fields

Bits	Field	Type	Description
2:0	Port1_NHI#	RO	Port mapping to NHI instance# 0x0 - 0x6 mapped to NHI# accordingly 0x7 Not mapped to NHI
3:3	*Reserved*	RO	Reserved.
6:4	*Port2_NHI#*	RO	Port mapping to NHI instance# 0x0 - 0x6 mapped to NHI# accordingly 0x7 Not mapped to NHI
7:7	*Reserved*	RO	Reserved.
10:8	*Port3_NHI#*	RO	Port mapping to NHI instance# 0x0 - 0x6 mapped to NHI# accordingly 0x7 Not mapped to NHI
11:11	*Reserved*	RO	Reserved.
14:12	*Port4_NHI#*	RO	Port mapping to NHI instance# 0x0 - 0x6 mapped to NHI# accordingly 0x7 Not mapped to NHI
15:15	*Reserved*	RO	Reserved.
18:16	*Port5_NHI#*	RO	Port mapping to NHI instance# 0x0 - 0x6 mapped to NHI# accordingly 0x7 Not mapped to NHI
19:19	*Reserved*	RO	Reserved.
22:20	*Port6_NHI#*	RO	Port mapping to NHI instance# 0x0 - 0x6 mapped to NHI# accordingly 0x7 Not mapped to NHI
23:23	*Reserved*	RO	Reserved.

Bits	Field	Type	Description
26:24	*Port7_NHI#*	RO	Port mapping to NHI instance# 0x0 - 0x6 mapped to NHI# accordingly 0x7 Not mapped to NHI
27:27	*Reserved*	RO	Reserved.
30:28	*Port8_NHI#*	RO	Port mapping to NHI instance# 0x0 - 0x6 mapped to NHI# accordingly 0x7 Not mapped to NHI
31:31	*Reserved*	RO	Reserved.