USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: DP FEC Jitter
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:
Adds FEC cycles into the DP IN Jitter calculation.

Benefits as a result of the changes:
Calculation is more accurate.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
None

An analysis of the hardware implications:
None

An analysis of the software implications:
None

An analysis of the compliance testing implications:
None

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Actual Change

(a). 10.5.4.2 Accumulation Cycles

Accumulation Cycles are counted in Link Symbol clock cycles, where one Accumulation Cycle equals one Link Symbol clock cycle. The number of Accumulation Cycles that a DP OUT Adapter waits is a function of the following:

- DP IN Jitter – the Jitter between Tunneled Packets from the DP IN Adapter.
    - The delay from when a DP construct is received over the DP Main-Link until a ~~the~~ DP IN Adapter generates the Main-Link Tunnel Packet can vary where:
        - Minimal delay is for MSA and BS.
        - Maximal delay is:
            - MST: 17 MTPs + Max FEC Cycles[1] = 1088 + 37 = 1125 LS Cycles.
            - SST: 16 Video TUs + Max FEC Cycles = 1024 + 37 = 1061 LS Cycles.
- USB4 Delay Jitter – the Jitter cause by delays over the USB4 Fabric.
    - The following can create delays at the Egress Adapter for each Hop:
        - Time Sync Packets.
        - Credit Grant Packets.
        - Control Packets.
        - Other Tunneled Packets (on both same priority and lower priority Paths).
        - Packet forwarding jitter within a Router.
    - The delay depends on the number Credit Grant Records, the number of additional DP Paths, the USB4 Link speed, and the assumptions regarding how many delay factors on average affect each Hop.

A DP OUT Adapter shall report the Maximum Accumulation Cycles it performs. The maximum is needed when operating at the maximum DisplayPort Link Rate.

The following is an example of a DP OUT Adapter that supports the maximum DP Link Rate of HBR3, supports MST, and assumes that a DP Tunneled Packet is delayed at every Hop by two full size Packets:

- Worst case Accumulating Cycles = (DP IN Jitter) + (USB4 Delay Jitter)

  = (17MTPs+Max FEC Cycles) + ((((5 Hops * 2 * 260 Bytes* 8) * USB4 UI) / HBR3 UI) + (6 Hops * tTunneledPacketJitter / HBR3 UI))

  = (1088+37) + ((20800 Bits * 0.1ns / 1.23ns) + (6 * 100ns / 1.23ns)) = ~~3268~~ 3305 Link Symbol Cycles

[1] Max FEC Cycles = 3x FEC_PARITY_PH + 1x FEC_PM = 3x12 + 1x1 = 37 Cycles