USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: CLx Support of TBT3 Cable
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:

When Link is TBT3, during Phase 1 of the Lane Initialization, the Router should get information about the Cable connected to determines whether or not the Cable supports CLx protocol. This comes to notify the CM about Optical Limit cable.

Benefits as a result of the changes:

CLx should not be enabled when using a TBT3 Cable that doesn't support the CLx Protocol.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

TBT3 Compatible Routers shall get information from the PD to determine if the connected Cable supports CLx.

An analysis of the hardware implications:

None

An analysis of the software implications:

None

An analysis of the compliance testing implications:

Need to verify that when connected with an Optical Limit cable the Router doesn't set the CPS bits.

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Actual Change

(a). Section 13.2.1.4.1 Phase 1 – Determination of Initial Conditions

From Text:

During phase 1, Router A determines whether or not TBT3 Mode is established on the Link. See the USB PD Specification and the USB Type-C Specification for how to determine if TBT3 Mode is established.

A Router shall not continue on to Phase 2 until it has obtained the connection information described in this section and in Section 4.1.2.1. If TBT3 Mode is established on the Link, a Router shall proceed with Lane Initialization as defined in Section 4.1.2 with the changes defined in this chapter.

To Text:

During phase 1, Router A determines whether or not TBT3 Mode is established on the Link and whether or not the Cable connected supports CLx. See the USB PD Specification and the USB Type-C Specification for how to determine if TBT3 Mode is established and Cable support of CLx.

A Router shall not continue on to Phase 2 until it has obtained the connection information described in this section and in Section 4.1.2.1. If TBT3 Mode is established on the Link, a Router shall proceed with Lane Initialization as defined in Section 4.1.2 with the changes defined in this chapter.

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(b). Table 13-18 USB4 Port Region Fields, Page 566

From Text:

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
151	LINK_ATTR	18	**CLx Protocol Support (CPS)** This bit indicates that the Router supports the Low Power protocol. When a Router supports the Low Power protocol, it either accepts or rejects entry to a CLx state as defined in Section 4.2.1.6. A Router shall set this bit to 1b if the Sideband Channel operates as a USB4 Sideband Channel. A Router shall set this bit to 0b if the Sideband Channel operates as a TBT3-Compatible Sideband Channel.	RO	0

To Text:

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
151	LINK_ATTR	18	**CLx Protocol Support (CPS)** This bit indicates that the Router and the Cable ~~-support~~s the Low Power protocol. When a Router supports the Low Power protocol, it either accepts or rejects entry to a CLx state as defined in Section 4.2.1.6. A Router shall set this bit to 1b if the Sideband Channel operates as a USB4 Sideband Channel and the Cable supports CLx. Otherwise, ~~A~~a Router shall set this bit to 0b ~~if the Sideband Channel operates as a TBT3-Compatible Sideband Channel~~.	RO	0