USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: Change in CL1 Response
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:
There are cases where the CL1 objection is asserted on a responding port, while CL0s entry and exit time is subject to temporary conditions which would not allow to meet the assumed link unavailability budget. For example - a port in CL0s.TX that receives CL1_REQ, but it expects the resume time back to CL0 to be longer than required may respond with CL_NACK instead of CL0s_ACK. It is still assumed that ports would normally prefer entering CL0s rather declining CLx entry initiation with CL_NACK.

Benefits as a result of the changes:
Increase the robustness for supporting CLx, and better guarantee a higher bound for USB4 link resumption time which would assist latency sensitive applications, mostly those which are using PCIe LTR.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
Lane Adapters with support for CLx are already required to support CL_NACK during CL0. This ECR requires Lane Adapters to also be able to transition to CL0 upon receiving CL_NACK when trying to transition from CL0s to CL1 or CL2..

An analysis of the hardware implications:
None

An analysis of the software implications:
None

An analysis of the compliance testing implications:
CL_NACK should not be considered as a violation after both sides of the link are enabled for CLx.

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Actual Change

(a). Section 4.2.1.6.2 Entry to State, Page 118

From Text:

- Else, if the *CL0s Enable* bit is set to 1b in the Lane 0 Adapter of the Responding Port, a Lane Adapter shall respond to a request to enter a Low Power state with a CL0s_ACK Ordered Set. The first CL0s_ACK shall be sent within tCLxRequest after receiving the request. The CL0s_ACK Ordered Set shall be sent 16 -times.

- Else, a Lane Adapter shall respond to a request to enter a Low Power state with CL_NACK Ordered Sets. The CL_NACK Ordered Sets shall be sent 16 times. The Adapter shall resume regular CL0 operation in the transmit direction once it stops sending the CL_NACK Ordered Sets.

To Text:

- Else, if the *CL0s Enable* bit is set to 1b in the Lane 0 Adapter of the Responding Port, and the Responding Port can meet the timing of both *tCL0sEntry* (Equation 4-1) and *tCL0sExit* (Equation 4-3 or Equation 4-4) a Lane Adapter shall respond to a request to enter a Low Power state with a CL0s_ACK Ordered Set ~~in case it can meet the timing of both **Equation 4-1** and **Equation 4-4**~~. The first CL0s_ACK shall be sent within tCLxRequest after receiving the request. The CL0s_ACK Ordered Set shall be sent 16 times

- Else, a Lane Adapter shall respond to a request to enter a Low Power state with CL_NACK Ordered Sets within a time which is lesser than ($tCL0sEntry + tCL0sExit$). The CL_NACK Ordered Sets shall be sent 16 times. The Adapter shall resume regular CL0 operation in the transmit direction once it stops sending the CL_NACK Ordered Sets.

- After sending a CL_NACK Ordered Set, a port shall be able to meet *tCL0sEntry* and *tCL0sExit* requirements within tCLxSetup, and shall keep meeting these timing requirements for a duration of tCLxAccept

IMPLEMENTATION NOTE

There could be rare circumstances at which the Responding Port cannot guarantee CL0s resumption to CL0 within the expected time. In such cases the port may reject CLx entry request to avoid any timing sensitive application failure (such as PCIe LTR). Since subsequent attempts to enter CLx may be initiated by the remote port, the value of tCLxSetup is defined to limit the duration at which the Responding Port may reject such requests, thus ensuring CL0s entry is not being deferred indefinitely.

(b). Table 4-65. Logical Layer Timing Parameters , Page 160

To Text:

Parameter	Description	Min	Max	Units
tCLxSetup	The time required for a Responding Port to meet tCL0sEntry and tCL0sExit timing, after sending CL_NACK	--	200	us
tCLxAccept	The duration in which the Responding Port is required to meet tCL0sEntry and tCL0sExit timing	500	--	us