

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: DP Bandwidth Allocation
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:

Adds DisplayPort Bandwidth Allocation optional feature. It consists of new: <ul style="list-style-type: none">• DP IN Adapter registers.• DP IN Adapter functionality• CM functionality• Notification Packet

Benefits as a result of the changes:

Allows Display driver and Connection Manager to dynamically allocate and deallocate bandwidth. The allocation is done in finer granularity. This will lead to better user experience.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
--

None

An analysis of the hardware implications:
--

None

An analysis of the software implications:
--

None

An analysis of the compliance testing implications:
--

Tests need to be added

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Actual Change

(a). Table 10-12

Table 10-12. Aggregated DisplayPort Capabilities

DPCD Register (Address)	DPCD Field Name	DisplayPort Capability
MAX_LINK_RATE (00001h / 02201h / F0001h)	MAX_LINK_RATE	Minimum of downstream response and DP_COMMON_CAP.Maximal Link Rate.
MAX_LANE_COUNT (00002h / 02202h / F0004h)	MAX_LANE_COUNT	Minimum of downstream response and DP_COMMON_CAP.Maximal Lane Count. If MFDP Mode is set, then Maximum is 2.
<u>DP_TUNNELING_MAX_LINK_RATE</u> (E0028h)	<u>DP_Tunneling_Max_Link_Rate</u>	If DP BW Allocation Mode was enabled, set to Minimum of: <ul style="list-style-type: none"> • <u>Maximum of DPRX response for MAX_LINK_RATE</u> <li style="text-align: center;">And • <u>ADP_DP_CS_2.NRD_Maximal_Link_Rate.</u> Else set to 0h.
<u>DP_TUNNELING_MAX_LANE_COUNT</u> (E0029h)	<u>DP_Tunneling_Max_Lane_Count</u>	If DP BW Allocation Mode was enabled, set to Minimum of: <ul style="list-style-type: none"> • <u>Maximum of DPRX response for MAX_LANE_COUNT</u> <li style="text-align: center;">And • <u>ADP_DP_CS_2.NRD_Maximal_Lane_Count.</u> Else set to 0h.

(d1). Section 10.4.2.1 Setup



CONNECTION MANAGER NOTE

Before configuring a Path between DP IN and DP OUT Adapters, the Connection Manager shall perform the following steps:

1. **Available Bandwidth** – Editor’s Note: No change from USB4 spec
2. **Capabilities Exchange** – Editor’s Note: No change from USB4 spec
3. **DP BW Allocation Mode** – *If the Connection Manager supports DP BW Allocation Mode, it does the following:*
 - a. Checks if the DP IN Adapter supports DP BW Allocation Mode by reading DP_LOCAL_CAP.DP_IN_BW_Allocation_Mode_Support.
 - b. If the DP IN Adapter supports DP BW Allocation Mode, the Connection Manager does the following in the DP IN Adapter Configuration Space:
 - i. Sets ADP_DP_CS_2.CM_BW_Allocation_Mode_Support to 1b.

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- ii. If the Path being setup between the two Adapters travels through the same USB4 Links as another DP Path, then it sets ADP_DP_CS_2.Group_ID to a non-zero value for all the Paths which travel through the same USB4 Links, otherwise it sets ADP_DP_CS_2.Group_ID to 0h.
- iii. If the host system contains multiple Connection Managers, then it sets ADP_DP_CS_2.CM_ID to the Connection Manager index otherwise it sets it to 0h.
- iv. Sets ADP_DP_CS_2.NRD_Maximal_Link_Rate to the DP_LOCAL_CAP.Maximal_Link_Rate of the DP_IN Adapter or DP_OUT Adapter (whichever is lower).
- v. Sets ADP_DP_CS_2.NRD_Maximal_Lane_Count to the DP_LOCAL_CAP.Maximal_Lane_Count of the DP_IN Adapter or DP_OUT Adapter (whichever is lower).
- vi. Sets ADP_DP_CS_2.Estimated_BW according to Section 10.7.
- vii. Sets ADP_DP_CS_2.Granularity to any of the valid values.
- viii. Sets DP_STATUS.Allocated_BW to 0h.
- ix. Sets ADP_DP_CS_2.CM_Ack to 0b.

A Connection Manager shall configure the Output HopID to be 8 for the segment ...

(d2). Section 10.4.2.2 Tear-down



CONNECTION MANAGER NOTE

Before tearing down a Path between two DP Adapters, the Connection Manager needs to disable the DP Adapters on both ends of the Path by setting the ADP_DP_CS_0.VE (Video Enable) and ADP_DP_CS_0.AE (Aux Enable) bits to 0b in register of each DP Adapter. The Connection Manager needs to use single Write Request to set the VE and AE bits to 0b so that they both are written at the same time.

After tearing down a DP Path, the Connection Manager releases the DP stream resource, using a DEALLOCATE_DP_RESOURCE command as defined in Section 8.3.1.1.3, with a DisplayPort Number parameter equal to the DP IN Adapter number being released.

If only one DP IN Adapter remains in a Group_ID, a Connection Manager sets the DP IN Adapter Group_ID to 0h.

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(e). New section 10.7 DP BW Allocation Mode

Editor's Note:

Original Section 10.7 becomes 10.8.

10.7 DP BW Allocation Mode

A DP IN Adapter may optionally support DP BW Allocation Mode. If a DP IN Adapter supports DP BW Allocation Mode, it shall do so as defined in this section.

When DP BW Allocation Mode is enabled (see Section 10.7.1), the DPTX and the Connection Manager communicate through the DP IN Adapter. The interaction between a DP IN Adapter and a DPTX is described in Section 10.7.2. The interaction between a DP IN Adapter and a Connection Manager is described in Section 10.7.3.

10.7.1 DP BW Allocation Mode Enablement

If a DP IN Adapter supports DP BW Allocation Mode, it shall:

- Set DP_LOCAL_CAP.DP_IN_BW_Allocation_Mode_Support bit to 1b.
- Update the AUX Response for DPCD DP_TUNNELING and PANEL REPLAY OPTIMIZATION SUPPORT.DP_IN_BW_Allocation_Mode_Support (E000Dh, bit 7) to 1b.
- Update the AUX Response for DPCD USB4_DRIVER_BW_CAPABILITY.USB4_Driver_BW_Allocation_Mode_Support (E0020h, bit 7) to have the same value as ADP_DP_CS_2.CM_BW_Allocation_Mode_Support.

When a Connection Manager changes ADP_DP_CS_2.CM_BW_Allocation_Mode_Support bit, a DP IN Adapter shall:

- Set the BW_Allocation_Capability_Changed field to 1b in DP_TUNNELING_STATUS DPCD register.
- Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESI0 register at DPCD 02005h)
- If Unmask BW_Allocation_IRQ is 1b, generate an IRQ_HP.

DP BW Allocation Mode enablement is initiated by the DPTX only if both, the DP IN Adapter and the Connection Manager, support the DP BW Allocation Mode.

When DPTX sets

DPTX_BW_ALLOCATION_MODE_CONTROL.DP_Display_Driver_BW_Allocation_Mode_Enable (E0030h, bit 7) to 1b, a DP IN Adapter shall:

- Enable DP BW Allocation Mode
- Send the Connection Manager a Notification Packet with Event Code = DP_BW as defined in Table 6-11.

10.7.2 Interaction with DPTX

Table 10-X lists the fields in the DPCD registers that are used by DPTX to negotiate bandwidth allocation with a Connection Manager. Table 10-Y describes how a DP IN Adapter maps the DPCD fields to Adapter Configuration Space.

Table 10-X. DPCD Bandwidth Allocation Registers

<u>DPCD Register</u>	<u>Register Address</u>	<u>Bits</u>	<u>DPCD Field Type</u>	<u>DPCD Field Name</u>
<u>DP_TUNNELING_CAPABILITIES</u>	<u>E000Dh</u>	<u>[7]</u>	<u>Read Only</u>	<u>DP_IN_BW_Allocation_Mode_Support</u>
<u>USB4_DRIVER_ID</u>	<u>E000Fh</u>	<u>[3:0]</u>	<u>Read Only</u>	<u>USB4_Driver_ID</u>

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<u>DPCD Register</u>	<u>Register Address</u>	<u>Bits</u>	<u>DPCD Field Type</u>	<u>DPCD Field Name</u>
<u>USB4 DRIVER BW CAPABILITY</u>	<u>E0020h</u>	<u>[7]</u>	<u>Read Only</u>	<u>USB4_Driver_BW_Allocation_Mode_Support</u>
<u>DP_IN_ADAPTER_TUNNEL_INFORMATION</u>	<u>E0021h</u>	<u>[2:0]</u>	<u>Read Only</u>	<u>Group_ID</u>
<u>DP_BW_GRANULARITY</u>	<u>E0022h</u>	<u>[1:0]</u>	<u>Read Only</u>	<u>Granularity</u>
<u>ESTIMATED_BW</u>	<u>E0023h</u>	<u>[7:0]</u>	<u>Read Only</u>	<u>Estimated_BW</u>
<u>ALLOCATED_BW</u>	<u>E0024h</u>	<u>[7:0]</u>	<u>Read Only</u>	<u>Allocated_BW</u>
<u>DP_TUNNELING_STATUS</u>	<u>E0025h</u>	<u>[0]</u>	<u>Clearable, Read Only (Bit is cleared when 1 is written by way of an AUX_CH write transaction)</u>	<u>BW_Request_Failed</u>
		<u>[1]</u>		<u>BW_Request_Succeeded</u>
		<u>[2]</u>		<u>Estimated_BW_Changed</u>
		<u>[3]</u>		<u>BW_Allocation_Capability_Changed</u>
<u>DP_TUNNELING_MAX_LINK_RATE</u>	<u>E0028h</u>	<u>[7:0]</u>	<u>Read Only</u>	<u>DP_Tunneling_Max_Link_Rate</u>
<u>DP_TUNNELING_MAX_LANE_COUNT</u>	<u>E0029h</u>	<u>[7:0]</u>	<u>Read Only</u>	<u>DP_Tunneling_Max_Lane_Count</u>
<u>DPTX_BW_ALLOCATION_MODE_CONTROL</u>	<u>E0030h</u>	<u>[6]</u>	<u>Read/Write</u>	<u>Unmask_BW_Allocation_IRQ</u>
		<u>[7]</u>	<u>Read/Write</u>	<u>DP_Display_Driver_BW_Allocation_Mode_Enable</u>
<u>REQUESTED_BW</u>	<u>E0031h</u>	<u>[7:0]</u>	<u>Read/Write</u>	<u>Requested_BW</u>

Table 10-Y. DP IN Adapter Configuration Space Mapping

<u>DPCD Field Name</u>	<u>DPCD Field Type</u>	<u>DP IN Adapter Register</u>	<u>DP IN Field</u>
<u>USB4_Driver_BW_Allocation_Mode_Support</u>	<u>Read Only</u>	<u>ADP_DP_CS_2</u>	<u>CM_BW_Allocation_Mode_Support</u>
<u>USB4_Driver_ID</u>	<u>Read Only</u>	<u>ADP_DP_CS_2</u>	<u>CM_ID</u>
<u>Group_ID</u>	<u>Read Only</u>	<u>ADP_DP_CS_2</u>	<u>Group_ID</u>
<u>Granularity</u>	<u>Read Only</u>	<u>ADP_DP_CS_2</u>	<u>Granularity</u>
<u>Estimated_BW</u>	<u>Read Only</u>	<u>ADP_DP_CS_2</u>	<u>Estimated_BW</u>
<u>Allocated_BW</u>	<u>Read Only</u>	<u>DP_STATUS</u>	<u>Allocated_BW</u>
<u>DP_Display_Driver_BW_Allocation_Mode_Enable</u>	<u>Read/Write</u>	<u>ADP_DP_CS_8</u>	<u>DPTX_BW_Allocation_Mode_Enable</u>
<u>Requested_BW</u>	<u>Read/Write</u>	<u>ADP_DP_CS_8</u>	<u>Requested_BW</u>

When a DP IN Adapter receives a DPCD AUX Write transaction that targets a DPCD register within Table 10-Y, and the targeted DPCD field Type is Read/Write, it shall update the corresponding field in Adapter configuration space with the value of the write transaction.

When a DP IN Adapter receives a DPCD AUX Read transaction that targets a DPCD register within Table 10-Y, and the targeted DPCD field Type is Read Only, it shall update the read transaction with the value in the corresponding field in Adapter Configuration Space.

When DPTX sends a DPCD AUX write transaction that targets the *REQUESTED_BW* register, a DP IN Adapter shall:

- Store the current *Allocated_BW* in an internal variable.

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- If the recovery timer is advancing, stop and reset it.
- Initiate a bandwidth request handshake with the Connection Manager as defined in Section 10.7.3.

When a Connection Manager writes a value to the *Allocated BW* field that is equal to or greater than the *Requested BW*, a DP IN Adapter shall:

- Set the *BW Request Succeeded* field to 1b in DP_TUNNELING_STATUS DPCD register.
- Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESIO register at DPCD 02005h)
- If Unmask BW Allocation IRQ is 1b, generate an IRQ HPD.
- If the *ESTIMATED BW* field was locked for updates due to bandwidth request failure, unlock it.

When a Connection Manager writes a value to the *Allocated BW* field that is smaller than the *Requested BW*, a DP IN Adapter shall:

- Set the *ESTIMATED BW* field to the *Allocated BW*, and lock its value (i.e. ignore any changes in the *Estimated BW* field).
- Set the *BW Request Failed* to 1b in DP_TUNNELING_STATUS DPCD register.
- Set DP_TUNNELING_IRQ bit (Bit 5 of LINK_SERVICE_IRQ_VECTOR_ESIO register at DPCD 02005h)
- If Unmask BW Allocation IRQ is 1b, generate an IRQ HPD.
- Start the recovery timer.

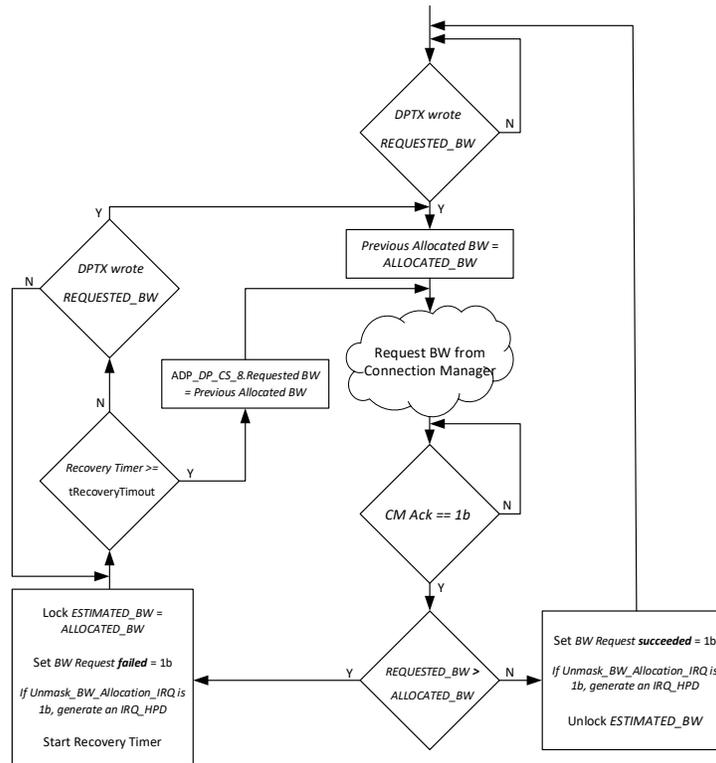
If the recovery timer has reached *tDPBWRecoveryTimeout*, the DP IN Adapter initiates a bandwidth allocation request. The DP BW that a DP IN Adapter requests shall be the same bandwidth as before the failed bandwidth allocation (i.e. the same value as in the *Allocated BW* field before the DPTX last updated the DPCD *Requested BW* register).

*Note: When a DPTX writes to the *REQUESTED BW* DPCD register, the DP IN Adapter should store the current *Allocated BW* in an internal variable. Then, in case of a *tDPBWRecoveryTimeout* timeout, the DP IN Adapter knows what *Requested BW* value to request.*

A DP IN Adapter interacts with DPTX according to Figure 10-X.

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Figure 10-X. DP IN Adapter Interaction with DPTX During DP BW Allocation



10.7.2.1 Estimated Bandwidth

Whenever the bandwidth allocation changes, the Connection Manager updates the available bandwidth by writing to ADP DP CS 2. *Estimated BW* field. Note that the *Estimated BW* field includes the bandwidth that is already allocated to the DP IN Adapter.

Upon a change in the *Estimated BW* field, a DP IN adapter shall:

- Set *Estimated BW Changed* bit in the DPCD DP TUNNELING STATUS register to 1b.
- Set DP TUNNELING IRQ bit (Bit 5 of LINK SERVICE IRQ VECTOR ES10 register at DPCD 02005h).
- If Unmask BW Allocation IRQ is 1b, generate an IRQ_HPD.



CONNECTION MANAGER NOTE

When there is a change in bandwidth across its Domain, the Connection Manager recalculates the estimated bandwidth for each DP IN Adapter in the Domain. The estimated bandwidth for a DP IN Adapter includes:

- *The bandwidth that has already been allocated to the DP IN Adapter.*
- *The available BW along the Path.*

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- Bandwidth that is allocated to the internal Host Controller, but not consumed
After the estimated bandwidth is recalculated, a Connection Manager updates the
ADP DP CS 2.Estimated BW field.

10.7.3 Interaction with the Connection Manager

When DPTX sends a DPCD AUX write transaction that targets the REQUESTED BW field, a DP IN Adapter shall:

1. Set the ADP DP CS 8.DPTX Req field to 1b.
2. Send the Connection Manager a Notification Packet with Event Code = DP BW as defined in Table 6-11.
3. Wait for the Connection Manager to set the ADP DP CS 2.CM Ack bit to 1b.
4. Set the ADP DP CS 8.DPTX Req field to 0b.



CONNECTION MANAGER NOTE

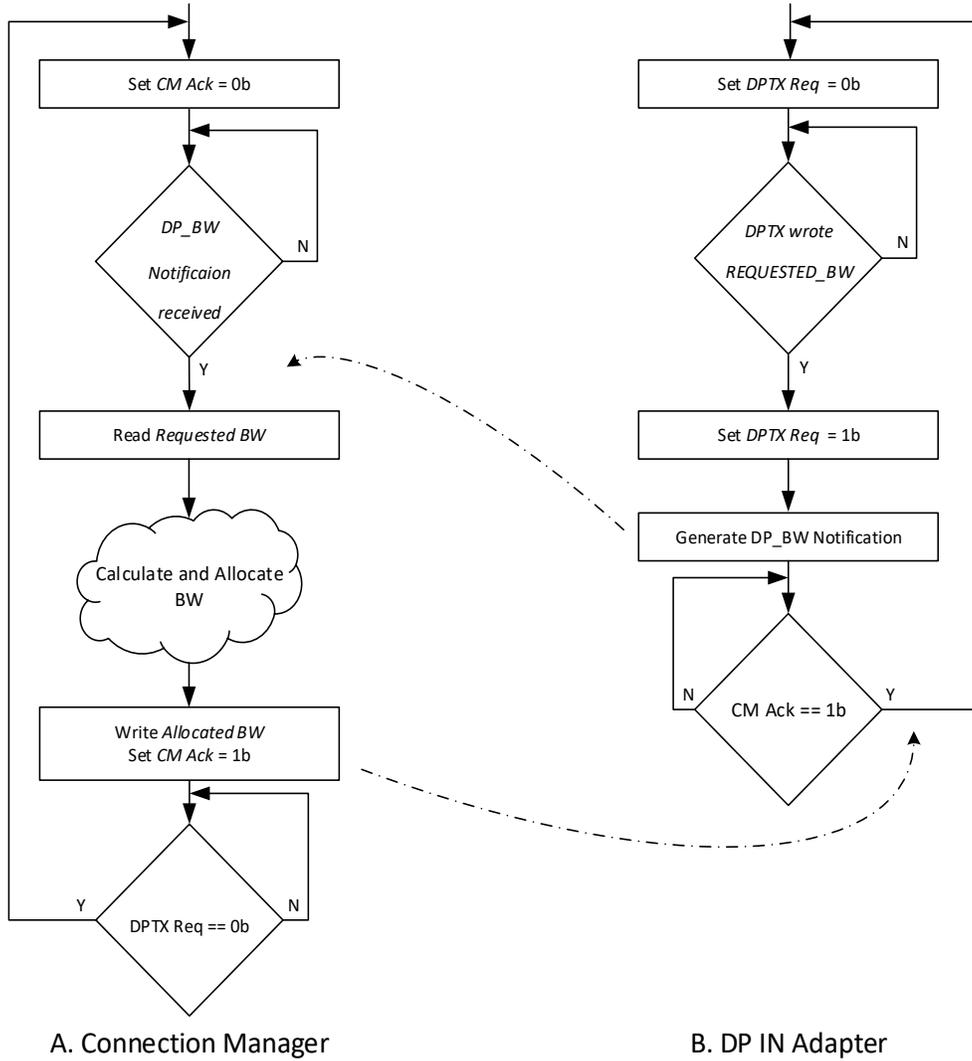
When a Connection Manager receives a DP BW Notification Packet, it completes the following steps within 100ms:

1. Reads ADP DP CS 8.Requested BW.
2. Allocates bandwidth:
 - a. If the Request bandwidth is less than or equal to the currently allocated bandwidth, then the new allocation will be equal to the new requested bandwidth.
 - If the DP IN Adapter has a Group ID different than zero, then for the following tDPBWRbalance, the Connection Manager will reserve the released bandwidth to be allocated to DP IN Adapters with the same Group ID.
 - b. Else, the Connection Manager tries to allocate bandwidth from the available bandwidth and by freeing bandwidth from other clients.
3. Writes the new allocated bandwidth to the DP STATUS.Allocated BW field.
4. Sets the ADP DP CS 2.CM Ack bit to 1b.
5. Waits for the DP IN Adapter to set the ADP DP CS 8.DPTX Req bit to 0b.
6. Sets the ADP DP CS 2.CM Ack bit to 0b.

A DP IN Adapter interacts with a Connection Manager according to Figure 10-X+1.

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Figure 10-X+1. DP BW Allocation Interaction with Connection Manager



(f). Section 6.5 Notification Events - Table 6-11

Table 6-11. Notification Events

Event Code	Reference	Initiator	Event Code	Adapter Num
Protocol Adapter Events				
<u>DP_BW</u>	<u>Section 10.7</u>	<u>Router</u>	<u>32</u>	<u>The DP IN Adapter.</u>

(g). Section 6.6 Notification Acknowledgement

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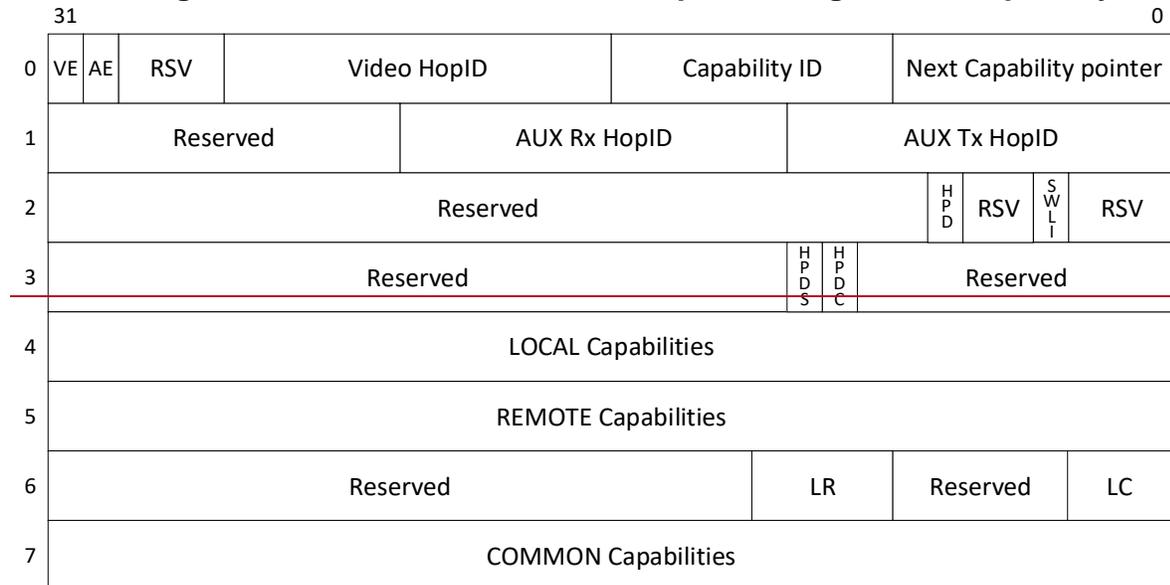
A Router expects a Notification Acknowledgment Packet from the Connection Manager in response to the following packets:

- A Notification Packet with Event Code = ERR_LINK.
- A Notification Packet with Event Code = ERR_HEC
- A Notification Packet with Event Code = ERR_FC
- A Notification Packet with Event Code = ERR_PLUG
- A Notification Packet with Event Code = DP_BW

(h). Section 8.2.2.6 DP Adapter Configuration Capability - Figure 8-12

Original Figure:

Figure 8-12. Structure of DP IN Adapter Configuration Capability



New Figure:

Figure 8-12. Structure of DP IN Adapter Configuration Capability

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31													0		
0	VE	AE	RSV	Video HopID				Capability ID				Next Capability pointer			
1	Reserved				AUX Rx HopID				AUX Tx HopID						
2	Estimated BW			RSV	CMMS	CM_ID	Group_ID	GR	CA	NRD MLR	HPD	RSV	SWLI	NRD MLC	
3	Reserved								HPDS	HPDC	Reserved				
4	LOCAL Capabilities														
5	REMOTE Capabilities														
6	Allocated BW			Reserved				LR	Reserved			LC			
7	COMMON Capabilities														
8	DR	DPE	Reserved								Requested BW				

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(i). Section 8.2.2.6 DP Adapter Configuration Capability - Table 8-15

Table 8-15. DP IN Adapter Configuration Capability Fields

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
2	ADP_DP_CS_2	2:0	Reserved NRD Max Lane Count (NRD MLC) <u>The Non-Reduced Max Lane Count is set by a Connection Manager to reflect the highest common Max Lane Count between the two DP Adapters, regardless of bandwidth availability.</u>	Rsvd R/W	0
		9:7	NRD Max Link Rate (NRD MLR) <u>The Non-Reduced Max Link Rate is set by a Connection Manager to reflect the highest common Max Link Rate between the two DP Adapters, regardless of bandwidth availability.</u>	R/W	0
		10	CM Ack (CA) <u>A Connection Manger sets this field to 1b to indicate that it completed the bandwidth allocation process. A Connection Manager sets this bit to 0b after the DP IN Adapter sets DPTX Req field to 0b</u>	R/W	0
		12:11	Granularity (GR) <u>A Connection Manager sets this field to indicate the bandwidth granularity for the Requested BW, Allocated BW and Estimated BW:</u> 0: 0.25 1: 0.5 2: 1.0 3: Reserved <u>The units are in Gbps.</u>	R/W	0
		15:13	Group ID <u>A Connection Manager uses this field to indicate the group this Path is associated with:</u> 0h – The Path is not associated to any group. 1-7h – The group number the Path is associated with.	R/W	0
		19:16	Reserved CM ID <u>A Connection Manager uses this field to indicate its own index, in case there are multiple CMs in the Host system</u>	R/W	0
		20	CM BW Allocation Mode Support (CMMS) 0: Not supported 1: Supported	R/W	<u>Vendor Defined</u>
		23:21	Reserved	Rsvd Z	0
		31:7:24	Reserved Estimated BW <u>A Connection Manager uses this field to indicate the estimated available bandwidth for the DP IN Adapter.</u>	Rsvd ZR/W	0
4	DP_LOCAL_CAP	28	Reserved DP IN BW Allocation Mode Support 0: Not supported 1: Supported	Rsvd	0 <u>Vendor Defined</u>
<u>DP_STATUS register is Lane Count and Link Rate fields are only valid after the DP Link is established.</u>					
6	DP_STATUS	31:23 1:7	Reserved	Rsvd Z	0

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		31:24	Allocated BW <u>A Connection Manager uses this field to indicate the allocated bandwidth for the DP IN Adapter.</u>	R/W	0
<u>A Connection Manager does not address this register if the DP IN Adapter does not support the DP BW Allocation Mode (i.e. DP_LOCAL_CAP.DPIN BW Allocation Mode Support = 1b)</u>					
8	ADP_DP_CS_8	7:0	Requested BW <u>A DP IN Adapter uses this field to reflect the requested bandwidth by the DPTX to the Connection Manager.</u>	RO	0
		29:8	Reserved	RO	0
		30	DPTX BW Allocation Mode Enable (DPME) 0: Disabled (default) 1: Enabled	RO	0
		31	DPTX Req(DR) <u>A DP IN Adapter sets this field to 1b when DPTX writes to the REQUESTED_BW register.</u> <u>A DP IN Adapter sets this field to 0b after the Connection Manager sets the CM Ack bit to 1b.</u>	RO	0

(j). Table 10-20

Add a line at the end of the table.

Table 10-20. DP Adapter Timing Parameters

Parameter	Description	Value	Units
<u>tDPBWRcoveryTimeout</u>	<u>The time that a DP IN Adapter waits for DPTX to request bandwidth in case of an allocation failure.</u>	10	Seconds
<u>tDPBWRebalance</u>	<u>The time a Connection Manager reserves released bandwidth to be used by other DP IN Adapters with the same Group_ID</u>	10	Seconds

(k). Table 10-9. DPCD Internal Addresses

Table 10-9. DPCD Internal Addresses

Functionality	Address	Name
<u>DP Tunneling over USB4 FieldTunneling-Device-Specific-Fields</u>	E0000h – E0FFh	<u>DP Tunneling over USB4™ FieldTunneling-Device-Specific Fields</u>

(l). Section 10.4.4.6 DPCD DP Tunneling over USB4 Tunneling Device-Specific-Field

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10.4.4.6 DPCD DP Tunneling over USB4 Tunneling Device Specific Field

When a DP IN Adapter receives an AUX Request targeting the DP Tunneling over USB4 Tunneling Device Specific Field DPCDs, it shall respond with its internal data.

A DP IN Adapter shall set the *DP Tunneling Support* bit to 1b in the DP TUNNELING CAPABILITIES DPCD (Address E000Dh bit offset 0).