# USB4 1.0 ENGINEERING CHANGE NOTICE FORM

## Title: Update TBT3 Support of L1 and L2
## Applied to: USB4 Specification Version 1.0

| **Brief description of the functional changes:** |
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| Clarifies the support of TBT3 devices in L1 and L2 over the PCIe tunnel. SW L1 always supported while in some cases ASPM L1 are not supported. The handshake timeouts were corrected according to current ecosystem. |

| **Benefits as a result of the changes:** |
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| Spec is aligned to current Ecosystem. |

| **An assessment of the impact to the existing revision and systems that currently conform to the USB specification:** |
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| None |

| **An analysis of the hardware implications:** |
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| Implement the Operation |

| **An analysis of the software implications:** |
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| None |

| **An analysis of the compliance testing implications:** |
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| None |

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## Actual Change

### (a). Section 13.7.1 PCIe Power Management

#### 13.7.1.1 L1

If TBT3 Mode is established on a link and the *USB4 Sideband Channel Support* bit at the Link Partner is set to 0b, then ASPM L1 operation over PCIe Tunneling is not supported. When ASPM L1 operation is not supported:

- If TBT3 Mode is established on a Downstream Facing Port, the state of the downstream port of the internal PCIe Switch that is connected to that Downstream Facing Port may be ignored when determining the conditions to enter L1 state on the upstream port of the internal PCIe Switch.
- If TBT3 Mode is established on the Upstream Facing Port, the upstream port of the internal PCIe Switch that is connected to that Upstream Facing Port shall disable L1.

If TBT3 Mode is established on a link and the *USB4 Sideband Channel Support* bit at the Link Partner is set to 1b, then ASPM L1 operation over PCIe Tunneling is supported.

*Note: SW L1 is always supported.*

*Note: The internal upstream PCIe port of a TBT3 device, implements an L1 handshake timeout of 10us for ASPM L1 and 2us for SW L1, starting from sending EIOS and ending when an EIOS is received. If timeout expires, the internal upstream PCIe port enters Recovery state.*

#### 13.7.1.2 L2

*Note: The internal upstream PCIe port of a TBT3 device implements an L2 handshake timeout of ~~4us~~2us, starting from sending EIOS and ending when an EIOS is received. If timeout expires, the internal upstream PCIe port enters either to Detect or Recovery state~~s~~.*