USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: PCIe Logical Idle
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:

Requires that Idle data Symbols are not tunneled.
Clarifies the internal PCIe port behavior around Recovery.Idle state.

Benefits as a result of the changes:

More accurate spec

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

None

An analysis of the hardware implications:

None

An analysis of the software implications:

None

An analysis of the compliance testing implications:

None

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Actual Change

(a). Section 11.1.1

The PCIe Adapter Layer shall encapsulate the following PCIe constructs in Tunneled Packets:

- Transaction Layer Packets (TLP).
- Data Link Layer Packets (DLLP).
- Ordered Sets.
- Out-of-band events.

A PCIe Adapter Layer shall not encapsulate Idle data Symbols into Tunneled Packets.

(b). Section 11.2.1.2

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The following changes shall also apply to the LTSSM:

- o A PCIe Upstream port in Recovery.idle shall transition to L0 state when it receives a TLP or DLLP. If the port does not receive any TLP or DLLP, it shall transition to the L0 state tRecovery time after it entered the Recovery.idle state. ~~A PCIe upstream port in Recovery.idle shall wait tRecovery before transitioning to the L0 state.~~
  - ▪ Note: The tRecovery wait period is needed to detect a possible transition to Disabled state or to Hot Reset State.

~~Before transitioning to the L0 state, a PCIe Adapter Layer that receives a TLP or DLLP shall:~~

- ~~Terminate the timer.~~
- ~~Generate logical idle.~~
- ~~Pass the TLP or DLLP to the Internal PCIe Port.~~

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📬 **IMPLEMENTATION NOTE**

Idle data Symbols are not sent over the USB4 Fabric. Therefore, a receiving internal PCIe port ~~Adapter~~ cannot depend on the reception of Idle data Symbols in its LTSSM. One possible implementation is that the PCIe Adapter Layer generates the Idle data Symbols towards the internal PCIe port before transitioning to L0 state. Another ~~A~~ possible implementation ~~would be~~is for the LTSSM to proceed from either Configuration.Idle state or Recovery.Idle state to ~~an~~ L0 state without reception of any Idle data Symbols. Note that TS2 Ordered Sets received after the transition to L0 state are ignored until a Tunneled Packet ~~is received that is not a~~ containing a construct other that a TS2 Ordered Set is received.

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(C). Table 11-6

Table 11-6 PCIe Adapter Timing Parameters

Parameter	Description	Min	Max	Units
tRecovery	Time in the Recovery.Idle state before transitioning to L0 state, in the absence of DLLP or TLP. Applicable only for a PCIe upstream port.	200	–	µs