USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: Byte Order in Host Memory Descriptors and Data Buffers
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:
New information about order of bytes in Descriptor Rings in host memory.

Benefits as a result of the changes:
Guidance to Connection Manager and system designer.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
None. Complies with existing PCIe-based systems.

An analysis of the hardware implications:
Mapping of descriptors and data buffers shall comply with the ECR.

An analysis of the software implications:
A Connection Manager shall post descriptors and data buffers in host memory in the order defined in the ECR. A Connection Manager shall read descriptors and data buffers in host memory in the order defined in the ECR.

An analysis of the compliance testing implications:
A Compliance Connection Manager shall verify the byte order within descriptors and data buffers.

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Actual Change

(a). Section 12.1.1 DW, Byte, and Bit Order

From Text:

A PCIe Host Interface Adapter Layer shall map the payload of a PCIe TLP into a Transmit Descriptor, a Receive Descriptor, or a Transport Layer Packet payload in the following manner:

- For a Transport Layer Packet: Data Byte 0 in the PCIe TLP payload, shall be mapped to bits [31:24] of the first payload DW depicted in Figure 5-1. Data Byte 1 in the PCIe TLP payload, shall be mapped to bits [23:16] of the first payload DW depicted in Figure 5-1, and so on.
- For a Transmit Descriptor: Data Byte 0 in the PCIe TLP payload shall be mapped to bits [7:0] of the first DW of the Transmit Descriptor depicted in Figure 12-4. Data Byte 1 in the PCIe TLP payload shall be mapped to bits [15:8] of the first DW of the Transmit Descriptor depicted in Figure 12-4.
- For a Receive Descriptor: Data Byte 0 in the PCIe TLP payload shall be mapped to bits [7:0] of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6. Data Byte 1 in the PCIe TLP payload shall be mapped to bits [15:8] of the first DW of the first DW of the Receive Descriptor depicted in Figure12-5 and Figure 12-6, and so on.
- Within each byte, bit[i] in the PCIe TLP payload shall be mapped to bit[i] in the corresponding byte of the Transmit Descriptor, Receive Descriptor, or Transport Layer Packet payload.

To Text:

Data Buffers , Transmit Descriptors, and Receive Descriptors shall be stored in host memory in the following manner:

- For a Data Buffer: the lowest-addressed byte of data shall be mapped to bits [31:24] of the first payload DW depicted in Figure 5-1. The following addressed byte shall be mapped to bits [23:16] of the first payload DW depicted in Figure 5-1, and so on.
- For a Transmit Descriptor: the lowest-addressed byte of descriptor data in memory shall be mapped to bits [7:0] of the first DW of the Transmit Descriptor depicted in Figure 12-4. The following addressed byte shall be mapped to bits [15:8] of the first DW of the Transmit Descriptor depicted in Figure 12-4, and so on.
- For a Receive Descriptor: the lowest-addressed byte of descriptor data in memory shall be mapped to bits [7:0] of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6. The following addressed byte shall be mapped to bits [15:8] of the first DW of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6, and so on.
- Within each byte, bit[i] in host memory shall be mapped to bit[i] in the corresponding byte of the Data Buffer, Transmit Descriptor, or Receive Descriptor.

A PCIe Host Interface Adapter Layer shall map the payload of a PCIe TLP into a Transport Layer Packet payload , Transmit Descriptor, or a Receive Descriptor~~, or a Transport Layer Packet payload~~ in the following manner:

- For a Transport Layer Packet: Data Byte 0 in the PCIe TLP payload, shall be mapped to bits [31:24] of the first payload DW depicted in Figure 5-1. Data Byte 1 in the PCIe TLP payload, shall be mapped to bits [23:16] of the first payload DW depicted in Figure 5-1, and so on.

- For a Transmit Descriptor: Data Byte 0 in the PCIe TLP payload shall be mapped to bits [7:0] of the first DW of the Transmit Descriptor depicted in Figure 12-4. Data Byte 1 in the PCIe TLP payload shall be mapped to bits [15:8] of the first DW of the Transmit Descriptor depicted in Figure 12-4, and so on.
- For a Receive Descriptor: Data Byte 0 in the PCIe TLP payload shall be mapped to bits [7:0] of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6. Data Byte 1 in the PCIe TLP payload shall be mapped to bits [15:8] of the first DW of the first DW of the Receive Descriptor depicted in Figure 12-5 and Figure 12-6, and so on.
- Within each byte, bit[i] in the PCIe TLP payload shall be mapped to bit[i] in the corresponding byte of the Transmit Descriptor, Receive Descriptor, or Transport Layer Packet payload.