USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: Self-Clear Bits
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:
A more precise definition of the self-clear bits.

Benefits as a result of the changes:
A more precise definition how SW accesses self-clear bits.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
none

An analysis of the hardware implications:
Self-clear bits shall be read by SW as defined in this ECR

An analysis of the software implications:
SW shall not rely on reading the self-clear bits prior to completion of an action.

An analysis of the compliance testing implications:
None

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Actual Change

(a). Table 8-1. Configuration Register Fields Access Types

From Text:

Access Type	Description
R/W SC	**Read/Write Self Clearing**. When set to 1b a field with this access type causes an action to be initiated. Once the action is complete, the field shall return to 0b. Unless specified otherwise, a field with this attribute shall always read as 0b.

To Text:

Access Type	Description
R/W SC	**Read/Write Self Clearing**. When set to 1b a field with this access type causes an action to be initiated. ~~Once the action is complete, the field shall return to 0b. Unless specified otherwise, a field with this attribute shall always read as 0b.~~ A field with this attribute shall read as 0b after the action is complete. The value returned prior to completion of the action is vendor defined.

(b). Table 12-9. Access Types

From Text:

Access Type	Description
R/W SC	**Read/Write Self Clearing**. When set to 1b a field with this access type causes an action to be initiated. Once the action is complete, the field shall return to 0b. Unless specified otherwise, a field with this attribute shall always read as 0b.

To Text:

Access Type	Description
R/W SC	**Read/Write Self Clearing**. When set to 1b a field with this access type causes an action to be initiated. ~~Once the action is complete, the field shall return to 0b. Unless specified otherwise, a field with this attribute shall always read as 0b.~~ A field with this attribute shall read as 0b after the action is complete. The value returned prior to completion of the action is vendor defined.
WO	**Write Only.** A field with this access type shall be capable of write operations. Reading the field returns a vendor-defined value.

(c). Table 8-12. Contents of the Lane Adapter Configuration Capability

From Text:

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	LANE_ADP_CS_1	15	**Lane Bonding (LB)** A Connection Manager sets this bit to 1b in either Adapter of a USB4 Port to transition the Adapters to the Lane Bonding state. Writing 0b to this bit shall have no effect. A Router shall clear this bit to 0b immediately after it is set to 1b. If the Adapter is already in the Lane Bonding state when this bit is set to 1b, the Adapter may reenter the Lane Bonding state after Lane Bonding is complete but is not required to do so.	R/W SC	0

To Text:

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	LANE_ADP_CS_1	15	**Lane Bonding (LB)** A Connection Manager sets this bit to 1b in either Adapter of a USB4 Port to transition the Adapters to the Lane Bonding state. Writing 0b to this bit shall have no effect. ~~A Router shall clear this bit to 0b immediately after it is set to 1b.~~ If the Adapter is already in the Lane Bonding state when this bit is set to 1b, the Adapter may reenter the Lane Bonding state after Lane Bonding is complete but is not required to do so.	R/W SC	0

(d). Table 12-12. Host Interface Reset Register

From Text:

Bit(s)	Field Name and Description	Type	Default Value
0	**RST** When set to 1b, shall reset the Host Interface registers and the E2E flow control counters to their default values. The Host Interface Adapter Layer shall set this bit to 0b once it completes the reset.	R/W SC	0b
31:1	**Reserved**	Rsvd	0

To Text:

Bit(s)	Field Name and Description	Type	Default Value
0	**RST** When set to 1b, shall reset the Host Interface registers and the E2E flow control counters to their default values. ~~The Host Interface Adapter Layer shall set this bit to 0b once it completes the reset~~. The Host Interface Adapter Layer shall complete the reset within tHIReset time.	R/W SC	0b
31:1	**Reserved**	Rsvd	0

(e). Table 12-37. Host Interface Timing Parameters

From Text:

Parameter	Description	Min	Max	Units
tE2ERate	The time interval between periodic E2E Credit Grant Packets.	1	1000	ms
tE2ESync	The time interval between E2E Credit Sync Packets.	10	20	sec

To Text:

Parameter	Description	Min	Max	Units
tE2ERate	The time interval between periodic E2E Credit Grant Packets.	1	1000	ms
tE2ESync	The time interval between E2E Credit Sync Packets.	10	20	Sec
tHIReset	Time to complete a Host Interface Reset	-	10	ms

(f). Table 12-28. Interrupt Status Clear

From Text:

Bit(s)	Field Name and Description	Type	Default Value
31:0	**Interrupt Status Clear bits** When a bit is set to 1b, the corresponding bit in the Interrupt Status Registers is set to 0b. Writing 0b to a bit in this register has no effect. Reading this register returns a vendor defined value.	R/W SC	Vendor Defined

To Text:

Bit(s)	Field Name and Description	Type	Default Value
31:0	**Interrupt Status Clear bits** When a bit is set to 1b, the corresponding bit in the Interrupt Status Registers is set to 0b. Writing 0b to a bit in this register has no effect. ~~Reading this register returns a vendor defined value.~~	~~R/W SC~~ WO	Vendor Defined

(g). Table 12-29. Interrupt Status Set

From Text:

Bit(s)	Field Name and Description	Type	Default Value
31:0	**Interrupt Status Set bits** When a bit is set to 1b, the corresponding bit in the Interrupt Status Registers is set to 1b. Writing 0b to a bit in this register has no effect. Reading this register returns a vendor defined value.	R/W SC	Vendor Defined

To Text:

Bit(s)	Field Name and Description	Type	Default Value
31:0	**Interrupt Status Set bits** When a bit is set to 1b, the corresponding bit in the Interrupt Status Registers is set to 1b. Writing 0b to a bit in this register has no effect. ~~Reading this register returns a vendor defined value.~~	~~R/W SC~~ WO	Vendor Defined

(h). Table 12-31. Interrupt Mask Clear

From Text:

Bit(s)	Field Name and Description	Type	Default Value
31:0	**Interrupt Mask Clear bits** Writing 1b to a bit in this register sets the corresponding bit in the Interrupt Mask Registers to 0b. Writing 0b to a bit in this register does not have any effect. Reading this register returns a vendor defined value.	R/W SC	Vendor Defined

To Text:

Bit(s)	Field Name and Description	Type	Default Value
31:0	**Interrupt Mask Clear bits** Writing 1b to a bit in this register sets the corresponding bit in the Interrupt Mask Registers to 0b. Writing 0b to a bit in this register does not have any effect. ~~Reading this register returns a vendor defined value.~~	~~R/W SC~~ WO	Vendor Defined

(j). Table 12-32. Interrupt Mask Set

From Text:

Bit(s)	Field Name and Description	Type	Default Value
31:0	**Interrupt Mask Set bits** Writing 1b to a bit in this register sets the corresponding bit in the Interrupt Mask Registers to 1b. Writing 0b to a bit in this register does not have any effect. Reading this register returns a vendor defined value.	R/W SC	Vendor Defined

To Text:

Bit(s)	Field Name and Description	Type	Default Value
31:0	**Interrupt Mask Set bits** Writing 1b to a bit in this register sets the corresponding bit in the Interrupt Mask Registers to 1b. Writing 0b to a bit in this register does not have any effect. ~~Reading this register returns a vendor defined value.~~	~~R/W SC~~ WO	Vendor Defined