USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: Re-timer Clock Switching Refinements
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:
Limits the Router Assembly's transmitter maximum transient frequency during training to 1400ppm, and the corresponding receiver incoming signal maximum frequency to 1600ppm (referenced to the baseline frequency of the link - 10.0G in Gen2, 20.0G in Gen3). The added budget on the receiver side is required for supporting active re-timing cables between the two ends, which might add intrinsic frequency variations on top of the input-to-output forwarding.

Benefits as a result of the changes:
Further constrains the Router Assembly transmitter frequency variation during Re-timer clock switching by defining maximum allowed frequency on top of the existing df/dt specification, and in parallel, ensures that the far-end receiver tracks appropriately the worst-case incoming signal.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
Impact expected to be minor (if at all).

An analysis of the hardware implications:
The Re-timer TXPLL clock switching from local clock to the recovered clock will need to be done more carefully and accurately in order to avoid large frequency overshoot.

An analysis of the software implications:
NA

An analysis of the compliance testing implications:
The transmitter maximum frequency will need to be monitored as part of the transmitter clock switching testing The receiver clock-switching test setup will need to be updated with the worst-case transmitter characteristics.

Actual Change

(a). Section 3.4.1.1.2

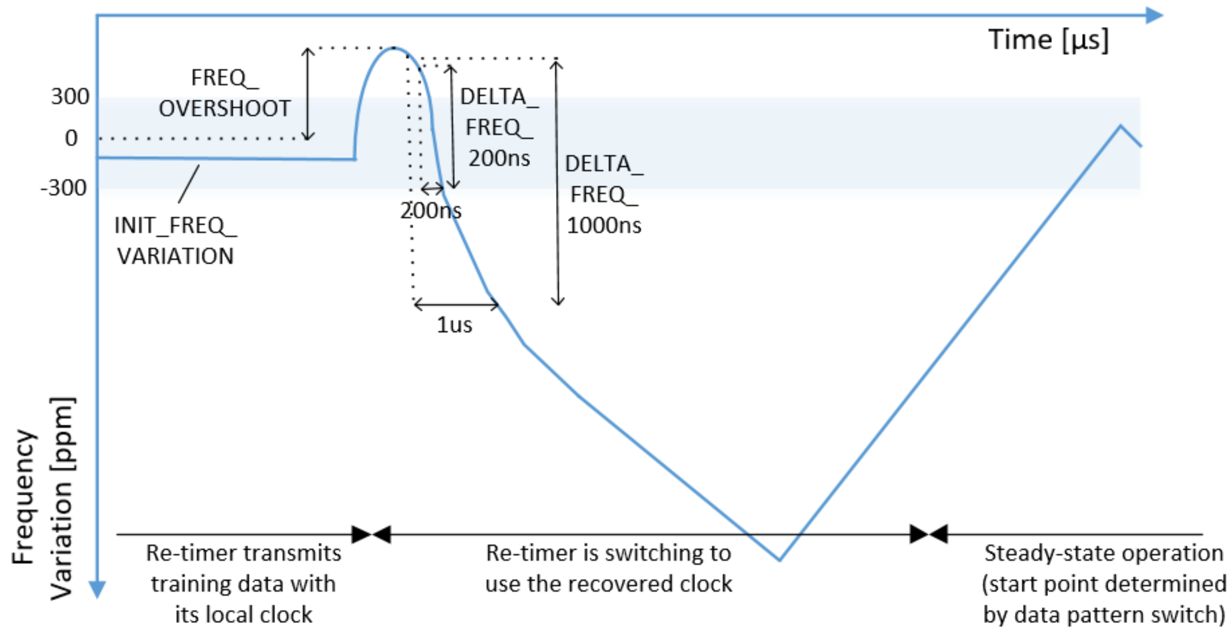
Table 3-4. Transmitter Frequency Variation Limits During Link Training Before Obtaining Steady-State

Symbol	Description	Min	Max	Units	Conditions
INIT_FREQ_VARIATION	~~i~~Initial non-modulated transmit frequency applied while sending CL_WAKE1.x pattern	-300	300	ppm	See Notes 1, 2~~.~~
DELTA_FREQ_200ns	Frequency variation during Link training over 200ns measurement windows	--	1400	ppm	See Note 1~~.~~
DELTA_FREQ_1000ns	Frequency variation during Link training over 1μs measurement windows	--	2200	ppm	See Note 1~~.~~
FREQ_OVERSHOOT	Maximum transient frequency offset from the Link baseline rate, including the clock source accuracy, dynamic clock switching effects and frequency variations induced by low frequency jitter		1400	ppm	See Note 1

Notes:

1. Measurement shall be performed over the transmitted signal. The signal phase shall be extracted while applying a 2nd order low-pass filter with 3dB point at 5MHz.
2. ~~1.~~ INIT_FREQ_VARIATION corresponds to the transmitter average frequency offset from the Link baseline rate (10.0 Gbps in Gen 2, 20.0 Gbps in Gen3), without including low frequency jitter variations, which shall be filtered out by averaging the extracted frequency variation waveform over a window of at least 30μs.

Figure 3-8. Router Assembly Transmitter Frequency Variation During Training



(b). Section 3.5.1

Table 3-10. Common Receiver Specifications at TP3'

Symbol	Parameters	Min	Max	Units	Comments
RL_DIFF	Differential Return Loss, 0.05 – 12GHz		See Section 3.5.1.1	dB	
RL_COMM	Common Mode Return Loss, 0.05 – 12GHz		See Section 3.5.1.2	dB	
LANE_TO_LANE_SKEW	Skew between dual incoming signals of the same USB4 Port		44	ns	See Note 1.
~~SIGNAL_FREQ_VARIATIONS_TRAINING~~	~~Frequency variations of the incoming signal during Link training, before obtaining steady-state~~		~~See Section 3.4.1.1~~	~~ppm~~	~~See Note 2.~~
RX_INIT_FREQ_VARIATION	Initial non-modulated signal frequency applied during training before obtaining steady-state operation	-300	300	ppm	See Notes 2, 3, 4
RX_DELTA_FREQ_200ns	Incoming signal's frequency variation during Link training over 200ns measurement windows		1400	ppm	See Notes 2, 3
RX_DELTA_FREQ_1000ns	Incoming signal's frequency variation during Link training over 1µs measurement windows		2200	ppm	See Notes 2, 3

RX_FREQ_OVERSHOOT	Incoming signal's maximum frequency offset from the Link baseline rate during training		1600	ppm	See Notes 2, 3

Notes:

1. LANE_TO_LANE_SKEW specifies the maximum skew at the connector. On top of the skew measured at TP3', the following informative budget is assumed between the connector and the Router RX IC: each Re-timer input-to-output skew: 8ns, physical media mismatches: 2 ns.
2. The clocking configuration during the different stages of the Link initialization is described in Section 3.4.1.1 and Figure 3-8.~~Steady-state clocking is applied from the point that SLOS training pattern is received.~~
3. Extracted while applying a 2nd order low-pass filter with 3dB point at 5MHz over the signal phase.
4. ~~2.~~4. RX_INIT_FREQ_VARIATION corresponds to the incoming nominal frequency offset from the Link baseline rate (10.0 Gbps in Gen 2, 20.0 Gbps in Gen3), without including low frequency jitter induced variations.

(c). Section 3.6.3.1

Table 3-17. Common Receiver Specifications at TP2

Symbol	Description	Min	Max	Units	Comments
RL_DIFF	Differential Return Loss, 0.05-12GHz	--	See Section 3.6.3.2	dB	
RL_COMM	Common Mode Return Loss, 0.05-12GHz	--	See Section 3.6.3.3	dB	
LANE_TO_LANE_SKEW	Skew between dual incoming signals of the same USB4 Port	--	26	ns	See Note 1.
~~SIGNAL_FREQ_VARIATIONS_TRAINING~~	~~Frequency variations of the incoming signal during Link training, before obtaining steady-state~~	~~--~~	~~See Section 3.4.1.1~~	~~ppm~~	~~See Note 2.~~
RX_INIT_FREQ_VARIATION	Initial non-modulated signal frequency applied during training before obtaining steady-state operation	-300	300	ppm	See Notes 2, 3, 4
RX_DELTA_FREQ_200ns	Incoming signal's frequency variation during Link training over 200ns measurement windows		1400	ppm	See Notes 2, 3
RX_DELTA_FREQ_1000ns	Incoming signal's frequency variation during Link training over 1µs measurement windows		2200	ppm	See Notes 2, 3
RX_FREQ_OVERSHOOT	Incoming signal's maximum frequency offset from the Link baseline rate during training		1400	ppm	See Notes 2, 3

Notes:

1. LANE_TO_LANE_SKEW specifies the maximum skew at the connector. On top of the skew measured at TP2, the following informative budget is assumed between the connector and the Router RX IC: each Re-timer input-to-output skew: 8ns, physical media mismatches: 4 ns.
2. The clocking configuration during the different stages of the Link initialization is described in Section 3.4.1.1 and Figure 3-8.~~Steady-state clocking is applied from the point that SLOS training pattern is received.~~
3. Extracted while applying a 2nd order low-pass filter with 3dB point at 5MHz over the signal phase.
4. ~~2.~~4. RX_INIT_FREQ_VARIATION corresponds to the incoming nominal frequency offset from the Link baseline rate (10.0 Gbps in Gen 2, 20.0 Gbps in Gen3), without including low frequency jitter induced variations.