USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: DP Link Training Failure
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:
1. Add descriptive bits to the STATUS_TRAINING_FAIL SET CONFIG Packet which elaborates the cause of the failure. 2. A DP OUT Adapter sends the new information. 3. A DP IN Adapter uses the new information to reflect the failure cause to the DPTX.

Benefits as a result of the changes:
Enables the DPTX to use it's intended fallback mechanism according to the nature of the failure. Enables to close a gap for a link failure CTS test in VESA

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
None

An analysis of the hardware implications:
None

An analysis of the software implications:
None

An analysis of the compliance testing implications:
None

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Actual Change

(a). Table 10-6 SET_CONFIG Message

Table 10-6. SET_CONFIG Message

MSG Type	Type Value	Direction	MSG Data	Reference
SET_LINK	0x01	Both	[0] – DP Link Training Mode 0b: Autonomous, concurrent (applicable to Non-LTTPR and LTTPR Transparent) 1b: DPTX-managed, sequential (applicable to LTTPR Non-Transparent) [7:1] – Reserved	Section 10.4.10 Section 10.4.12
STATUS_TRAINING_ FAIL	0x02	OUT to IN	[0] – LANE0_CHANNEL_EQ_DONE [1] – LANE0_SYMBOL_LOCKED [2] – LANE1_CHANNEL_EQ_DONE [3] – LANE1_SYMBOL_LOCKED [4] – LANE2_CHANNEL_EQ_DONE [5] – LANE2_SYMBOL_LOCKED [6] – LANE3_CHANNEL_EQ_DONE [7] – LANE3_SYMBOL_LOCKED [7:0] – Reserved	Section 10.4.10.2

10.4.10.2 Non-LTTPR and LTTPR Transparent

When a DPTX performs link training, it trains the DP IN Adapter receiver - it is unaware of the second DisplayPort link being trained by the DP OUT Adapter. The two DisplayPort links are trained simultaneously. The DP IN Adapter aggregates the status from each link when responding to the DPTX.

A DP Adapter shall perform DisplayPort link training according to the DisplayPort 1.4a Specification with the modifications and requirements defined in Section 10.4.10.2.1 and Section 10.4.10.1.210.4.10.2.2

10.4.10.2.1 DP IN Adapter Requirements

A DP IN Adapter shall send a SET_CONFIG Packet of type SET_LINK after DPTX writes TPS1 to the DP RX TRAINING_PATTERN_SET DPCD register. The SET_CONFIG packet shall have the following values:

- LC = LANE_COUNT_SET value written by DPTX.
- LR = LINK_BW_SET value written by the DPTX.
- TPS = Reflects TPS3 and TPS4 support as indicated in the DP_COMMON_CAP register.
- MSG Data = 0b, representing *DP Link Training Mode* = Non-LTTPR and LTTPR Transparent modes.

A DP IN Adapter shall respond to a status read of LANEx_CR_DONE as follows:

- If a SET_CONFIG Packet of type STATUS_CR_DONE was not received since link training started, set the LANEx_CR_DONE bits to 0b.

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- If a SET_CONFIG Packet of type STATUS_CR_DONE was received since link training started, set the LANEx_CR_DONE bits to be the internal DP IN Adapter status for a lane ANDed with the relevant bit present in the last received SET_CONFIG MSG Data.

A DP IN Adapter shall respond to a DPTX that link training has ended successfully only when all the following are true:

- The DP IN Adapter internal status indicates link training has ended successfully.

- The DP IN Adapter received a SET_CONFIG Packet of type SET_LINK, carrying the same *LC* and *LR* fields that it sent to the DP OUT Adapter when link training was initiated.

- The DP IN Adapter sent at least nine DP Clock Sync Packets after it received a SET_CONFIG Packet of type STATUS_CR_DONE.

While the conditions (as defined in this section) for successful link training are not met, a DP IN Adapter shall respond to a status read of INTERLANE_ALIGN_DONE, LANEx_CHANNEL_EQ_DONE and LANEx_SYMBOL_LOCKED as follows:

- If a SET_CONFIG Packet of type STATUS_TRAINING_FAIL was received since link training started, set the following bits:

    o INTERLANE_ALIGN_DONE shall be set to 0b.

    o LANEx_CHANNEL_EQ_DONE is equal to the DP IN internal status ANDed with *LANEx_CHANNEL_EQ_DONE* that was received *as MSG Data* by the STATUS_TRAINING_FAIL.

    o LANEx_SYMBOL_LOCKED is equal to the DP IN internal status ANDed with *LANEx_SYMBOL_LOCKED* that was received *as MSG Data* by the STATUS_TRAINING_FAIL.

- Else, a DP IN Adapter shall use one or more of the methods below to indicate to DPTX that link training has not completed successfully yet:

~~A DP IN Adapter shall respond to a DPTX and indicate that link training has not ended successfully yet for the following cases:~~

- ~~The conditions, as defined in this section, for successful link training were not met.~~
- ~~The DP IN Adapter received a SET_CONFIG Packet of type STATUS_TRAINING_FAIL.~~

~~A DP IN Adapter shall use one or more of the methods below to indicate to DPTX that link training is not completed successfully yet:~~

    o Set INTERLANE_ALIGN_DONE to 0b.
    o Set LANEx_CHANNEL_EQ_DONE to 0b for any of the active lanes.
    o Set LANEx_SYMBOL_LOCKED to 0b for any of the active lanes.

Note: Which indication(s) to negate is implementation specific.

10.4.10.2.2   DP OUT Adapter Requirements

A DP OUT Adapter receiving a SET_CONFIG Packet of type SET_LINK, with *LC* field other than 0h shall:

- Initiate link training with the target Link Rate and Lane Count received from the SET_LINK Packet.

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- Link training proceeds according to the DisplayPort 1.4a spec except that a DP OUT Adapter that concludes that it needs to either reduce the Link Rate or Lane Count shall treat it as link training failure and shall not reduce the Link Rate or Lane Count.

A DP OUT Adapter which finishes the Clock Recovery Sequence (as defined in the DisplayPort 1.4a Specification) shall send a SET_CONFIG Packet of type STATUS_CR_DONE, reflecting the LANEx_CR_DONE statuses of the active lanes. The *Phase* field shall be set to 0b.

A DP OUT Adapter in EQ phase which detects that the DP receiver has lost Clock Recovery on one or more of the active lanes shall conclude that link training has failed and shall send a SET_CONFIG Packet of type STATUS_CR_DONE, reflecting the new LANEx_CR_DONE statuses of the active lanes. The *Phase* field shall be set to 1b.

If link training fails for a reason other than lost Clock Recovery, a DP OUT Adapter shall send a SET_CONFIG Packet of type STATUS_TRAINING_FAIL. The MSG Data shall be set as follows:

- *LANEx_CHANNEL_EQ_DONE* is equal to the value of the last read from LANEx_CHANNEL_EQ_DONE field in DPRX.

- *LANEx_SYMBOL_LOCKED* is equal to the value of the last read from LANEx_SYMBOL_LOCKED field in DPRX.

If link training finishes successfully, a DP OUT Adapter shall:

- Send a SET_CONFIG Packet of type SET_LINK, with the same *LC* and *LR* fields it received from the DP IN Adapter when link training was initiated.
- Generate IDLE pattern (including SR) for both MST and SST DP Links.