USB 3.0 Electrical Compliance Methodology White Paper

Revision 0.5

Contents

1. Introduction

1.1 Purpose

The physical layer section (chapter 6) of the USB 3.0 specification defines informative and normative specifications for SuperSpeed transceivers. This document describes the compliance test fixtures, data patterns, and measurement and analysis methodologies for the USB 3.0 SuperSpeed interface. The transmitter and receiver will be tested for compliance to the normative specification parameters with the reference channels defined in this document. Figure 1 shows representations of the SuperSpeed USB channel, including the transmitters and receivers.

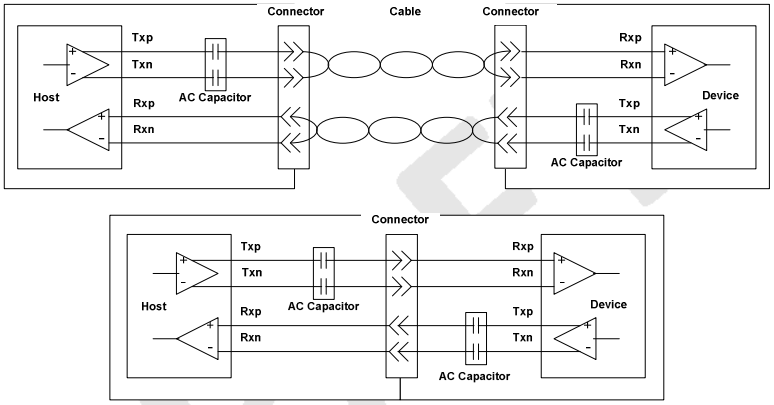


Figure 1. USB channel schematics – with and without cable.

1.2 Methodology Overview

The ideal compliance test for transmitters (Tx) and receivers (Rx) is to test them in a full system with a spec limit Tx or Rx in a package on the other side. The methodology presented here attempts to get as close to this as possible while balancing complexity and cost. This document describes the compliance reference host, cable and device design characteristics, the compliance testing setup, the usage of compliance patterns to test compliance to specific metrics, and considerations for compliance data capture, extraction and analysis.

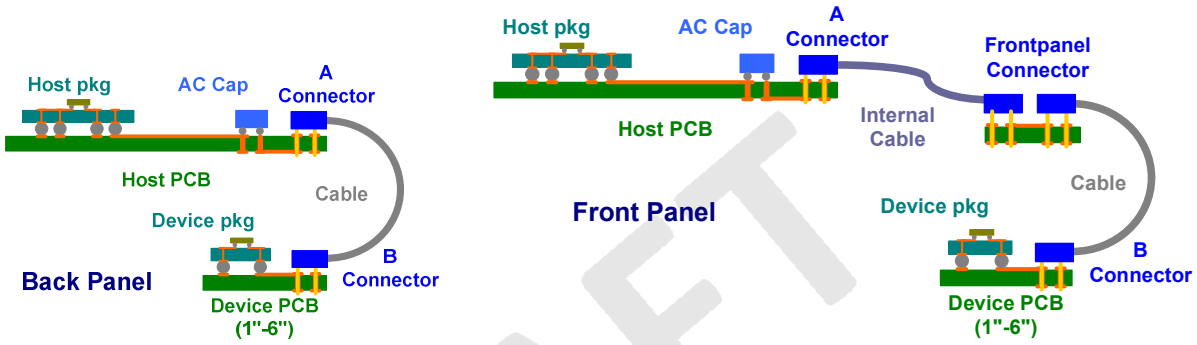
1.3 References

Universal Serial Bus 3.0 Specification, revision 1.0.

Universal Serial Bus 3.0 SuperSpeed Electrical Compliance Test Specification, revision 0.5.

2. Compliance Channels

In order to cover the wide range of expected applications, two compliance channels are defined for electric compliance testing. One of the reference channels is intended to represent a long channel, such as a back panel port in a desktop client, in which the performance is largely determined by channel loss. The other reference channel is intended to represent a shorter channel, such as a front panel port, in which reflections play a larger role in determining the performance. The physical characteristics for both types of channels are shown in Figure 2 and Figure 3, and the electrical characteristics of the printed circuit boards and cables are summarized in Figure 4.



(a) Back panel port channel topology

(b) Front panel port channel topology

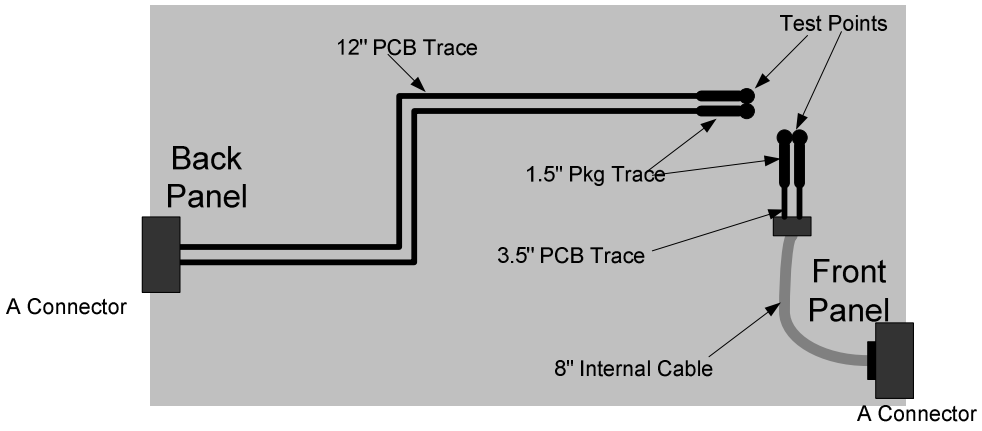
Figure 2. Example channels for front panel and back panel ports.

The compliance channel configurations are defined with the intent of getting the best possible correlation between compliance measurement and the actual performance at the silicon. Figure 3 depicts the planned compliance channel designs for hosts, devices and cables. The host and cable compliance channels are used in testing of devices. The device and cable compliance channels are used for testing of host designs.

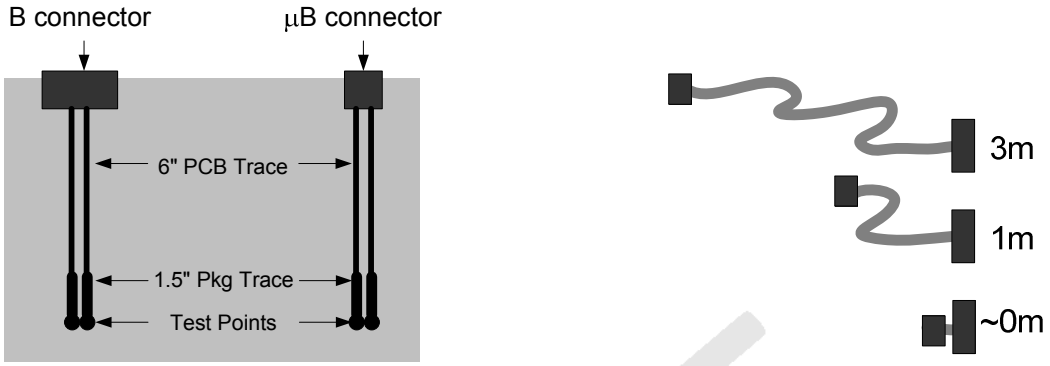
As the figure shows, the host reference board contains channels that represent both front (short, reflective) and back panel (long, lossy) applications. For compliance, a device must pass testing with both configurations. The device reference board contains both the standard B connector and the micro B connector. For compliance, a host must pass testing with both configurations.

An additional feature of the compliance boards is that they contain routing to represent both the PCB and the package. The traces that represent the package are compensated to reflect the lower impedance that package routing typically contains.

Though not shown explicitly in the figures, the reference board contains lanes for testing both transmitter and receiver. The reference boards also contain AC coupling caps on the transmitter lanes.



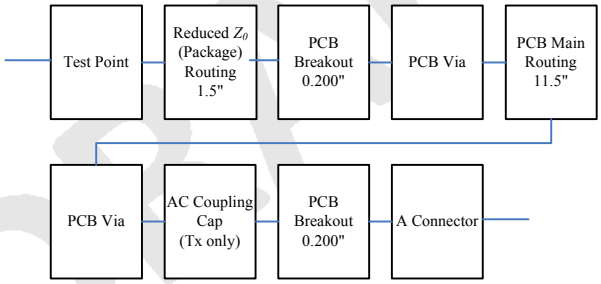
(a) Host reference design



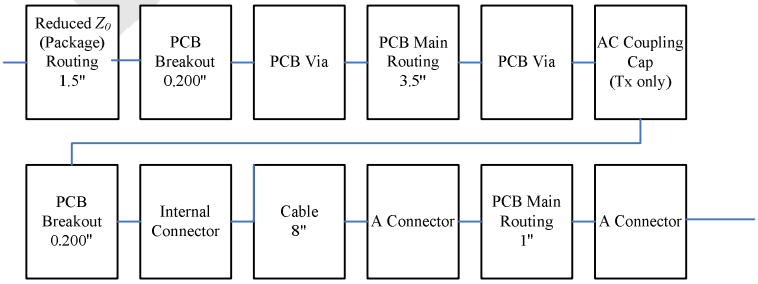
(b) Device reference design

(c) Reference cables

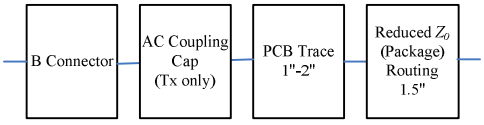
Figure 3. Reference channels for compliance testing (Host, Device, Cables)



(a) Back Panel Host Reference channel



(b) Front Panel Host Reference channel



(c) Device Reference channel

Figure 4. Topology details for host and device reference channels.

3. Compliance Channel Models

Models of compliance channels, in Touchstone® format, are available for use in design and characterization of SuperSpeed devices. They can be found at the USB website (www.usb.org).

Due to the lossy nature of the channel, the data eye at the receiver input may be closed. USB 3.0 allows the use of receiver equalization to meet system timing and voltage margins, in the form of a continuous time linear equalizer (CTLE). The Rx equalizer may be required to adapt to different channel losses using the Rx EQ training period. The exact Rx equalizer and training method is implementation specific.

Compliance testing for the transmitter eye requires the use of a reference CTLE, which is described by equation (1) below. Table 1 describes the parameters of the reference equalizer and Figure 5 plots the transfer function.

$$H(s) = \frac{A_{dc}\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})} \quad (1)$$

where $H(s)$ is the reference CTLE transfer function

Table 1. Reference CTLE design parameters

Parameter	*Value*	*Description*
A_{dc}	0.667	DC gain
ω_z	2π(650 MHz)	Zero frequency
ω_{p1}	2π(1.95 GHz)	1st pole frequency
ω_{p2}	2π(5 GHz)	2nd pole frequency

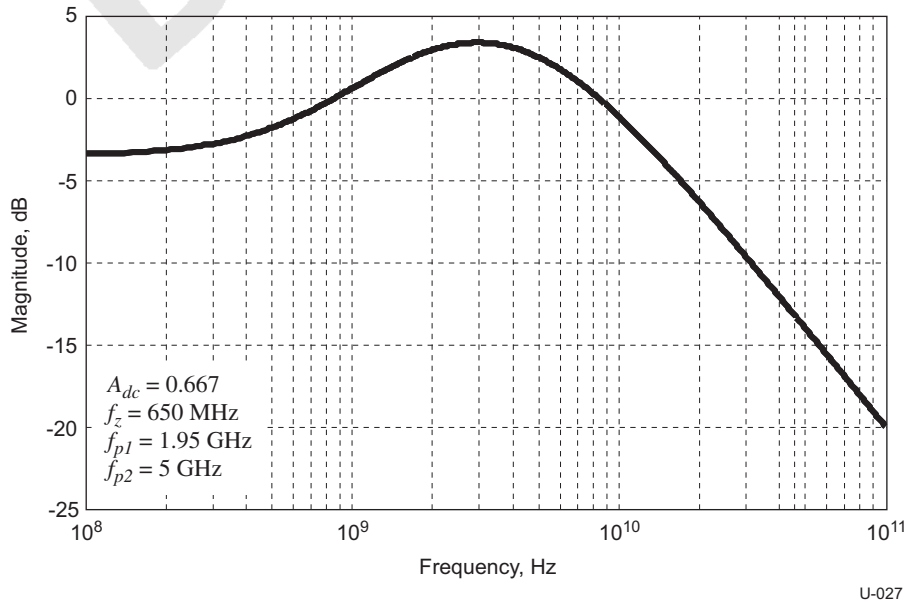


Figure 5. Tx Compliance Rx EQ Transfer Function.

4. Compliance Tests

4.1 Compliance Mode Entry and Data Patterns

Entry to the Polling.Compliance substate is described in Chapter 7 of the USB 3.0 specification. It initiates the transmission of the first compliance pattern (CP0), which is a pseudo–random data pattern generated by the scrambled D10.0 compliance sequence. Note: No SKPs are sent during the compliance pattern transmission.

The compliance pattern is transmitted continuously or until a Ping.LFPS is detected at the receiver. (Refer to Section 6.9 of the USB 3.0 specification.) Detection of a Ping.LFPS signal causes the transmitting device to advance to the next compliance pattern. Upon detection of a Warm Reset, the compliance pattern transmission is terminated. The compliance pattern sequences are described in Table 2.

The use of the compliance pattern sequences is described in sections 4.2 and 4.3.

Table 2. Compliance pattern sequences

Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7 of the USB 3.0 specification) but does not include SKP sequences.
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1’s and 0’s	With de-emphasis. Repeating 50-250 1’s and then 50-250 0’s.
CP8	50-250 1’s and 0’s	Without de-emphasis. Repeating 50-250 1’s and then 50-250 0’s.

Note: Unless otherwise noted, scrambling is disabled for compliance patterns.

4.2 Transmitter Compliance

The compliance testing setup for transmitters is shown in Figure 6. All measurements are made at the test point (TP1), and the transmitter specifications are applied after processing the measured data with the compliance reference equalizer transfer function described in Section 3.

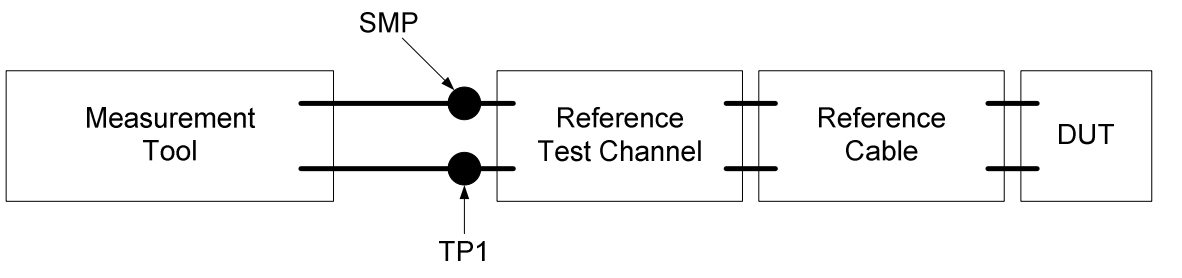


Figure 6. Tx compliance testing setup

The compliance tests for individual transmitter specifications are summarized in Table 3. Additional descriptions of the tests follow.

Compliance pattern CP8 creates a quasi-step function by sending 50 to 250 successive logical 1's followed by an equal number of logical zeros. This pattern continues until detection of Ping.LFPS or Warm Resest, as described above. Effectively, CP gives a periodic signal with a 10 MHz to 50 MHz frequency. The frequency is low enough to allow DC specifications to be measured, in particular the differential swing and differential impedance.

Compliance pattern CP7 is identical to CP8, except that it includes de-emphasis for measurement of compliance to the transmit de-emphasis specification.

Compliance to the maximum jitter and minimum eye height specs is measured using the CP0 pattern. It is a pseudo-random pattern that is created by the scrambling of the logical idle pattern (D0.0). The pattern repeats every 65,536 symbols, or every 655,360 encoded bits. The measured data must be post-processed through the reference CTLE in order to provide an open data eye. The minimum eye height may be found from an eye diagram capture on the scope.

The data lane under test is sampled, and a post processing analysis software package (SigTest) is then used to analyze the data. Sigtest performs the RJ/DJ extraction and extrapolation, and includes the reference CTLE function. SigTest supports all common RT scope data formats.

Since DJ/RJ separation can be difficult, compliance pattern CP1 is provided in order to assist with the separation. CP1 is simply a sequence of alternating zeros and ones toggling at the maximum switching rate of the link. This eliminates one source of deterministic jitter, channel DJ caused by intersymbol interference. Channel-induced jitter with scrambled data tends to appear to be Gaussian in nature, so removal of this source may make it easier to extract the random jitter.

The extracted jitter must be properly analyzed against the specifications. In particular, the random jitter must be estimated the target the target bit error ratio (BER) of 10^{-12}. Since we are transmitting only 10^6 data bits, the compliance measurement does not directly capture all of the random jitter that exists in the system. Accounting for the RJ at the target BER requires that the root-mean-square (RMS) random jitter be multiplied by 14.069.

Table 3. Summary of transmitter compliance tests

Parameter	Symbol	Specification	Data Pattern	Notes
Differential Swing	$V_{TX-DIFF-PP}$	0.8V – 1.2V	CP8	4, 5
De-emphasis	$V_{TX-DE-RATIO}$	3.0dB – 4.0dB	CP7	4, 5
DC differential impedance	$R_{TX-DIFF-DC}$	72Ω - 120Ω	CP8	4, 5
Deterministic Jitter	Dj	0.465UI (max)	CP0	1, 2, 4
Random Jitter	Rj	0.30UI (max)	CP0, CP1	1, 2, 4
Total Jitter	Tj	0.66UI (max)	CP0	1, 2, 4
Eye Height		100mV (min)	CP0	1, 2, 3, 4

Notes:

1. Measured over 10^6 consecutive UI and extrapolated to 10^{-12} BER. The Rj specification is calculated as 14.069 times the RMS random jitter for 10^{-12} BER.
2. Measured after receiver equalization function.
3. The eye height is to be measured at the maximum opening (at the center of the eye width ± 0.05 UI).
4. All specified values in this table were extracted from tables 6-10 and 6-12 of the USB 3.0 Specification. In case of conflict, the values in the USB 3.0 Specification supersede those contained herein.
5. Optional measurement for characterization and troubleshooting purposes.

4.3 Receiver Compliance

The receiver jitter tolerance test is performed using the compliance reference channel shown in Figure 10. A pattern generator sends a compliance test pattern with added jitter through the compliance reference channels to the receiver. When running the compliance tests, the receiver should be put into loopback mode. The receiver loops back the data and any difference in the pattern sent from the pattern generator and returned is counted as an error.

A second method exists in which the receiver can be put into BERT mode, in which it counts errors and transmits them back to the transmitting agent. The purpose of the receiver loopback BERT feature is to provide a more accurate estimate of the measured BER by avoiding any errors that can occur on the loopback data path.

When performing the jitter tolerance measurement, the reference clocks for both the transmitting equipment and the device under test must be put into spread spectrum mode. The jitter tolerance test includes sources of both random jitter and deterministic jitter (in the form of sinusoidal jitter). The characteristics of the RJ and DJ sources are summarized in Table 6, and are specified at the test point, TP1 in Figure 10.

In addition to the above characteristics, note that the output from the transmitter is equalized with a minimum swing of 0.75V.

The recommended data sequence is the scrambled logical idle (D0.0). If using the loopback BERT, then scrambled D0.0 must be used. The reference channel will add deterministic jitter to the signal seen by the receiver.

Testing to the 10^{-12} BER delineated in the USB 3.0 specification requires transmission of 2.996×10^{12} bits without error for a 95% statistical confidence level. This corresponds to a duration of approximately 10 minutes per test point, and 50 minutes total for the five frequencies defined in the specification.

In order to reduce test times to more manageable levels, SuperSpeed USB plans to employ an accelerated BER testing approach. In this approach, we add a sufficient amount of DJ at the transmitter to increase the budgeted BER from 10^{-12} to 10^{-10}. Figure 7 compares the jitter PDFs for the two BERs obtained using the dual Dirac model that upon which the SuperSpeed jitter budget it based. Figure 8 shows the resulting BER bathtub curves demonstrating that by increasing the injected DJ at the transmitter from 41 ps to 46.43 ps we increase the BER that we obtain from the budgeted jitter values moves the resulting BER from 10^{-12} to 10^{-10}. In addition to the DJ, we also inject RJ with a an RMS value 2.42 ps (34.05 ps at BER = 10^{-12} and 30.79 ps at BER = 10^{-10}). The original and revised jitter budgets for BER equal to 10^{-12} and 10^{-10} are summarized in Table 4.

The planned receiver jitter tolerance testing approach also affects the jitter tolerance requirements at low frequencies, as shown in Figure 9 and Table 5. The complete set of jitter tolerance test conditions are described in Table 6.

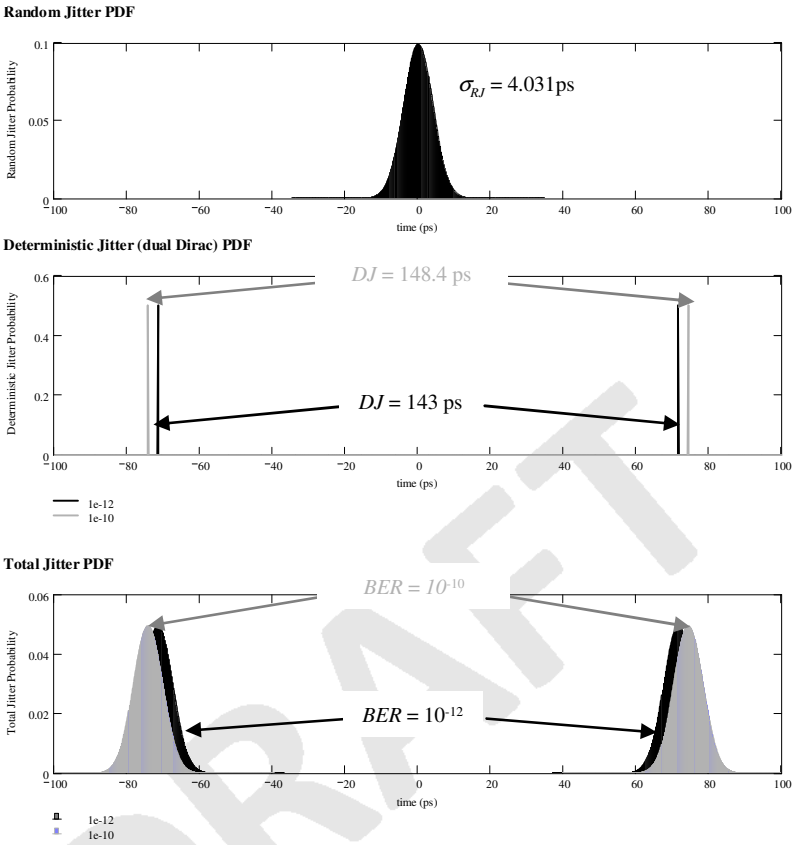


Figure 7. Dual-Dirac jitter PDFs for BER = 10^{-12} and 10^{-10}

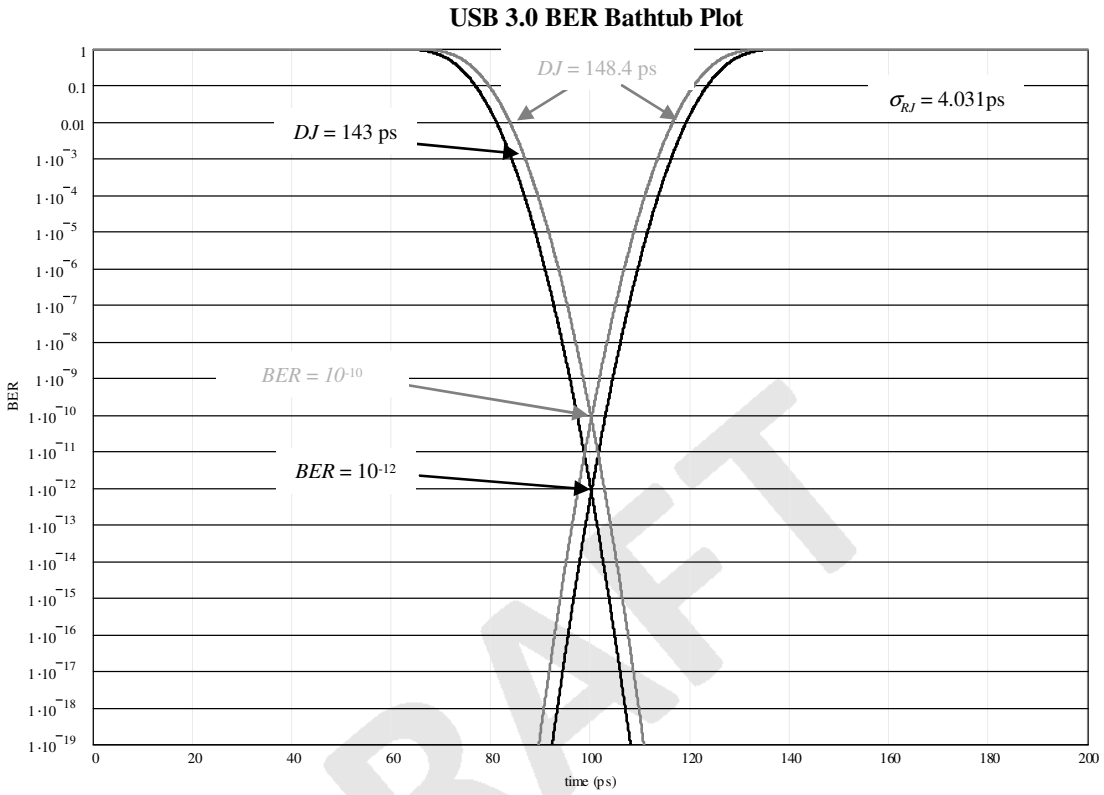


Figure 8. Jitter bathtub curves for BER = 10^{-12} and 10^{-10}

Table 4. Comparison of jitter specs for BER = 10^{-12} and 10^{-10}

		BER	
		10^{-12}	10^{-10}
Transmitter	***DJ* (ps)**	41.00	46.43
	σ_{RJ} (ps)	2.42	
Channel	***DJ* (ps)**	45.00	
	σ_{RJ} (ps)	2.13	
Receiver	***DJ* (ps)**	57.00	
	σ_{RJ} (ps)	2.42	
System	***DJ* (ps)**	143.00	148.43
	σ_{RJ} (ps)	4.031	
	***TJ* (ps)**	199.713	199.713
# Transmitted bits		$2.996 \cdot 10^{12}$	$2.996 \cdot 10^{10}$
Test Duration (s)		599.2	5.99

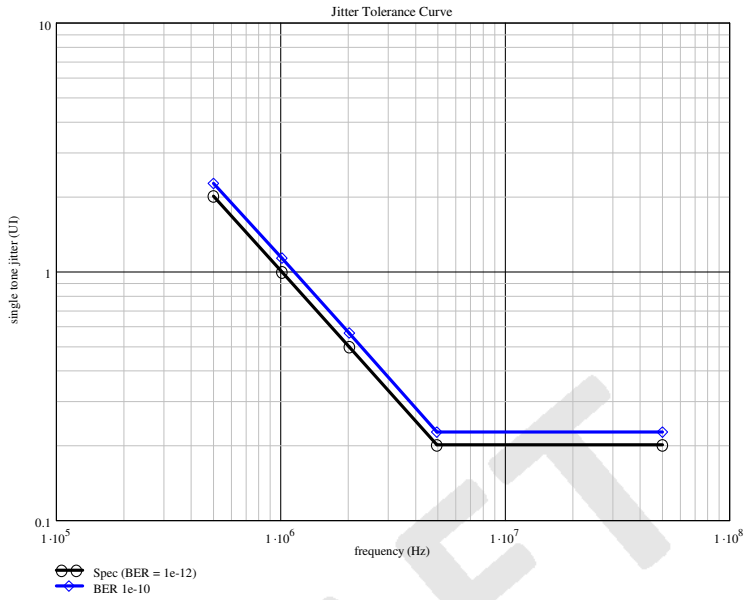


Figure 9. Receiver jitter tolerance curves for BER = 10^{-12} and 10^{-10}

Table 5. Jitter tolerance curves for BER = 10^{-12} and 10^{-10}

Frequency (Hz)	Jitter (UI)		Jitter (ps)	
	BER=10^{-12}	BER=10^{-10}	BER=10^{-12}	BER=10^{-10}
$5x10^5$	2	2.265	400	453
$1x10^6$	1	1.132	200	226.4
$2x10^6$	0.5	0.566	100	113.2
$4.9x10^6$	0.205	0.232	41	46.4
$5x10^7$	0.205	0.232	41	46.4

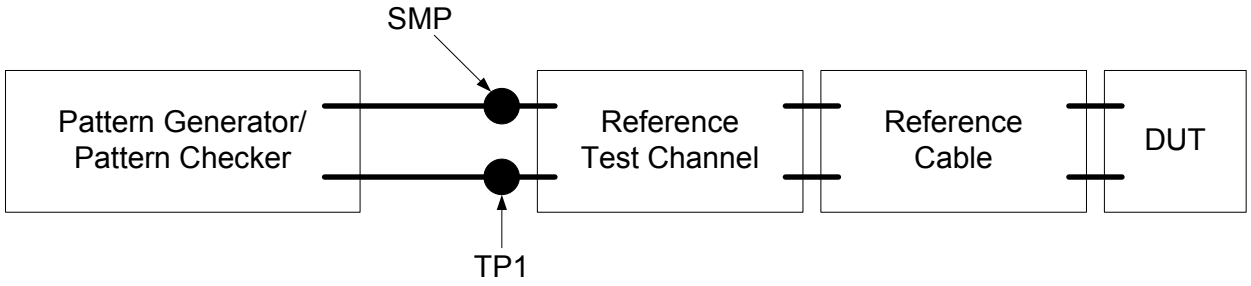


Figure 10. Receiver compliance testing setup

Table 6. Input jitter requirements for Rx tolerance testing

Symbol	Parameter	Value	Units	Notes
f1	Tolerance corner	4.9	MHz	1,2,3,5
J_{Rj}	Random Jitter	0.0121	UI rms	1,2,3,4
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-10}	0.154	UI p-p	1,2,3,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2.265	UI p-p	1,2,3,4
J_{Pj_1Mhz}	Sinusoidal Jitter	1.132	UI p-p	1,2,3,4
J_{Pj_2MHz}	Sinusoidal Jitter	0.566	UI p-p	1,2,3,4
J_{Pj_f1}	Sinusoidal Jitter	0.232	UI p-p	1,2,3,4
J_{Pj_50MHz}	Sinusoidal Jitter	0.232	UI p-p	1,2,3,4
V_full_swing	Transition bit differential voltage swing	0.75	V p-p	1,2,3,5
V_EQ_level	Non transition bit voltage (equalization)	-3	dB	1,2,3,5

Notes:

1. All parameters are measured at TP1 Figure 10.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Specified for a budgeted BER of 10^{-10}.
5. All specified values in this table were extracted from tables 6-19 of the USB 3.0 Specification. In case of conflict, the values in the USB 3.0 Specification supersede those contained in this row.

4.4 Channel Characterization (Informative)

In some situations it is desirable to characterize the behavior of interconnect in order to diagnose the cause of compliance issues. This can be done using a subset of the compliance patterns listed in Table 7 with the transmitter compliance configuration shown in Figure 6. By transmitting each pattern and measuring the minimum eye height, a plot of the approximate insertion loss can be constructed (Figure 11). Such a plot can then be compared against the expect response obtained via simulation.

Table 7. Compliance pattern usage for characterizing channel insertion loss

Description	Pattern	Frequency range
Nyquist rate	CP1	2.5 GHz
Half-Nyquist rate	CP2	1.25 GHz
K28.7	CP4	500 MHz
LFPS	CP5	20 – 100 MHz
	CP8	10 – 50 MHz

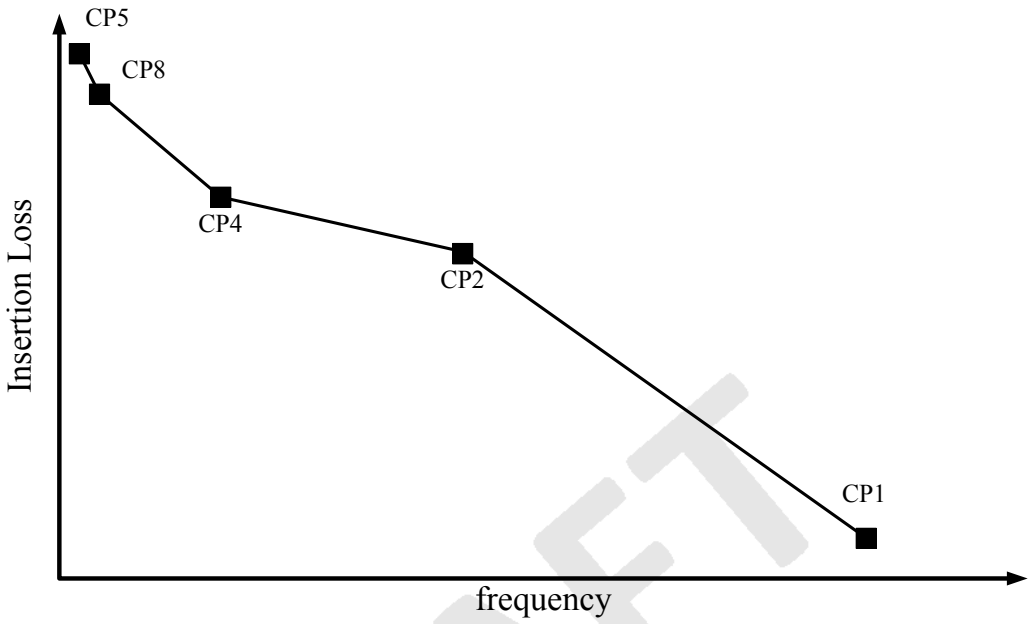


Figure 11. Example insertion loss plot