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# Alternate BMC Receiver Design Examples

*USB Power Delivery - Informative White Paper*

Revision 1.1

January 1, 2026

# Alternate BMC Receiver Design Examples

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## Revision History

Revision	Date	Author	Description
1.0	2016-06-28	J. Tsai	original.
1.1	2026-01-01	S. Jackson	Split out from USB PD Specification.

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### 1. Scope

This document is informative and does not define requirements.

### 2. Overview

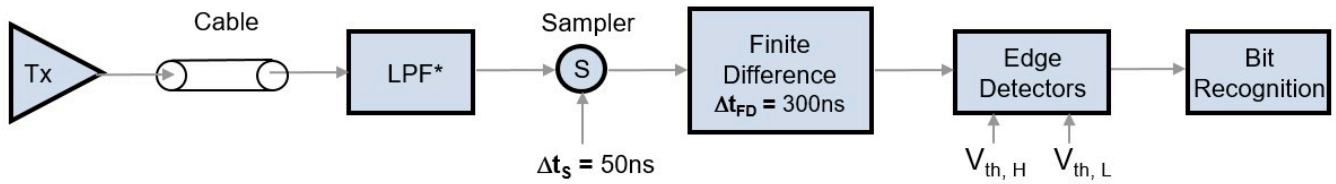
The USB PD BMC signal (as defined in the USB PD specification) is DC-coupled so that the voltage level is affected by the ground IR drop through the cable and connectors. The DC offsets of the BMC signal at the Source and the Sink are in opposite directions. When the VBUS current is increased from 0A, the BMC signal waveform shifts downward at the Sink and upward at the Source. This companion document introduces two sample BMC receiver circuit implementations, which are immune to DC offset and high-current load steps. They can be used in Sources, Sinks, and Cable Plugs.

### 3. Finite Difference Scheme

#### 3.1. Sample Circuitry

The sample Finite Difference BMC receiver shown in [Figure 1](#) consists of the Rx bandwidth-limiting filter with time constant  $t_{RxFilter}$  (as defined in the USB PD specification), a sampler with 50 ns sampling step  $\Delta t_S$ , a Finite Difference Calculator that measures the voltage difference over  $\Delta t_{FD} = 300$  ns, an edge detector controlled by thresholds  $V_{th,H}$  and  $V_{th,L}$ , and a logic block for bit recognition.

**Figure 1. Circuit Block of BMC Finite Difference Receiver**



### 3.2. Theory

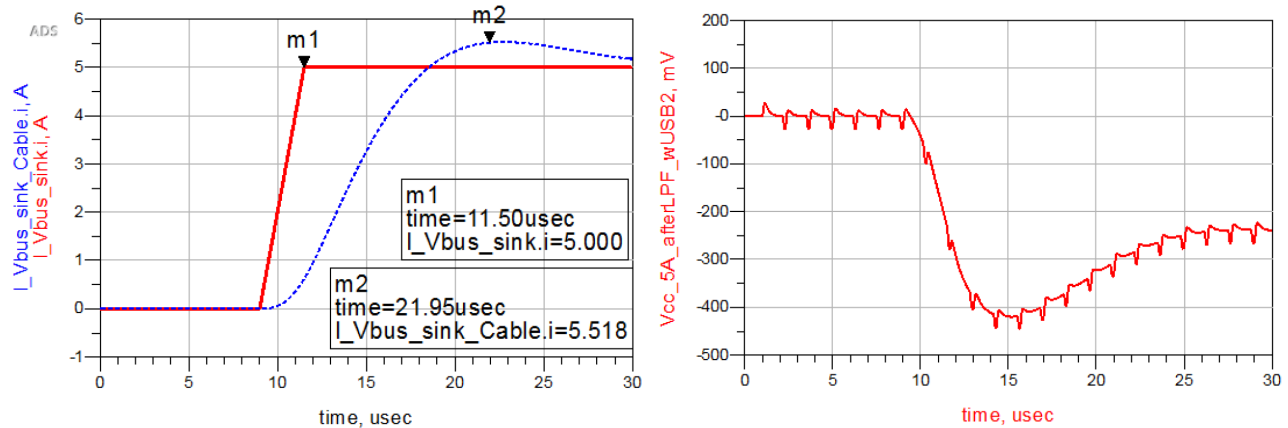
This section describes the fundamental theory of the Finite Difference Scheme to recover the received BMC signal with the input and output waveforms of the circuit blocks shown in [Figure 1](#). To illustrate robustness, the VBUS current load step rate is intentionally increased to 2A/μs at the Sink load. In [Figure 2](#) (a), the red curve shows the VBUS current at the Sink rising from 0A to 5A at 9 μs, and the blue dashed curve shows the VBUS current at the USB Type-C connector of the Sink. The peak current overshoot rises to 518 mA.

[Figure 2](#) (b) shows the total BMC noise at the Sink, coupled from VBUS and D+/D- through the worst [USB Type-C 2.4] compliant cable after the Rx bandwidth-limiting filter with time constant tRxFilter is applied. The noise has three components.

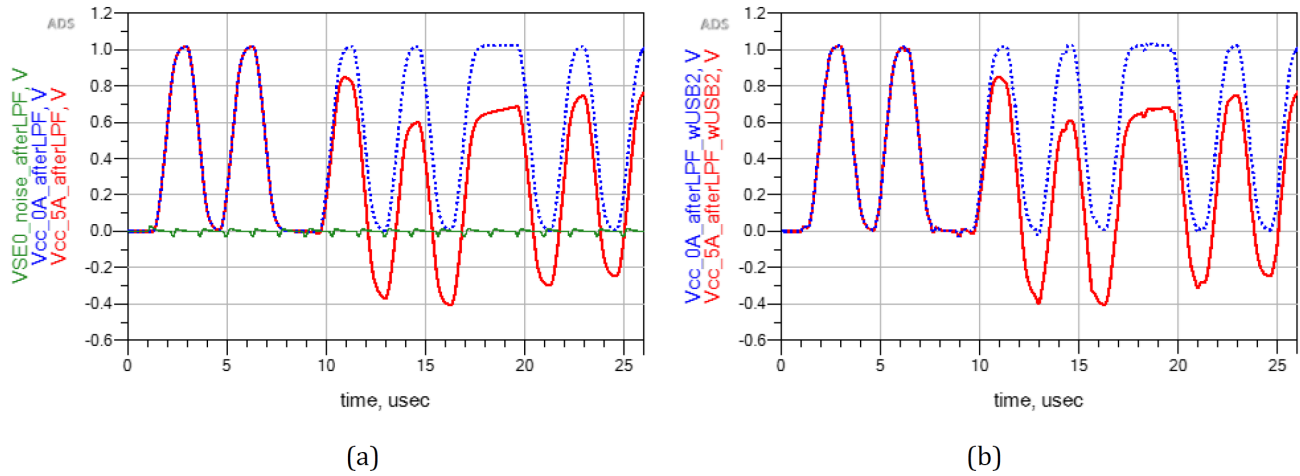
The first is the DC offset,  $I_{VBUS}(t) \times R_{GND}$ , while  $I_{VBUS}$  is the VBUS current and  $R_{GND}$  is the ground DC resistance of the cable. The offset is negative in the Sink and positive at the Source. The second is the inductive VBUS noise,  $M \times dI_{VBUS}(t) \div dt$ , where  $M$  is the mutual inductance between the VBUS and CC wires and  $dI_{VBUS}(t) \div dt$  is the load step rate. The third component is [USB 2.0] Full Speed SE0 coupling noise, modeled as periodic to capture crosstalk with the BMC signal.

[Figure 3](#) compares the BMC signal with and without VBUS current. The blue dashed curve shows the BMC signal without VBUS current; the red solid curve shows the BMC signal with the VBUS coupling noise from [Figure 2](#) (b). The green solid curve is the sample [USB 2.0] noise after the Rx bandwidth-limiting filter with time constant tRxFilter is applied.

**Figure 2. BMC AC and DC noise from VBUS at Sink**

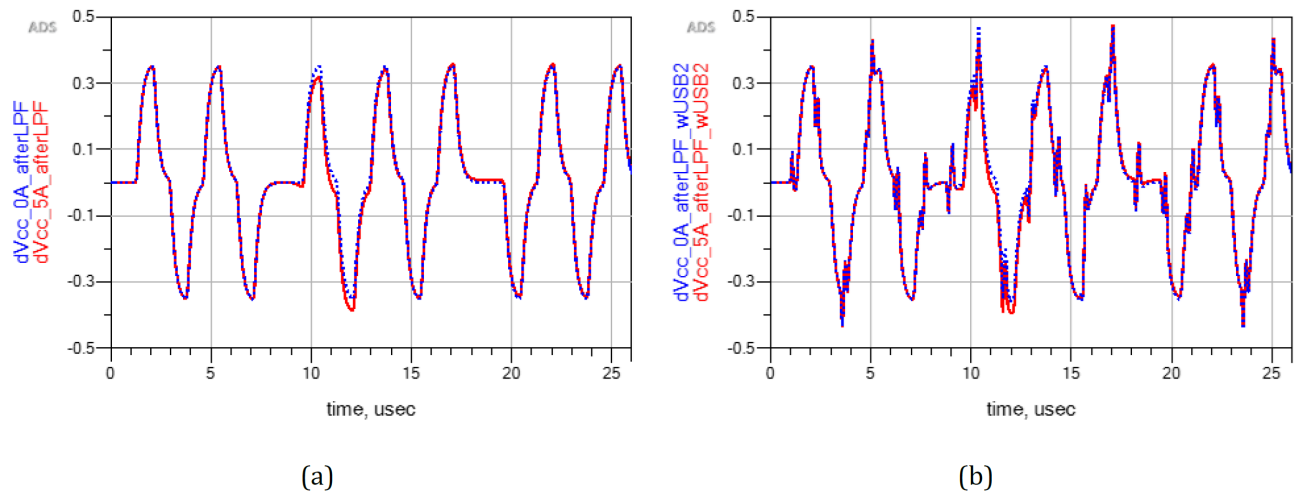


**Figure 3. Sample BMC Signals (a) without USB 2.0 SE0 Noise (b) with USB 2.0 SE0 Noise**



The BMC signals shown in [Figure 3](#) are sampled every 50 ns, and the scaled derivative waveforms  $V_{cc}(t) - V_{cc}(t - 50 \text{ ns})$  with and without [USB 2.0] noise are shown in [Figure 4](#) (a) and (b). When [USB 2.0] noise is absent, the derivative changes only slightly before and after the VBUS current transition, indicating that the BMC waveform slope is insensitive to DC offset and supports a robust receiver. With [USB 2.0] noise present, the derivative exhibits large perturbations as shown in [Figure 4](#) (b).

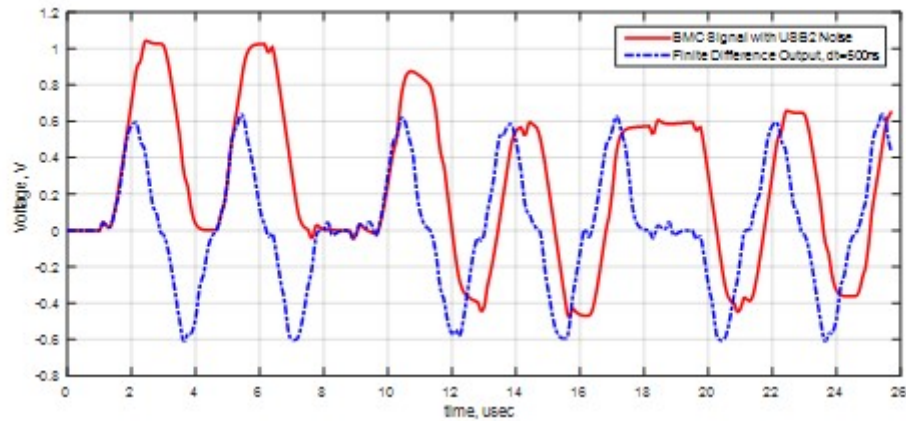
**Figure 4. Scaled BMC Signal Derivative with 50ns Sampling Rate (a) without USB 2.0 Noise (b) with USB**



To remove the high-frequency content of the [USB 2.0] noise, apply the Finite Difference technique with an appropriate time interval to the BMC waveform with [USB 2.0] noise in [Figure 3](#).

Using the Backward Finite Difference Calculator,  $\Delta V_{cc} = V_{cc}(t) - V_{cc}(t - \Delta t)$ , [Figure 5](#) shows the Finite Difference Output when  $\Delta t = 500 \text{ ns}$ . Larger  $\Delta t$  yields a larger peak-to-peak magnitude, but  $\Delta t$  is bounded by the BMC rise time; 300 ns to 500 ns is a good range.

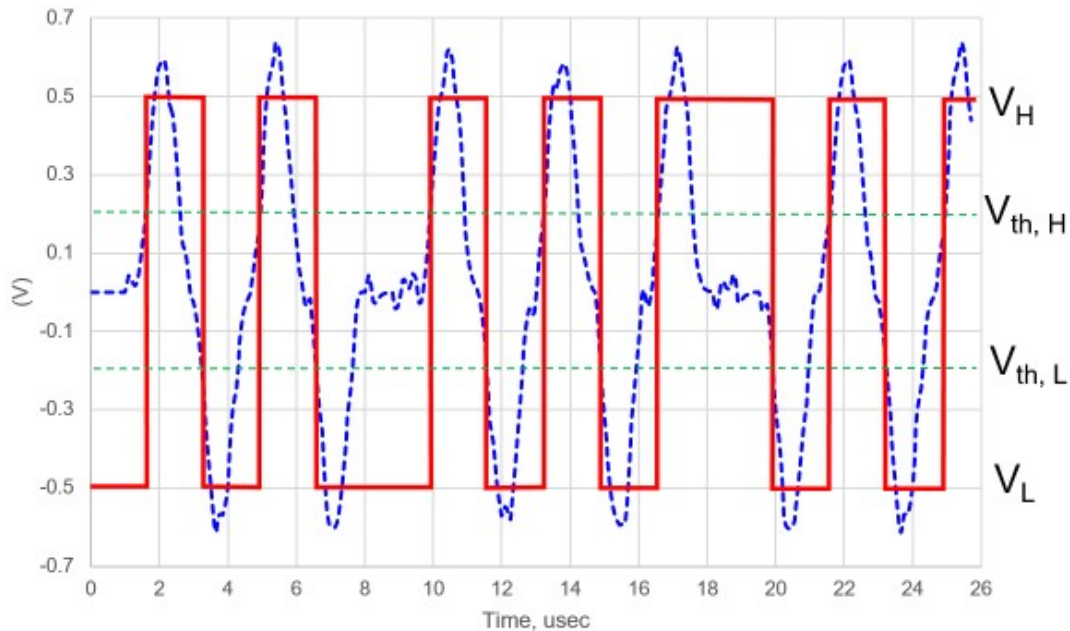
**Figure 5. BMC Signal and Finite Difference Output with Various Time Steps**



### 3.3. Data Recovery

Edge detection follows the Finite Difference Calculation. At the input of the edge detector, if the voltage is greater than  $V_{th,H}$  at the rising edge, the output becomes high ( $V_H$ ); if the voltage is less than  $V_{th,L}$  at the falling edge, the output becomes low ( $V_L$ ). In this example,  $V_{th,H}$  and  $V_{th,L}$  are 0.2V and -0.2V, respectively. The solid curve in [Figure 6](#) represents the output of the edge detector, where  $V_H$  is 0.5V and  $V_L$  is -0.5V.

**Figure 6. Output of Finite Difference as dash line and Edge Detector as solid line**



The duty cycle of the output signal from the edge detector varies depending on the thresholds  $V_{th,H}$  and  $V_{th,L}$ , as well as jitter and noise from silicon and the channel. Techniques such as an integrating receiver can be used to recover the BMC signal.

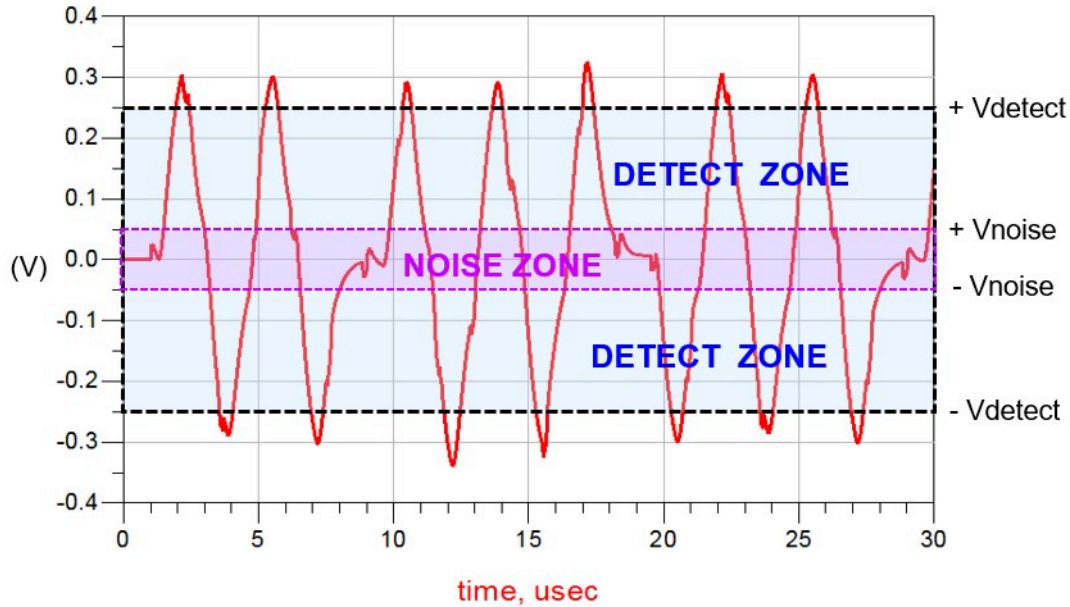
### 3.4. Noise Zone and Detection Zone

[Figure 7](#) shows the output of Finite Difference when the time interval of Finite Difference is set to 300ns. The noise zone is defined in between +Vnoise and -Vnoise, in which the noise glitches occur. The detect zone is defined in

between +Vdetect and -Vdetect, excluding the noise zone. The thresholds of the edge detectors,  $V_{th,H}$  and  $V_{th,L}$ , must be properly set within the detect zone so that the data can be recovered successfully.

In this example, Vdetect is 250mV and Vnoise is 50mV. It is highly recommended that the product implemented with the similar techniques indicates the performance with the range of Vnoise and Vdetect in the electrical specification.

**Figure 7. Noise Zone and Detect Zone of BMC Receiver**

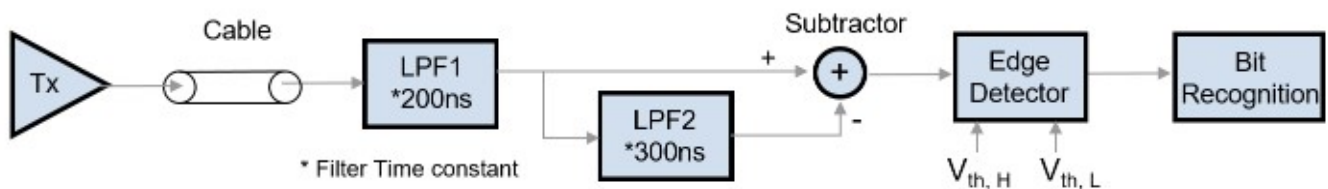


## 4. Subtraction Scheme

### 4.1. Sample Circuitry

The sample Subtraction BMC receiver shown in [Figure 8](#) consists of two Low Pass Filters (LPF1 and LPF2), a Subtractor, an Edge Detector, and a logic block for bit recognition. The time constants of the first and second LPF are 200 ns and 300 ns, respectively. The Subtractor subtracts the LPF1 output from the LPF2 output. The Edge Detector, controlled by two voltage thresholds  $V_{th,H}$  and  $V_{th,L}$ , recovers the data.

**Figure 8. Circuit Block of BMC Subtraction Receiver**

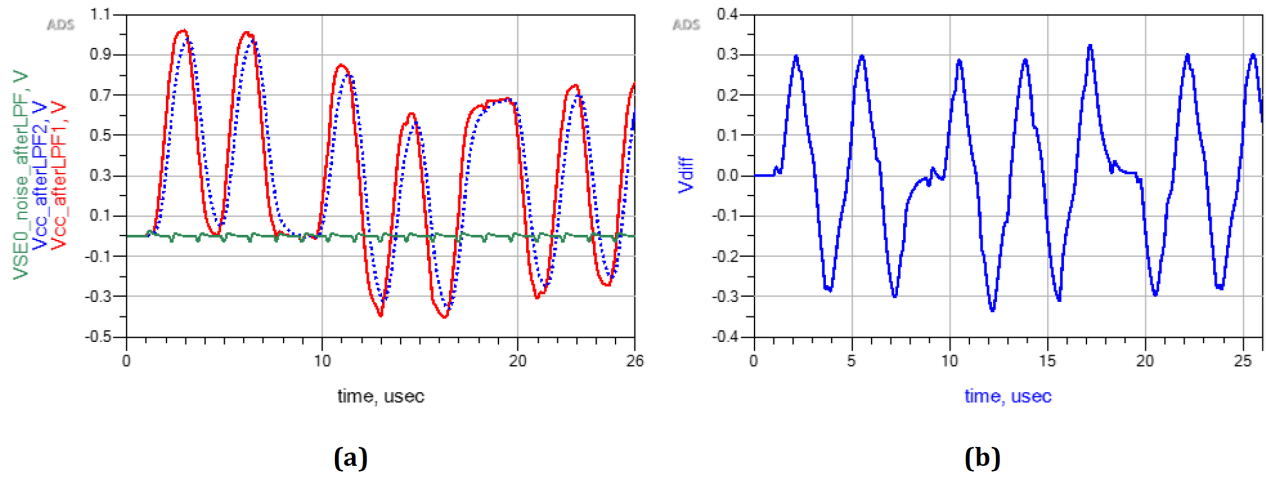


### 4.2. Output of Each Circuit Block

[Figure 9](#) (a) shows the output of LPF1 as the red solid line and LPF2 as the blue dashed line, along with the [USB 2.0] noise in green solid line.

[Figure 9](#) (b) shows the voltage difference between the two output filters,  $V_{diff} = V_{cc\_afterLPF1} - V_{cc\_afterLPF2}$ . The  $V_{diff}$  waveform looks very similar to the Finite Difference output waveform shown in [Figure 6](#), so the data recovery method through the edge detector is the same as described in [Section 3.3](#).

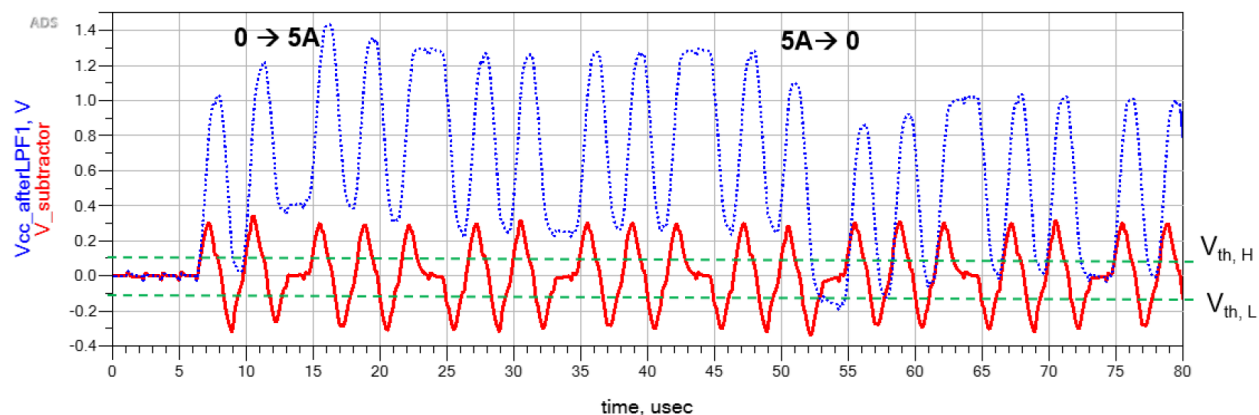
**Figure 9. LPF1 and LPF2 (a) Output (b) Output Difference**



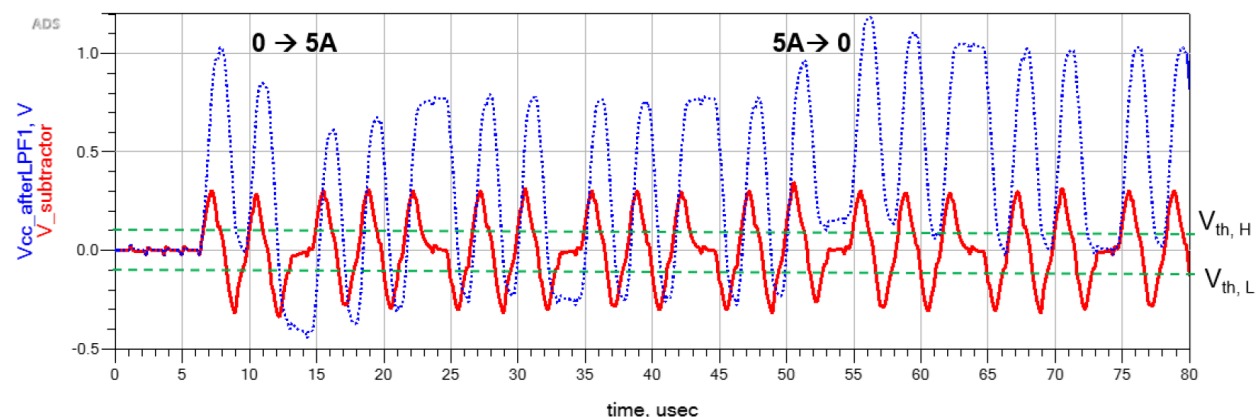
### 4.3. Subtractor Output at Source and Sink

The following figure shows an example when the VBUS current increases from 0A to 5A and then decreases to 0A with a high load step rate. The outputs of LPF1 and the Subtractor at Source and Sink are shown in [Figure 10](#) (a) and (b), respectively. Although the BMC signals at Source and Sink shift in opposite directions, the Subtractor outputs at both locations are almost identical regardless of the opposite DC offset directions.

**Figure 10. Output of the BMC LPF1 in blue dash curve and the Subtractor in red solid curve (a) at Source (b) at Sink**



**(a)**



**(b)**

#### 4.4. Noise Zone and Detection Zone

The zone definition is the same as defined in [Section 3.4](#). The sizes of the noise zone and detect zone of the Subtraction Scheme are dependent on the filter time constant. When the time constants of the first and second LPF are 200 ns and 300 ns, respectively,  $V_{detect}$  is 250 mV and  $V_{noise}$  is 50 mV. Products using similar techniques should report performance across the  $V_{noise}$  and  $V_{detect}$  ranges in the electrical specification.