

***Inter-Chip Supplement to the USB  
Revision 3.0 Specification***

***Revision 1.02***

***May 19, 2014***

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## Revision History

Revision	Issue Date	Comment
1.0	05/03/2012	Version 1.0 release of the supplement.
1.01	02/11/2013	<ul style="list-style-type: none"> <li>• Clarification in Section 2.5.2 about contiguous nature of RRAP and Response Packet behavior.</li> <li>• Update in Table 2-5 for optional disabling of LUP/LDN and a change in the MPHY.TEST register address space.</li> <li>• Update in Table 3-2 for value of PM_ENTRY_TIMER and a new entry for tPortConfiguration.</li> <li>• Clarification in the implementation note of Section 3.2 regarding TX_ProtDORDY behavior.</li> <li>• Clarification in Section 3.8.2.6 for requirements to exit to the MPHY.TEST state.</li> <li>• Clarifications in Section 5.1.2 for the operational model of a DSP disconnect.</li> <li>• Updates in Section 6 for scope for multi-lane support, addition of Analog Loopback and Tx Compliance modes, clarification of requirements for Receive Burst Testing and a change in the MPHY.TEST register address space.</li> <li>• Update to Section 7.3 for a missing label in the figure.</li> </ul>
1.02	05/19/2014	<ul style="list-style-type: none"> <li>• Sec 1.3: Updated reference to M-PHY Spec</li> <li>• Table 2-2 &amp; 2-3: Added attributes that are newly defined in [M-PHY] . Modified required value of RX_PWM_Burst_Closure_Length_Capability</li> <li>• Sec 2.5.2: Clarified requirements for DSP in MPHY.TEST. Clarified when Write Responses are to be provided and when registers may be reset.</li> <li>• Sec 3.2: Clarified normative behavior in implementation note</li> <li>• Sec 3.3: Added note on handling of decode errors</li> <li>• Sec 3.4: Various modifications to clarify clock compensation rules</li> <li>• Sec 3.6.2.2: Clarified the requirement to use PAIR0 for Warm Reset</li> <li>• Sec 3.8: Clarified Rx.Detect.Reset requirements for local RESET assertion. Implementation note added regarding handling of LAU corruption during U2/U3 entry and support for RX_Advanced_Granularity_Capability. Various other minor text modifications</li> <li>• Sec 4: Relaxed the accuracy of timestamps reported in ITP packets.</li> <li>• Sec 5: Clarified requirements for local reset assertion during USP disconnect and the RRAP operational model for DSP disconnect. Added a new section that defines Disconnect timing parameters.</li> <li>• Sec 6: Various clarifications made on the operational behavior of MPHY.TEST. Specified effect of LINE-RESET on MPHY.TEST registers.</li> <li>• Sec 7: Figures edited for clarity.</li> </ul>

**Universal Serial Bus Specification Supplement**  
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## Table of Contents

<b>1</b>	<b>Introduction</b> .....	<b>10</b>
1.1	SSIC Significant Features .....	11
1.2	SSIC and Standard SuperSpeed Comparison .....	11
1.3	Related Documents .....	12
1.4	Terminology.....	12
1.5	Acronyms and Terms .....	12
<b>2</b>	<b>Adaptation of M-PHY for the Physical Layer</b> .....	<b>14</b>
2.1	M-PHY for SSIC Overview .....	14
2.2	M-PHY MODULE Capabilities.....	14
2.3	M-PHY Configuration Attributes .....	21
2.4	M-PHY State Machine .....	22
2.5	LS-MODE Support.....	22
<b>3</b>	<b>Link Layer</b> .....	<b>31</b>
3.1	Bit and Byte Ordering .....	31
3.2	Logical Idle and FLR non-insertion.....	32
3.3	Line Coding .....	33
3.4	Clock Compensation .....	34
3.5	Data Scrambling .....	36
3.6	PowerOn Reset and Inband Reset.....	37
3.7	Link Layer Timing Requirements.....	38
3.8	SSIC Link Training and Status State Machine (LTSSM).....	39
<b>4</b>	<b>Protocol Layer</b> .....	<b>51</b>
4.1	Port Capability Link Management Packet (LMP) .....	51
4.2	Timing Parameters .....	51
<b>5</b>	<b>Device Framework</b> .....	<b>53</b>
5.1	Dynamic Attachment and Removal .....	53
<b>6</b>	<b>MPHY.TEST</b> .....	<b>55</b>
6.1	Overview.....	55
6.2	Entering MPHY.TEST.....	56
6.3	Loopback Testing .....	57
6.4	Receive Burst Testing .....	58
6.5	Tx Compliance Mode.....	58
6.6	Analog Loopback Mode.....	58
6.7	MPHY.TEST Block Registers .....	59
<b>7</b>	<b>Timing Diagrams Appendix (Informative)</b> .....	<b>63</b>
7.1	SS.DISABLED TO RX.DETECT .....	63
7.2	RX.DETECT TO POLLING .....	64
7.3	POLLING TO U0 .....	65
7.4	U0 TO U1 .....	66
7.5	U1 TO U0 .....	67
7.6	U0 TO U2/U3.....	68

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7.7	U2/U3 TO U0 .....	69
7.8	USP Disconnect .....	70
7.9	DSP Disconnect .....	71

## Figures

Figure 1-1 SSIC Layers with modifications from [USB3.0] highlighted.....	10
Figure 1-2 Example of an implementation with a PHY Adapter Layer to a Standard SS MAC.....	11
Figure 2-1 RRAP Packet Types.....	23
Figure 3-1 Bit Ordering.....	31
Figure 3-2 Byte Ordering.....	31
Figure 3-3 Byte Ordering in a 2 LANE Configuration.....	32
Figure 3-4 Byte Ordering in a 4 LANE Configuration.....	32
Figure 3-5 Two examples of Logical Idle insertion in a 4x LANE configuration.....	33
Figure 3-6 Example of SKP Insertion in a 4x LANE Configuration.....	35
Figure 3-7 SSIC LTSSM state diagram .....	40
Figure 3-8 SS.Disabled state .....	41
Figure 3-9 Rx.Detect Sub-state Machine.....	42
Figure 3-10 Polling Sub-state Machine.....	44
Figure 3-11 U0 Sub-state Machine .....	47
Figure 6-1 MPHY.TEST Overview .....	55
Figure 6-2 Example of an MPHY.TEST Block.....	56
Figure 6-3 Receive BURST Test Sequence .....	56



## Tables

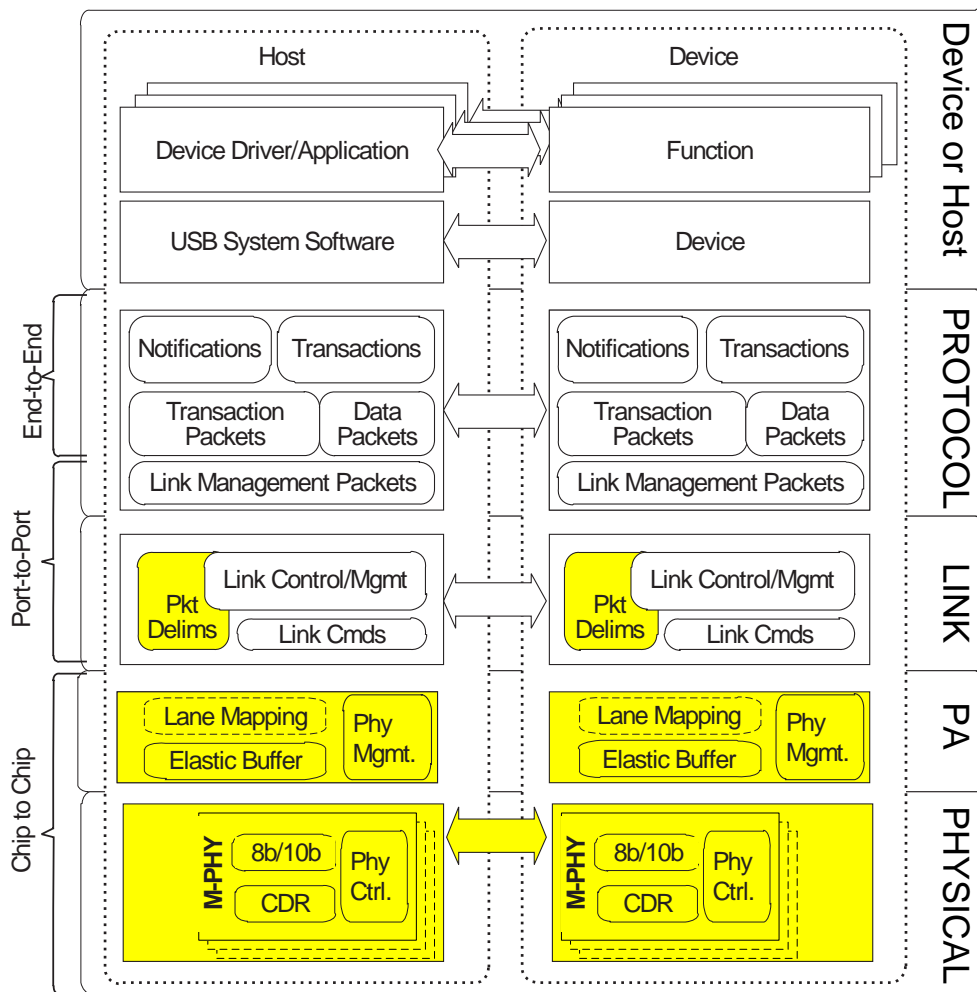
Table 2-1 Multi-LANE Parameters .....	15
Table 2-2 M-TX Capability Attributes .....	16
Table 2-3 M-RX Capability Attributes.....	18
Table 2-4 TX Configuration Attributes.....	21
Table 2-5 RRAP Address Map.....	24
Table 2-6 RRAP Timing Parameters .....	30
Table 3-1 Mapping of SS Control Symbols.....	33
Table 3-2 Link Layer Timing Parameter.....	38
Table 4-1 Protocol Timing Parameters .....	51
Table 5-1 Disconnect Timing Parameters.....	54
Table 6-1 MPHY.TEST Block Registers .....	59

# 1 Introduction

USB is the ubiquitous peripheral-interconnect of choice for a large number of computing and consumer applications. Many systems provide a comprehensive set of software drivers to support commonly available USB peripherals. In addition there is an existing USB ecosystem that includes USB silicon suppliers, design IP houses and verification and testing vendors that lowers the cost for product manufacturers of USB hosts and peripherals.

These advantages have made USB attractive as a chip-to-chip interconnect within a product (without use of cables or connectors). This usage has been validated by the adoption of the High Speed Inter-Chip Supplement [HSIC] in mobile platforms. HSIC leveraged the benefits of High Speed USB while optimizing the link for power, cost and complexity. However the 480 Mbps bandwidth limitation of HSIC poses a limitation for the next generation of applications that require higher bandwidth.

The USB 3.0 specification adds support for transfer speeds of 5 Gbps to address the need for higher bandwidth. However the USB3.0 specification as-is does not meet the requirements of embedded inter-chip interfaces with respect to power and EMI robustness. To address this need, this supplement describes Super Speed Inter-Chip (SSIC) as an optimized inter-chip version of USB3.0.



**Figure 1-1 SSIC Layers with modifications from [USB3.0] highlighted**

As shown in Figure 1-1, SSIC uses the MIPI M-PHY specification as the physical layer of the interconnect to meet the requirements of embedded inter-chip interfaces. The MIPI M-PHY [M-PHY]

20 specification describes a serial physical layer technology with high bandwidth capabilities, which is  
 21 specifically developed for mobile applications to obtain low pin count combined with very good power  
 22 efficiency.

### 23 1.1 SSIC Significant Features

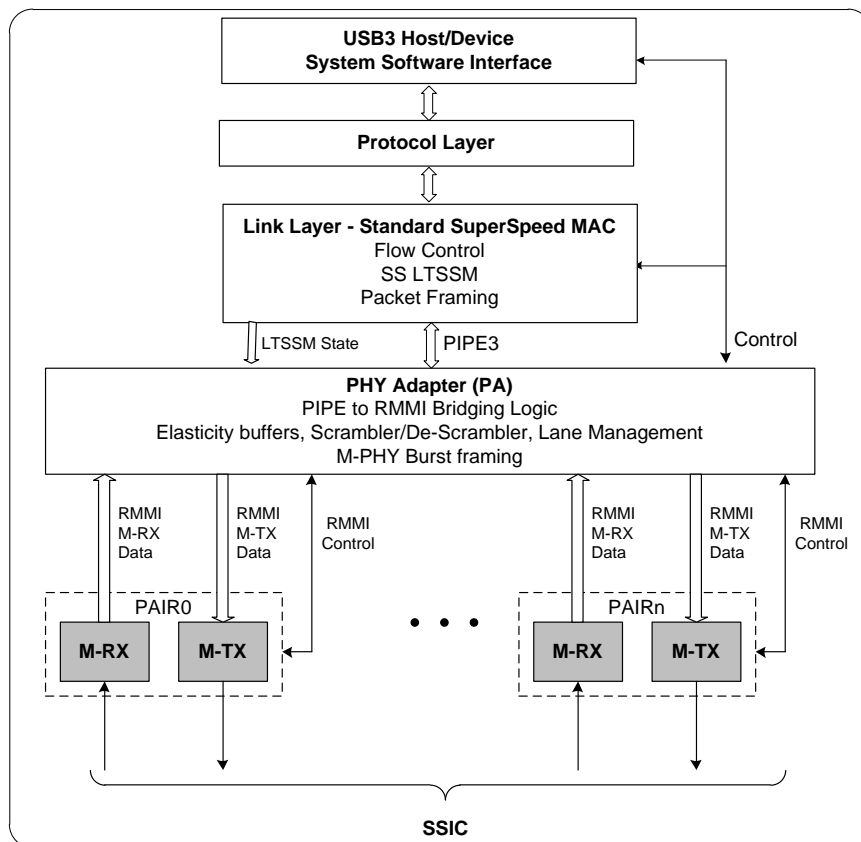
24 The following summarizes the key features of SSIC:

- 25 • Support for the SuperSpeed protocol only as defined in [USB 3.0]
- 26 • Optimized for power, area, cost and EMI robustness for embedded inter-chip interfaces
- 27 • Compliant with the Type-I M-PORTs from the MIPI M-PHY specification [M-PHY]
- 28 • Support for x1, x2 and x4 LANE configurations.

29 This supplement only focuses on peripherals that are directly attached to hosts. Support for hubs is not  
 30 defined and may be achieved in an implementation-specific manner.

### 31 1.2 SSIC and Standard SuperSpeed Comparison

32 SSIC has been designed to replace a standard SuperSpeed Controller and PHY with an implementation  
 33 that maps the SuperSpeed controller on the MIPI M-PHY. **This supplement does not specify details**  
 34 **of any particular implementation** and it is intended that SSIC be implementable in multiple ways,  
 35 depending on what is appropriate for a particular product.



36  
 37 **Figure 1-2 Example of an implementation with a PHY Adapter Layer to a Standard SS MAC**

38 Figure 1-2 shows an example of an SSIC implementation that leverages a standard SuperSpeed  
 39 controller with minimal modifications in the link layer and above. All specifics related to SSIC including  
 40 bridging logic between the PIPE3 interface of the controller and the Reference M-PHY MODULE

41 Interface (RMMI) of the M-PHY are contained in the PHY Adapter (PA). In such an implementation, it is  
 42 necessary for the PHY Adapter to implement whatever mechanisms are needed to allow the controller to  
 43 operate as if it were connected to a SuperSpeed link, for example by tracking the Link Training Status  
 44 State Machine (LTSSM) and providing the expected responses on the link. Other alternatives to this  
 45 example may also be designed that are compliant to this supplement.

46

47 **1.3 Related Documents**

48 This is not a stand-alone document. It is a supplement to [USB 3.0]. Any aspects of USB which are not  
 49 specifically changed by this supplement are governed by [USB 3.0].

50 The following referenced documents can be found on the USB-IF website www.usb.org:

- [USB 3.0]                      *Universal Serial Bus Revision 3.0 Specification including ECNs*
- [HSIC]                         *High Speed Inter-Chip USB Electrical Specification including ECNs*

51

52 The following referenced documents are published by the MIPI Alliance:

- [M-PHY]                      *MIPI® Alliance Specification for M-PHY<sup>SM</sup> Version 3.0*
- [CTS]                         *MIPI M-PHY Conformance Test Suite*

53

54 **1.4 Terminology**

55 “Shall” is normative and used to indicate mandatory requirements which are to be followed strictly in  
 56 order to conform to this standard.

57 “Should” is normative and used to indicate a recommended option or possibility.

58 “May” is normative and used to indicate permitted behavior.

59 “Can” is informative and used to indicate behavior which is possible or may be seen

60 The use of “must” and “will” is deprecated for requirements and shall only be used for statements of fact.

61

62 **1.5 Acronyms and Terms**

63 This section lists and defines terms and abbreviations used throughout this specification.

64 Acronyms and Terms defined in [USB 3.0] and [M-PHY] are not reproduced here. Except where explicitly  
 65 noted, when there is a terminology conflict between the [USB 3.0] and [M-PHY] specifications, the [USB  
 66 3.0] definition is used in this document.

Acronym/Term	Description
DSP	DownStream Port (DSP) refers to the port of a host to which a peripheral is connected.

<b>Link</b>	Refers to the Link Layer as defined in [USB 3.0]. To be distinguished from “M-PHY LINK”.
<b>M-PHY LINK</b>	Refers to LINK as defined in [M-PHY] .
<b>PA</b>	PHY Adapter (PA). Term that refers to logic that interfaces the link layer with the M-PHY.
<b>PAIR</b>	A PAIR consists of a LANE in the downstream SUB-LINK and a counterpart LANE in the upstream SUB-LINK.
<b>RRAP</b>	Remote Register Access Protocol (RRAP) is used while in the PWM-BURST LS-MODE of operation.
<b>SSIC</b>	SuperSpeed Inter-Chip.
<b>USP</b>	UpStream Port (USP) refers to the port that a peripheral uses to connect to a host.

## 68 2 Adaptation of M-PHY for the Physical Layer

69 This document references the MIPI M-PHY [M-PHY] specification for the definition of the physical layer.  
70 This section includes an overview of the relevant M-PHY features, defines required M-PHY capabilities  
71 and describes functionality while in the [M-PHY] LS-MODE of operation.

### 72 2.1 M-PHY for SSIC Overview

73 The following summarizes relevant M-PHY features:

- 74 • Requirement to implement Type-I M-PHY
- 75 • Support for PWM-G1 and HS-G1/G2/G3 BURST mode operation
- 76 • SSIC profile definitions to aid in inter-operability of M-PHYs in SSIC implementations
- 77 • M-PHY SAVE states mapped appropriately to SuperSpeed link states
- 78 • Compliant to M-PHY Symbol coding (8b10b) engine for spectral conditioning and clock recovery
- 79 • Ability to operate with shared and non-shared reference clocks.

#### 80 2.1.1 M-PHY Architecture and the Definition of PAIRs

81 The architecture of the M-PHY is defined in terms of LANEs, SUB-LINKs and LINKs. The M-PHY LINK  
82 shall comply with the following:

- 83 • The two SUB-LINKs of an SSIC implementation shall support the same number of LANEs.
- 84 • All LANEs in the M-PHY LINK shall enter and exit HIBERN8 simultaneously.

85 In addition this supplement defines the concept of a PAIR.

86 A LANE in the downstream SUB-LINK and a counterpart LANE in the upstream SUB-LINK are together  
87 referred to as a PAIR. A multi-LANE implementation consists of multiple PAIRs and shall have a specific  
88 PAIR be statically pre-determined as PAIR0. A single-LANE implementation shall consist of only one  
89 PAIR which shall be PAIR0.

## 90 2.2 M-PHY MODULE Capabilities

91 The M-PHY specification defines capability, configuration and status attributes for an M-TX and for an M-  
92 RX MODULE. Capability attributes describe the capability of M-PHY MODULEs and may vary  
93 depending on the implementation.

94 To aid in the inter-operability of devices, this document defines profiles within which specific M-PHY  
95 Capabilities are mandated.

### 96 2.2.1 Profile Definitions

97 Profiles are indicated by jointly specifying the speed, the multi-LANE capabilities and the rate series such  
98 as:

99 SSIC-G $g$ rL $l$  where

- 100 •  $g = 1, 2$  or  $3$  and indicates the specific HS-GEAR that the M-PHY LINK operates in
- 101 •  $r = A$  or  $B$  and indicates the Rate Series that the M-PHY LINK operates in
- 102 •  $l = 1, 2$  or  $4$  and indicates the number of LANEs active in each SUB-LINK (See Section 2.2.2)

103 All lanes in an implementation shall only operate at the HS-GEAR that corresponds to the profile that is  
104 supported. An implementation is permitted to support one or more profiles, however the combination of  
105 different profiles supported by a specific implementation are out of scope of this specification. For  
106 example: an SSIC-G2A-L1 may or may not choose to support SSIC-G1B-L1.

107 An implementation of a profile shall support the corresponding speed, multi-LANE and mandated  
 108 capabilities of the M-TX and M-RX MODULEs as specified in Section 2.2.3.

109 Certain M-PHY MODULE configurations attributes are chosen not based on the choice of profile or the  
 110 mandate of this document but instead are based on implementation-specific constraints. A complete list  
 111 of such parameters is specified in Section 2.3.

112 **2.2.2 Multi-LANE Capabilities**

113 An implementation may choose to feature one (x1), two (x2) or four (x4) LANEs in each SUB-LINK.

114 The HS-TX LANE-to-LANE skew shall be established by the receipt of a MK0 symbol at the start of a  
 115 HS-Burst. Receivers shall accept LANE-to-LANE skew up to the allowed limit.

116 For multi-LANE M-PHY LINKs, Table 2-1 specifies the required timing parameters.

117 **Table 2-1 Multi-LANE Parameters**

Symbol	Parameter	Value	Comments
T <sub>L2L_SKEW_HS_TX</sub>	Permitted skew between any two LANEs measured at the M-TX's pins	1300ps	To be measured by the receipt of MK0 at the start of a HS-BURST and as defined in Section 5.1.2.4 of [M-PHY]
T <sub>L2L_SKEW_HS_RX</sub>	Permitted skew between any two LANEs measured at the receiver's pins	4000ps	

118

119 **2.2.3 M-TX and M-RX Capabilities**

120 An implementation shall ensure that the local and remote M-PORTs are configured to the selected  
 121 profile. M-PORTs are required to support the M-TX and M-RX capabilities required in this section.

122 Table 2-2 and Table 2-3 define the set of capabilities that are mandated for M-TX and M-RX MODULEs  
 123 respectively. The tables list attributes for which this supplement imposes specific requirements.  
 124 Attributes defined by [M-PHY] which are not specified by this supplement may be set to implementation-  
 125 specific values.

126

127

128

Table 2-2 M-TX Capability Attributes

Attribute	AttrID	Description	M-PHY range	Required Value
TX_HSMODE_Capability	0x01	Specifies support for HS-MODE.	0=no 1=yes	1
TX_HSGEAR_Capability	0x02	Specifies supported HS-GEARS.	1=HS-G1 2=HS-G1/G2 3=HS-G1/G2/G3	≥1 for SSIC-G1 ≥2 for SSIC-G2 =3 for SSIC-G3
TX_PWMGEAR_Capability	0x04	Specifies support for PWM-GEARs other than PWM-G0.	PWM_G1_ONLY = 1, PWM_G1_TO_G2 = 2, PWM_G1_TO_G3 = 3, PWM_G1_TO_G4 = 4, PWM_G1_TO_G5 = 5, PWM_G1_TO_G6 = 6, PWM_G1_TO_G7 = 7	≥ 1
TX_Amplitude_Capability	0x05	Specifies supported signal amplitude levels.	1=SA 2=LA 3=SA and LA	3 = SA and LA. Both options supported.
TX_ExternalSYNC_Capability	0x06	Specifies support for external SYNC pattern.	0=no 1=yes	≥ 0
TX_HS_Unterminated_LINE_Drive_Capability	0x07	Specifies whether or not M-TX supports driving an unterminated LINE in HS-MODE.	0=no 1=yes	≥ 0
TX_LS_Terminated_LINE_Drive_Capability	0x08	Specifies whether or not M-TX supports driving a terminated LINE in LS-MODE.	0=no 1=yes	≥ 0
TX_Min_SLEEP_NoConfig_Time_Capability	0x09	Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed.	1 to 15	≤ 15



Attribute	AttrID	Description	M-PHY range	Required Value
TX_Min_STALL_NoConfig_Time_Capability	0x0A	Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed.	1 to 255	$\leq 8$
TX_Min_SAVE_Config_Time_Capability	0x0B	Specifies minimum reconfiguration time (in 40 ns steps). This applies only to SLEEP and STALL states.	1 to 250 (10000 ns)	$\leq 125$ (5000 ns)
TX_REF_CLOCK_SHARED_Capability	0x0C	Specifies support for a shared reference Clock.	0 = no 1 = yes	$\geq 0$
TX_PHY_MajorMinor_Release_Capability	0x0D	Specifies the major and minor numbers of the M-PHY version supported by the M-TX.	Major version 0 to 9 Minor version 0 to 9	Based on M-PHY Spec Rev in Section 1.3
TX_PHY_Editorial_Release_Capability	0x0E	Specifies the sequence number of the M-PHY version supported by the M-TX.	1 to 99	Based on M-PHY Spec Rev in Section 1.3
TX_Hibern8Time_Capability	0x0F	Specifies minimum time (in 100 $\mu$ s steps) in HIBERN8 state.	1 to 128 (100 $\mu$ s to 12.8 ms)	1 (100 $\mu$ s)
TX_Advanced_Granularity_Capability	0x10	Support and degree of fine granularity steps for a reduced time in HIBERN8 state. If a finer granularity is specified, all coarser granularities shall be supported.	Step size b00 = 4 $\mu$ s, b01 = 8 $\mu$ s, b10 = 16 $\mu$ s, b11 = 32 $\mu$ s Supports fine granularity steps: No = 0 (100 $\mu$ s step), Yes = 1	Step Size No Requirement defined.  Supports fine granularity steps: $\geq 0$
TX_Advanced_Hibern8Time_Capability	0x11	Specifies minimum time in HIBERN8 state when advanced granularity is supported in steps defined by TX_Advanced_Granularity_Capability. Existence depends on: TX_Advanced_Granularity_Capability	1 to 128	No Requirement defined.

Attribute	AttrID	Description	M-PHY range	Required Value
TX_HS_Equalizer_Setting_Capability	0x12	Support for transmit path de-emphasis for HS-MODE Existence depends on: <i>TX_HSMODE_Capability</i>	B[0] = 0: De-emphasis of 3.5dB not supported, B[0] = 1; De-emphasis of 3.5dB supported, B[1] = 0; De-emphasis of 6dB not supported, B[1] = 1; De-emphasis of 6dB supported	B[0] ≥ 0 B[1] ≥ 0

130

Table 2-3 M-RX Capability Attributes

Attribute	AttrID	Description	M-PHY Range	Required Value
RX_HSMODE_Capability	0x81	Specifies support for HS-MODE.	0=no 1=yes	1=yes
RX_HSGEAR_Capability	0x82	Specifies supported HS-GEARs.	1=HS-G1 2=HS-G1/G2 3=HS-G1/G2/G3	≥1 for SSIC-G1 ≥2 for SSIC-G2 =3 for SSIC-G3
RX_PWMGEAR_Capability	0x84	Specifies support for PWM-GEARs other than PWM-G0.	PWM_G1_ONLY = 1, PWM_G1_TO_G2 = 2, PWM_G1_TO_G3 = 3, PWM_G1_TO_G4 = 4, PWM_G1_TO_G5 = 5, PWM_G1_TO_G6 = 6, PWM_G1_TO_G7 = 7	≥ 1
RX_HS_Unterminated_Capability	0x85	Specifies support for disconnection of resistive termination in HS-MODE.	0=no 1=yes	0 = no for all profiles
RX_LS_Terminated_LINE_Drive_Capability	0x86	Specifies support for enabling resistive termination in LS-MODE.	0=no 1=yes	≥ 0
RX_Min_SLEEP_NoConfig_Time_Capability	0x87	Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed.	1 to 15	≤ 15

Attribute	AttrID	Description	M-PHY Range	Required Value
RX_Min_STALL_NoConfig_Time_Capability	0x88	Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed.	1 to 255	≤ 8 <i>Please see Note 1.</i>
RX_Min_SAVE_Config_Time_Capability	0x89	Specifies minimum reconfiguration time (in 40 ns steps). This applies only to SLEEP and STALL states.	1 to 250 (10000 ns)	≤ 125 (5000 ns)
RX_REF_CLOCK_SHARED_Capability	0x8A	Specifies support for a shared reference Clock.	0=no 1=yes	≥ 0
RX_HS_G1_SYNC_LENGTH_Capability	0x8B	HS-G1 Synchronization pattern length in SI.	{Sync range, Sync Length}	≤ {1,4}
RX_HS_G1_PREPARE_LENGTH_Capability	0x8C	HS-G1 prepare length multiplier for M-RX	0 to 15	≤ 4
RX_LS_PREPARE_LENGTH_Capability	0x8D	PWM-BURST or SYS-BURST PREPARE length multiplier for M-RX.	0 to 15	≤ 8
RX_PWM_Burst_Closure_Length_Capability	0x8E	Specifies minimum burst closure time (in SI) necessary to guarantee complete data processing inside M-RX.	0 to 31	≤ 16
RX_Min_ActivateTime_Capability	0x8F	Specifies minimum activate time needed in 100us steps	1 to 9	1
RX_PHY_MajorMinor_Release_Capability	0x90	Specifies the major and minor numbers of the M-PHY version supported by the M-RX.	Major version 0 to 9 Minor version 0 to 9	Based on M-PHY Spec Rev in Section 1.3
RX_PHY_Editorial_Release_Capability	0x91	Specifies the sequence number of the M-PHY version supported by the M-RX.	1 to 99	Based on M-PHY Spec Rev in Section 1.3
RX_Hibern8Time_Capability	0x92	Specifies minimum time (in 100 μs steps) in HIBERN8 state.	1 to 128 (100 μs to 12.8 ms)	1 (100 μs)
RX_HS_G2_SYNC_LENGTH_Capability	0x94	HS-G2 Synchronization pattern length in SI.	{Sync range, Sync Length}	≤ {1,5}

Attribute	AttrID	Description	M-PHY Range	Required Value
RX_HS_G3_SYNC_LENGTH_Capability	0x95	HS-G3 Synchronization pattern length in SI.	{Sync range, Sync Length}	≤ {1,6}
RX_HS_G2_PREPARE_LENGTH_Capability	0x96	HS-G2 prepare length multiplier for M-RX	0 to 15	≤ 4
RX_HS_G3_PREPARE_LENGTH_Capability	0x97	HS-G3 prepare length multiplier for M-RX	0 to 15	≤ 4
RX_Advanced_Granularity_Capability	0x98	Support and degree of fine granularity steps for THIBERN8 and TACTIVATE.	Step size b00 = 4 μs, b01 = 8 μs, b10 = 16 μs, b11 = 32 μs  Supports fine granularity steps No = 0 (100 μs step), Yes = 1	Step Size No Requirement defined.  Supports fine granularity steps: ≥ 0
RX_Advanced_Hibern8Time_Capability	0x99	Specifies minimum time in HIBERN8 state when advanced granularity is supported in steps defined by RX_advanced_Granularity_Capability. Existence depends on: RX_Advanced_Granularity_Capability	1 to 128	No Requirement defined.
RX_Advanced_Min_ActivateTime_Capability	0x9A	Specifies minimum activate time when advanced granularity is supported in steps defined by RX_Advanced_Granularity_Capability. Existence depends on: RX_Advanced_Granularity_Capability	1 to 14	No Requirement defined.

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132  
133  
134

**Note 1:** [M-PHY] requires an RMMI based M-RX to output at least two cycles of RX\_SymbolClk after the end of a HS-BURST. An M-RX cannot exit STALL to start a new HS-BURST until after it has output two cycles of RX\_SymbolClk from the previous HS-BURST. Depending on the width of RX\_Symbol (ie 10/20/40 bits), two cycles of RX\_SymbolClk may be either 2, 4 or 8 SIs. For an RX\_Symbol width of 40 bits, the M-RX needs to remain in stall for at least 8 SIs before the start of the next burst.

135

136

### 2.3 M-PHY Configuration Attributes

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140

As noted in Annex D.2 in [M-PHY] , M-TX Configuration attributes shall be set appropriately to match the corresponding M-RX capability attribute values. Depending on the profile supported by the implementation, default values for the configuration attributes for the M-TX and M-RX MODULE shall be suitably chosen and configured by implementations. Optimizations to the default values for the configuration attributes may be applied in an implementation-specific manner. For more details on the configuration attributes please refer to [M-PHY]

141

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144

However there are some M-PHY configuration attributes listed in Table 2-4 that are not based on the profile but are instead configured depending on implementation considerations. This section makes note of these implementation-specific configuration parameters. This supplement does not specify recommended values for these parameters and does not mandate a mechanism for configuring and coordinating the values of these parameters across the M-PHY LINK.

145

**Table 2-4 TX Configuration Attributes**

Attribute	AttrID	Description	M-PHY range	Required Value
TX_HS_SlewRate	0x26	Slew Rate control of M-TX output driver.	0 to 255	Depending on implementation.
TX_DRIVER_POLARITY	0x2F	M-TX output driver polarity.	NORMAL = 0, INVERTED = 1	Depending on implementation.

## 146 **2.4 M-PHY State Machine**

147 This supplement is in compliance with the State Machine for Type-I MODULEs as described in Figure 7  
148 for M-TX and Figure 8 for M-RX in [M-PHY].

149 However the following is to be noted:

- 150 • The LINE-CFG states are not required for SSIC implementations.
- 151 • Optical Media Converters are not supported.

152 Details regarding the mapping of the SSIC Link Training and Status State Machine (LTSSM) on the M-  
153 PHY Type-I state machines are provided in Section 3.8.

## 154 **2.5 LS-MODE Support**

155 The M-TX and M-RX MODULEs enter the LS-MODE of operation following events such as a power-on-  
156 reset, a warm reset, a USP disconnect or a DSP disconnect. Section 3.8 includes further details on the  
157 link layer conditions for entering LS-MODE.

158 The only PWM-GEAR that is used in a PWM-BURST is PWM-G1. The Remote Register Access Protocol  
159 (RRAP) defined in Section 2.5.2 shall be implemented for data transmission in this mode.

160 Data transmission in a PWM-BURST shall take place in one of the following scenarios:

- 161 • In the Rx.Detect LTSSM state between a USP and a DSP or
- 162 • in the MPHY.TEST LTSSM state when the USP or DSP operates as a DUT under the control of  
163 external Test Equipment.

164 The following section details the entry conditions for PWM-BURST in the Rx.Detect state. For details on  
165 the entry requirements in the MPHY.TEST state please refer to Section 6.2.

### 166 **2.5.1 PWM-BURST Entry in Rx.Detect**

167 Upon entering the Rx.Detect LTSSM state and the LS-MODE sub-state as described in Section 3.8.2, a  
168 DSP and an USP shall:

- 169 • Disable Support for LCCs in the M-TX for all PAIRs.
- 170 • Initiate a PWM-BURST as defined in this section.

#### **Implementation Note:**

*As per [M-PHY] disabling support for LCC requires configuring a value of "NO = 0" to the LCC\_ENABLE Configuration Attribute in the Effective Bank and subsequently asserting the TX\_CfgUpdt signal of the M-TX for all PAIRs.*

171

172 The DSP shall initiate a PWM-BURST as per [M-PHY] on the M-TX MODULE of PAIR0. The DSP shall  
173 then monitor the M-RX of PAIR0 for the USP to initiate a PWM-BURST.

174 The USP shall initiate a PWM-BURST as per [M-PHY] on the M-TX MODULE of PAIR0 after it detects a  
175 PWM-BURST on the M-RX of PAIR0.

176 In a multi-LANE M-PHY LINK the remaining M-TX MODULEs shall remain in the SLEEP state.

177 **2.5.2 Remote Register Access Protocol (RRAP)**

178 While in the PWM-BURST mode, communication is achieved using the RRAP which consists of the  
 179 following packet types:

- 180 • Write Command
- 181 • Write Response
- 182 • Read Command
- 183 • Read Response

184 An RRAP Master shall be capable of issuing Command packets while a RRAP Target shall issue  
 185 response packets.

186

**Write Command**

	P	Rsvd								Data								LowerAddr								UpperAddr								Rsvd		0	0							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0				
Byte	3								2								1								0																			

**Write Response**

	P	Rsvd																																0	1							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0		
Byte	3								2								1								0																	

**Read Command**

	P	Rsvd																LowerAddr								UpperAddr								Rsvd		1	0					
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0		
Byte	3								2								1								0																	

**Read Response**

	P	Rsvd								Data								Rsvd																1	1							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0		
Byte	3								2								1																									

187

188 **Figure 2-1 RRAP Packet Types**

189 The RRAP packets are described in Figure 2-1 along with the following additional requirements:

- 190 • “LowerAddr” and “UpperAddr” values are set based on the address map defined in Table 2-5.
- 191 • The “Rsvd” fields shall not be used and shall be set to 0.
- 192 • The “P” field functions as an odd-parity bit for the entire packet.
- 193 • The entire packet is transmitted continuously without intervening symbols.

194 The following requirements apply to the RRAP:

- 195 • When in PWM-BURST mode and not transmitting a RRAP packet, the M-TX MODULEs in SUB-  
 196 LINKs shall transmit the FLR symbol as per [M-PHY].
- 197 • The RRAP follows the bit and byte ordering rules defined in Section 3.1.
- 198 • A DSP shall support RRAP Master functionality.

- 199 • When in PWM-BURST, a DSP that supports the optional MPHY.TEST state shall support the receipt  
200 of a Write Command to enable a transition to that state. All RRAP commands received by a DSP in  
201 the MPHY.TEST state shall be processed per RRAP Target functionality.
- 202 • A USP shall only support RRAP Target functionality.
- 203 • Test Equipment shall function as a RRAP Master with either the DSP or the USP as the Device  
204 Under Test (DUT).
- 205 • A DSP serving as a RRAP Master shall only send commands and receive responses on PAIR0.
- 206 • A DSP or an USP serving as a RRAP Target shall support receiving commands over any PAIRx and  
207 shall return a response on the same PAIRx.
- 208 • Test Equipment serving as a RRAP Master may send commands and receive responses on any  
209 PAIR.
- 210 • Upon receiving a Write Command packet, a Target shall transmit the corresponding response  
211 packet within tRRAPTargetResponse. This requirement shall apply for any Write Command received  
212 including Writes to Reserved Registers and Registers that are identified in Table 2-5 as having no  
213 effect.
- 214 • Upon receiving a Read Command packet, a Target shall transmit the corresponding response  
215 packet within tRRAPTargetResponse.
- 216 • If a Master has issued a Command, then the Master shall not retry the Command or issue another  
217 Command until either the Target has provided a Response, or after tRRAPInitiatorResponse has  
218 elapsed.
- 219 • A Target shall map the attributes of all implemented PAIRs to RRAP addresses as defined in Table  
220 2-5.
- 221 • A Target shall not send a response until the RRAP Command is fully received with a valid parity.

**Implementation Note:**

*Additional steps to improve the reliability offered by a single parity bit may be taken at the RRAP level using implementation specific means such as redundant write commands or performing reads after writes to ensure the correctness of operations.*

222

223

**Table 2-5 RRAP Address Map**

UpperAddr	LowerAddr	Register Name	Description
0x0	0x00-0xFF	As defined in [M-PHY]	Capability, configuration and status attributes for PAIR0. Writes to these registers shall only affect the shadow bank until an RCT is executed. The Target shall provide a Write Response only after the corresponding Register Write specified in the RRAP Command is committed to the shadow bank.
0x1	0x00-0xFF	As defined in [M-PHY]	Capability, configuration and status attributes for PAIR1. Writes to these registers shall only affect the shadow bank until an RCT is executed. The Target shall provide a Write Response only after the corresponding Register Write specified in the RRAP Command is committed to the shadow bank.



UpperAddr	LowerAddr	Register Name	Description
0x2	0x00-0xFF	As defined in [M-PHY]	Capability, configuration and status attributes for PAIR2. Writes to these registers shall only affect the shadow bank until an RCT is executed. The Target shall provide a Write Response only after the corresponding Register Write specified in the RRAP Command is committed to the shadow bank.
0x3	0x00-0xFF	As defined in [M-PHY]	Capability, configuration and status attributes for PAIR3. Writes to these registers shall only affect the shadow bank until an RCT is executed. The Target shall provide a Write Response only after the corresponding Register Write specified in the RRAP Command is committed to the shadow bank.
0x4	0x00	DSP_DISCONNECT	<p>This Register is used by a DSP following a LINE-RESET to signal a DSP Disconnect. This bit is required only for an USP only. A DSP or a USP in the MPHY.TEST state shall ignore writes to this register.</p> <p>Read/Write Attributes:</p> <ul style="list-style-type: none"> <li>• R/W</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>• 0x00</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>• Writing 1'b1 signals a DSP disconnect as detailed in Section 5.1.2.</li> <li>• Writing 1'b0 shall have no effect.</li> </ul> <p>Once the bit is set, it shall only be reset via a LINE-RESET issued either by a DSP (as part of Warm Reset) or by Test Equipment.</p> <p>Bit [7:1] Reserved.</p> <ul style="list-style-type: none"> <li>• Writes shall be ignored and Reads shall return zero values.</li> </ul>
0x4	0x01	CONFIGURE_FOR_HS	This Register is used to direct the Target to update its shadow bank for HS-BURST with the settings that correspond to the SSIC profile supported. As noted in Section 2.2.1 this profile is statically determined and this supplement provides no means for selecting between different profiles if so supported. The Target shall provide a Write Response only after the corresponding Register Write specified in the RRAP Command is committed to the shadow bank.

UpperAddr	LowerAddr	Register Name	Description
			<p>A Master may alternatively choose to not use this register in which case it shall rely on a set of implementation-specific RRAP commands to update the shadow bank of the Target for HS-BURST operation.</p> <p>Read/Write Attributes:</p> <ul style="list-style-type: none"> <li>• R/W</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>• 0x00</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>• Writing 1'b1 directs the Target to update its shadow bank with the settings that correspond to its SSIC profile.</li> <li>• Writing 1'b0 shall have no effect.</li> </ul> <p>Once the bit is set, it shall only be reset via a LINE-RESET issued either by a DSP (as part of Warm Reset) or by Test Equipment.</p> <p>Bit[7:1] Reserved.</p> <ul style="list-style-type: none"> <li>• Writes shall be ignored and Reads shall return zero values.</li> </ul>
0x4	0x02	BURST_CLOSURE	<p>This Register is used to direct the Target to terminate the PWM-BURST.</p> <p>Read/Write Attributes:</p> <ul style="list-style-type: none"> <li>• R/W</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>• 0x00</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>• Writing 1'b1 terminates the PWM-BURST and initiates an RCT to exit LS-MODE as defined in Section 2.5.3.</li> <li>• Writing 1'b0 shall have no effect.</li> </ul> <p>Once the bit is set, it shall only be reset via a LINE-RESET issued either by a DSP (as part of Warm Reset) or by Test Equipment.</p> <p>Bit[7:1] Reserved.</p> <ul style="list-style-type: none"> <li>• Writes shall be ignored and Reads shall return zero values.</li> </ul>
0x4	0x03	DISABLE_SCRAMBLING	<p>This Register is used by a DSP to indicate to an USP that data transmission in HS-MODE shall</p>

UpperAddr	LowerAddr	Register Name	Description
			<p>have scrambling disabled.</p> <p>Read/Write Attributes:</p> <ul style="list-style-type: none"> <li>• R/W</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>• 0x00</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>• Writing 1'b1 configures the USP to disable HS-MODE scrambling.</li> <li>• Writing 1'b0 shall have no effect.</li> </ul> <p>Once the bit is set, it shall only be reset via a LINE-RESET issued either by a DSP (as part of Warm Reset) or by Test Equipment.</p> <p>Bit [7:1] Reserved.</p> <ul style="list-style-type: none"> <li>• Writes shall be ignored and Reads shall return zero values.</li> </ul>
0x4	0x04	DISABLE_STALL_IN_U0	<p>This Register is used by a DSP to disable STALL entry in U0 in an USP. A DSP or a USP in the MPHY.TEST state shall ignore writes to this register.</p> <p>Read/Write Attributes:</p> <ul style="list-style-type: none"> <li>• R/W</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>• 0x00</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>• Writing 1'b1 configures the USP to disable STALL entry while in U0.</li> <li>• Writing 1'b0 shall have no effect.</li> </ul> <p>Once the bit is set, it shall only be reset via a LINE-RESET issued either by a DSP (as part of Warm Reset) or by Test Equipment.</p> <p>Bit [7:1] Reserved.</p> <ul style="list-style-type: none"> <li>• Writes shall be ignored and Reads shall return zero values.</li> </ul>
0x4	0x05	DISABLE_LUP_LDN	<p>This optional Register is used by a DSP to disable the use of the LDN and LUP Link Commands defined in [USB 3.0] to allow additional power optimizations in the M-TX.</p> <p>Read/Write Attributes:</p> <ul style="list-style-type: none"> <li>• R/W</li> </ul> <p>Reset Default:</p>

UpperAddr	LowerAddr	Register Name	Description
			<ul style="list-style-type: none"> <li>• 0x00</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>• Writing 1'b1 configures the USP to disable LUP/LDN commands. In addition, the USP shall not flag a tUOLTimeout Error or transition to Recovery upon detecting a missing LUP or LDN.</li> <li>• A DSP that generates a RRAP command to set this bit shall not transmit any LUP and LDN link commands. In addition, the DSP shall not flag a tUOLTimeout Error or transition to Recovery upon detecting a missing LUP or LDN.</li> <li>• Writing 1'b0 shall have no effect.</li> </ul> <p>Once the bit is set, it shall only be reset via a LINE-RESET issued either by a DSP (as part of Warm Reset) or by Test Equipment.</p> <p>Bit [7:1] Reserved.</p> <ul style="list-style-type: none"> <li>• Writes shall be ignored and Reads shall return zero values.</li> </ul>
0x4	0x05-0xFE	RESERVED	Reserved. Writes shall be ignored and Reads shall return zero values.
0x4	0xFF	TEST_MODE	<p>This Register is used by Test Equipment to configure a Target in the MPHY.TEST state. The Target shall complete its configuration to the MPHY.TEST state prior to issuing a Write Response to the command.</p> <p>Read/Write Attributes:</p> <ul style="list-style-type: none"> <li>• R/W</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>• 0x00</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>• Writing 1'b1 configures the RRAP Target in the MPHY.TEST state.</li> <li>• Writing 1'b0 shall have no effect.</li> </ul> <p>Once the bit is set, it shall only be reset via a LINE-RESET issued either by a DSP (as part of Warm Reset) or by Test Equipment.</p> <p>Bit [7:1] Reserved.</p> <ul style="list-style-type: none"> <li>• Writes shall be ignored and Reads shall return zero values.</li> </ul>

UpperAddr	LowerAddr	Register Name	Description
0x5	0x00	PAIR_CAPABILITY	<p>This Register is used by a Master to determine the number PAIRs supported by a Target.</p> <p>Read/Write Attributes:</p> <ul style="list-style-type: none"> <li>• RO</li> <li>• Writes to this register shall be ignored.</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>• Implementation-specific.</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>• A read of this field shall always return a value of 1'b1</li> </ul> <p>Bit [1]:</p> <ul style="list-style-type: none"> <li>• A read of this field shall return a value of 1'b1 if PAIR0 and PAIR1 are supported.</li> </ul> <p>Bit [2]:</p> <ul style="list-style-type: none"> <li>• A read of this field shall return a value of 1'b1 if PAIR0, PAIR1, PAIR2 and PAIR3 are supported.</li> </ul> <p>Bit [7:3] Reserved.</p> <ul style="list-style-type: none"> <li>• Reads shall return zero values.</li> </ul>
0x5	0x01- 0xFF	RESERVED	Reserved. Writes shall be ignored and Reads shall return zero values.
0x6-0xD	0x00-0xFF	RESERVED	Reserved. Writes shall be ignored and Reads shall return zero values.
0xE	0x00-0xFF	MPHY.TEST Registers	Refer to Section 6.
0xF	0x00-0xFF	VENDOR-SPECIFIC REGISTERS	Registers in this address space are not defined in this specification and are reserved to implement vendor-specific functionality.

224

### 225 2.5.3 PWM-BURST Closure

226 PWM-BURST closure shall be implemented in the following manner:

- 227
- 228
- 229
- 230
- 231
- The Master shall set BURST\_CLOSURE[0] register in the Target.
  - Upon the receipt of a Write Response with a valid parity from the Target, the Master shall end the PWM-BURST on its M-TX.
  - On detecting the closure of the PWM-BURST on its M-RX, the RRAP Target shall end the PWM-BURST on its M-TX.

232 After the closure of the PWM-BURST, the conditions for a Re-Configuration Trigger (RCT) as defined in  
233 [M-PHY] shall be met upon which the Effective bank of the Configuration Attributes are updated.

#### 234 2.5.4 RRAP Timing Parameters

235 This section defines the timing parameters relevant to the RRAP.

236 **Table 2-6 RRAP Timing Parameters**

Name	Description	Min	Max	Units
tRRAPTargetResponse	Time between the receipt of a RRAP command and the transmission of the response by a Target		50	ms
tRRAPInitiatorResponse	Time between the transmission of a RRAP command and the reception of the response by an Initiator		60	ms

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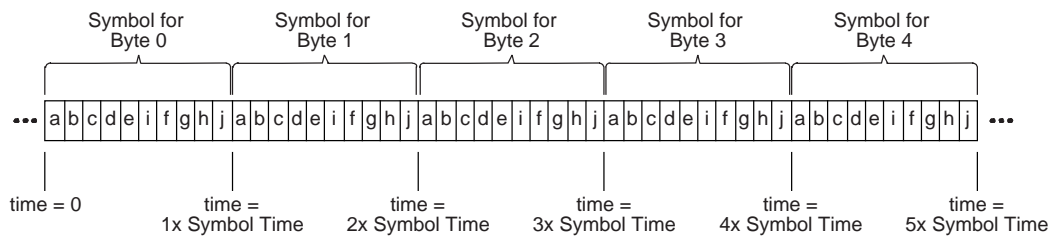
241 **3 Link Layer**

242 This chapter specifies the Link layer including:

- 243 • Reset signaling
- 244 • Bit and byte ordering
- 245 • Packet framing
- 246 • Logical idle
- 247 • SSIC LTSSM and operations
- 248 • Scrambling
- 249 • Clock Compensation

250 **3.1 Bit and Byte Ordering**

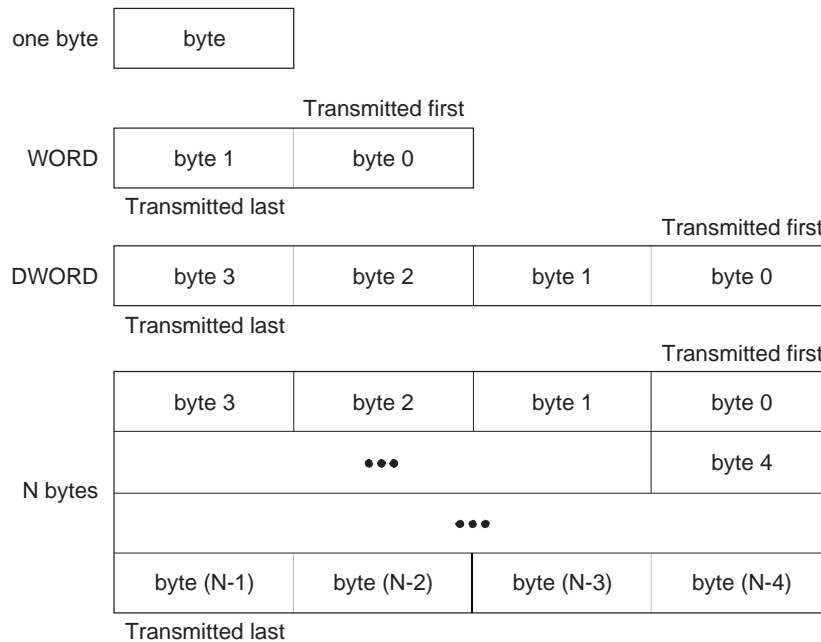
251 Bit ordering shall be big-endian as defined by [M-PHY] and as shown in Figure 3-1.



252

253 **Figure 3-1 Bit Ordering**

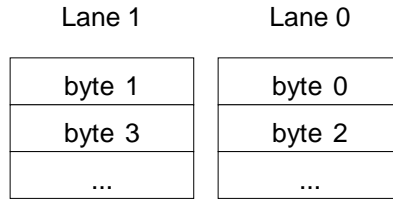
254 In a Single-LANE (x1) implementations, all bytes are transmitted in-order as shown in Figure 3-2.



255

256 **Figure 3-2 Byte Ordering**

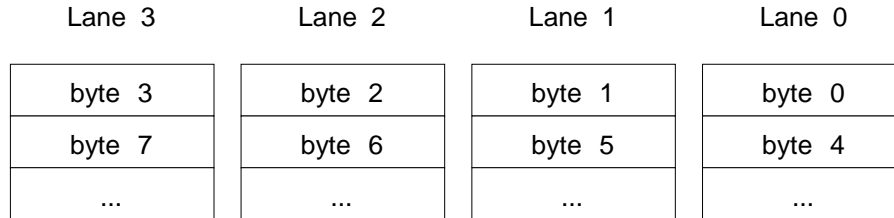
257 In multi-LANE implementations, all bytes are transmitted by mapping them to the multiple lanes as  
 258 shown in Figure 3-3 and Figure 3-4. These rules apply for all packets (including Link Commands, TPs  
 259 and DPs) as well as special symbols such as Training Sets.



260

261

**Figure 3-3 Byte Ordering in a 2 LANE Configuration**



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263

**Figure 3-4 Byte Ordering in a 4 LANE Configuration**

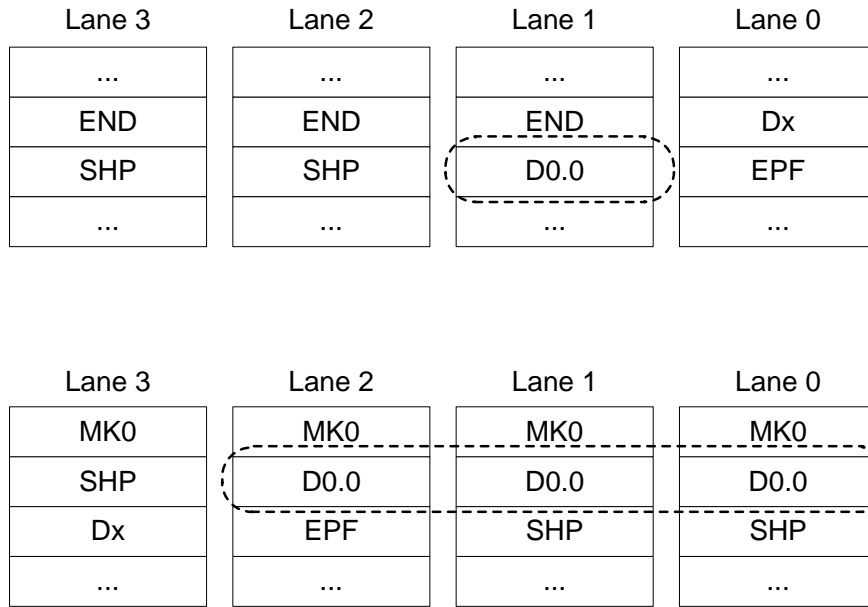
264

### 265 **3.2 Logical Idle and FLR non-insertion**

266 The Logical Idle Symbol D0.0 - scrambled as defined in Section 3.5 – shall be transmitted when the M-  
 267 TX is in the HS-BURST state and no SS packets (Link Commands, TPs or DPs) are being transferred on  
 268 the link. Once started, the transmission of a SS packet shall continue without the insertion of any logical  
 269 idle symbols as per [USB 3.0].

270 In a multi-LANE implementation, the first byte of a SS packet may be placed on any LANE. When  
 271 ending an HS-BURST, if the packet transmission finishes misaligned, logical idle symbols shall be  
 272 transmitted on all remaining LANES. Figure 3-5 presents two examples of D0.0 logical idle transmission  
 273 between packets.





**Figure 3-5 Two examples of Logical Idle insertion in a 4x LANE configuration**

The M-TX shall not insert any FLRs in the transmit stream.

**Implementation Note:** To prevent the M-TX from inserting FLR symbols in the transmit stream, the PA layer needs to always provide symbols for transmission (by always asserting TX\_ProtDORDY during a HS-BURST) and also should ensure the M-TX never throttles transmission by deasserting TX\_PhyDIRDY on the M-PHY RMMI. This may place specific requirements on the clocking implementation of the M-TX such as ensuring that the TX\_BitClk and TX\_SymbolClk are derived from the same reference.

### 3.3 Line Coding

All information communicated in the PWM-BURST and HS-BURST states shall be 8b10b encoded as per the data and control symbols assignments prescribed in [M-PHY] and the symbol mapping assignment described in this section.

Data symbols shall be directly mapped as per the assignment described in [M-PHY].

**Table 3-1 Mapping of SS Control Symbols**

Control Symbols	SS Encoding	SSIC Encoding	M-PHY Usage	Notes
COM	K28.5	K28.5	MARKER0	MK0 sent at start of HS-BURST. Also re-used for COM.
EDB	K28.3	K28.3	MARKER1	MK1 used only for EDB.
SDP	K28.2	K28.6	MARKER2	MK2 used only for SDP - encoding differs from [USB3.0]
EPF	K23.7	K23.7	MARKER3	MARKER3 used only for EPF
SHP	K27.7	K27.7	MARKER4	MARKER4 used for SHP
END	K29.7	K29.7	MARKER5	MARKER5 used for END

SLC	K30.7	K30.7	MARKER6	MARKER6 used for SLC
SKP	K28.1	K28.1	FILLER	FLR used only for SKP.
SUB	K28.4	n/a	n/a	SUB not used in SSIC

284  
285 Table 3-1 describes the mapping of the SS control symbols. As noted most of the the SuperSpeed  
286 control symbols (COM, EPF, SHP, END, SLC, SKP, EDB) are K-encoded as defined in [USB 3.0] with  
287 the one exception (SDP) that has a different K-encoding.

288 The FLR symbol is only used to indicate a SuperSpeed SKP Symbol and implementations shall ensure  
289 that an M-TX shall not independently insert FLRs as noted in Section 3.2.

290 The SUB symbol which is defined in [USB 3.0] for when a decode error is detected does not require a M-  
291 PHY mapping.

292 8b/10b decode errors detected by the M-RX shall be signaled to the link layer using implementation-  
293 specific mechanisms.

294 .

### 295 3.4 Clock Compensation

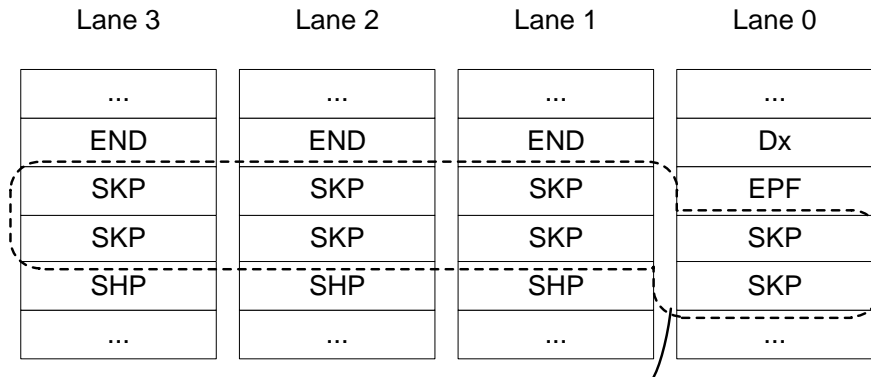
296 The following rules replace those defined in Section 6.4.3. of [USB 3.0]:

- 297 • A SKP Ordered Set shall consist of two SKP symbols transmitted one after the other on a single  
298 LANE.
- 299 • For x2 and x4 M-PHY LINKs, when transmitted, SKP Ordered Sets shall be transmitted on all  
300 LANEs such that the same number of SKP Ordered Sets are transmitted on all LANEs, however  
301 the SKP Ordered Set transmission is permitted to start on any LANE
- 302 • SKP Ordered Sets shall not be transmitted within any packet or Ordered Set.
- 303 • For a x1 M-PHY LINK, while in HS.BURST mode, transmitting TS1 Ordered Set, TS2 Ordered  
304 Set, LMP, TP, DP, or Logical Idle, transmitters shall transmit SKP Ordered Sets such that within  
305 any set of 1416 successively transmitted symbols at least 4 SKP Ordered Sets are transmitted.
- 306 • For a x2 M-PHY LINK, while in HS.BURST mode, transmitting TS1 Ordered Set, TS2 Ordered  
307 Set, LMP, TP, DP, or Logical Idle, transmitters shall transmit SKP Ordered Sets such that within  
308 any set of 708 successively transmitted symbols per LANE at least 2 SKP Ordered Sets are  
309 transmitted.
- 310 • For a x4 M-PHY LINK, while in HS.BURST mode, transmitting TS1 Ordered Set, TS2 Ordered  
311 Set, LMP, TP, DP, or Logical Idle, transmitters shall transmit SKP Ordered Sets such that within  
312 any set of 354 successively transmitted symbols per LANE at least 1 SKP Ordered Set is  
313 transmitted.
- 314 • It is permitted for a transmitter to transmit SKP Ordered Sets more frequently than this minimum  
315 requirement.
- 316 • For x1 M-PHY LINKs, receivers shall be tolerant to receive:
  - 317 ○ no SKP ordered set(s) within a set of as many as 1416 successively received non-SKP  
318 symbols, and
  - 319 ○ as few as 4 SKP Ordered Sets within any set of 1424 successively received SKP and/or  
320 non-SKP symbols.
- 321 • For x2 M-PHY LINKs, receivers shall be tolerant to receive per LANE :
  - 322 ○ no SKP ordered set(s) within a set of as many as 708 successively received non-SKP  
323 symbols, and
  - 324 ○ as few as 2 SKP Ordered Sets within any set of 712 successively received SKP and/or  
325 non-SKP symbols.
- 326 • For x4 M-PHY LINKs, receivers shall be tolerant to receive per LANE :

- 327 ○ no SKP ordered set(s) within a set of as many as 354 successively received non-SKP
- 328 symbols, and
- 329 ○ as few as 1 SKP Ordered Sets within any set of 356 successively received SKP and/or
- 330 non-SKP symbols.
- 331

332 Figure 3-6 shows an example of SKPs between two packet transmissions on a x4 M-PHY LINK.

333



It is permitted that SKPs not align across all lanes, but each lane shall contain same number of SKPs

334

335

**Figure 3-6 Example of SKP Insertion in a 4x LANE Configuration**

336

**Implementation Note:**

When reusing existing SuperSpeed controllers with x2 or x4 M-PHY LINKs, it may be desirable to avoid increasing the number of SKPs transmitted for a given amount of data transferred. However, the requirement that SKP transmissions include the same number of SKPs on all LANEs means that, if, when the controller indicates a SKP transmission, that the transmission is simply replicated across all LANEs, the average number of SKPs transmitted would be increased relative to the amount of data transferred. It is possible to satisfy the above rules and at the same time avoid needlessly increasing the relative number of SKPs transmitted by implementing an algorithm that accumulates SKPs for transmission, such that, for example, on a x2 M-PHY LINK, the transmitter would transmit two SKPs on each LANE, but only at alternate intervals. If the transmit controller already buffered up multiple SKPs, then it is not necessary to implement interval skipping, as this has in effect already been done by the controller.

The recommended algorithm is the following:

- A transmitter should keep a running count of the number of transmitted symbols across all LANEs since the last SKP symbol transmission, referred to as Z.
- Z should be reset to 0 whenever the transmitter enters HS.Burst
- The non-integer remainder of the following Z calculations should not be discarded and shall be used in the calculation to schedule the next SKP symbols
- While transmitting TS1 Ordered Set, TS2 Ordered Set, LMP, TP, DP, or Logical Idle, when the integer result of

$$\frac{Z}{354 * \text{NumberOfLanes}}$$

reaches one, the transmitter should buffer one (additional) SKP Ordered Set to be transmitted on each LANE at the end of the current packet or Ordered Set transmission

337

338 **3.5 Data Scrambling**

339 Data shall be scrambled according to the following rules on a per-LANE basis:

- 340 • Scrambling shall be done using an LFSR applied
- 341 • The LFSR implements the polynomial:  $G(X)=X^{16}+X^5+X^4+X^3+1$
- 342 • The LFSR value shall be advanced eight serial shifts for each Data Symbol and K Code **except**
- 343 for SKP.
- 344 • All 8b/10b D-codes, *including* those within the Training Sequence Ordered Sets shall be
- 345 scrambled.
- 346 • K codes shall not be scrambled.
- 347 • During a HS-BURST the LFSR on the transmit side shall be initialized to FFFFh after the
- 348 transmission of any MK0 symbol.
- 349 • During a HS-BURST the LFSR on the receive side shall be initialized to FFFFh after the receipt
- 350 of any MK0 symbol.
- 351 • Scrambling shall only be applied while in HS-BURST and shall not be used in PWM-BURST.
- 352 • Scrambling can be optionally disabled via the DISABLE\_SCRAMBLING RRAP command as
- 353 described in Section 2.5.2.

**Implementation Note:**

*In the implementation example described in Figure 1-2, this implies that the standard SuperSpeed scrambler is disabled and a scrambler compliant with this section is implemented in the PHY Adapter layer on a per-LANE basis.*

354

355 **3.6 PowerOn Reset and Inband Reset**

356 **3.6.1 PowerOn Reset**

357 PowerOn Reset refers to a condition that shall be defined as the power supply of the port achieving a  
358 steady state, the details of which are implementation specific and not defined by this document.

359 When an implementation is powered and the PowerOn Reset is asserted the SSIC LTSSM shall enter  
360 the SS.Disabled state. On the deassertion of PowerOn Reset, the SSIC LTSSM shall enter the  
361 RX.Detect state.

362 Upon assertion and de-assertion of PowerOn Reset, M-PHY MODULEs shall enter and exit the  
363 DISABLED state as defined in Section 4.7.1.4 of [M-PHY] .

364 **3.6.2 Inband Reset (Hot Reset and Warm Reset)**

365 Both mechanisms of Inband reset defined in [USB 3.0] are supported: Hot Reset and Warm Reset.  
366 However the reset signaling mechanisms are modified to be implemented on top of the M-PHY as  
367 defined in this section.

368 **3.6.2.1 Hot Reset**

369 Hot Reset is signaled by a DSP by sending TS2 ordered sets with the Reset bit asserted. A Hot Reset  
370 shall cause the SSIC LTSSM to transition to the Hot Reset state as described in 3.8.9. Upon completion  
371 of Hot Reset, the following shall occur:

- 372
- 373 • A DSP shall reset its Link Error Count.
  - 374 • The port configuration information of a USP shall remain unchanged.
  - 375 • The M-PHY configuration settings shall remain unchanged.
  - 376 • The LTSSM of a port shall transition to U0.

376 If a Hot Reset fails, the DSP shall signal a Warm Reset as per [USB 3.0].

377 **3.6.2.2 Warm Reset**

378 Warm Reset is signaled by a DSP using the LINE-RESET mechanism defined in [M-PHY] .

379 The operational model of a Warm Reset is as follows:

- 380
- 381 • The DSP shall drive DIF-N on the M-TX of PAIR0 for a period of tResetDIFN.
  - 382 • The DSP shall issue a LINE-RESET on the M-TX of PAIR0.
  - 383 • When a LINE-RESET is signaled, the LTSSM shall transition to the Rx.Detect.Reset state.

384 Signaling a Warm Reset using the LINE-RESET mechanism on any M-TX other than that of PAIR0 has  
385 undefined results. Only a DSP shall issue Warm Reset via the LINE-RESET mechanism. A USP shall  
use the LINE-RESET mechanism to signal a USP disconnect as defined in Section 5.

386 **3.7 Link Layer Timing Requirements**  
 387 Link layer timing requirements shall remain the same as specified in [USB 3.0] except for the parameters  
 388 defined below.

389 **Table 3-2 Link Layer Timing Parameter**

Name	Description	Min	Max	Units
PENDING_HP_TIMER	As described in [USB 3.0]		100	μs
PM_LC_TIMER	As described in [USB 3.0]		100	μs
PM_ENTRY_TIMER	As described in [USB 3.0]		120	μs
tRetrain	Timer to detect improper training of the local and remote M-RX as part of HS-BURST entry. Timer is implemented in the Polling and Recovery LTSSM states as described in Section 3.8.3 and Section 3.8.8.	40	50	μs
tResetDIFN	Period of time a DSP is required to drive a DIF-N prior to a LINE-RESET. Defined to ensure USP is ready to receive the LINE-RESET and to not break Warm Reset timing as defined in [USB 3.0].	60	80	ms
tPollingSTALLResidency	Period of time spent in the Polling.STALL sub-state. Timing values are specified to allow for designs using an existing [USB 3.0] LTSSM as shown in Figure 1 2. Such implementations may require up to two legacy Receiver detection cycles to be performed in this sub-state that may take up to 12 ms each along with some operating margin.		40	ms
tPollingActiveTimeout	As described in [USB 3.0]. Increased from the 12ms value prescribed in [USB 3.0] to account for maximum of 40ms in the Polling.STALL state along with some operating margin.		58	ms
tPortConfiguration	As described in [USB 3.0]. Increased from the 20μs value prescribed in [USB 3.0] to be in sync with the increase to the PENDING_HP_TIMER		110	μs

390

391

### 3.8 SSIC Link Training and Status State Machine (LTSSM)

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393  
394

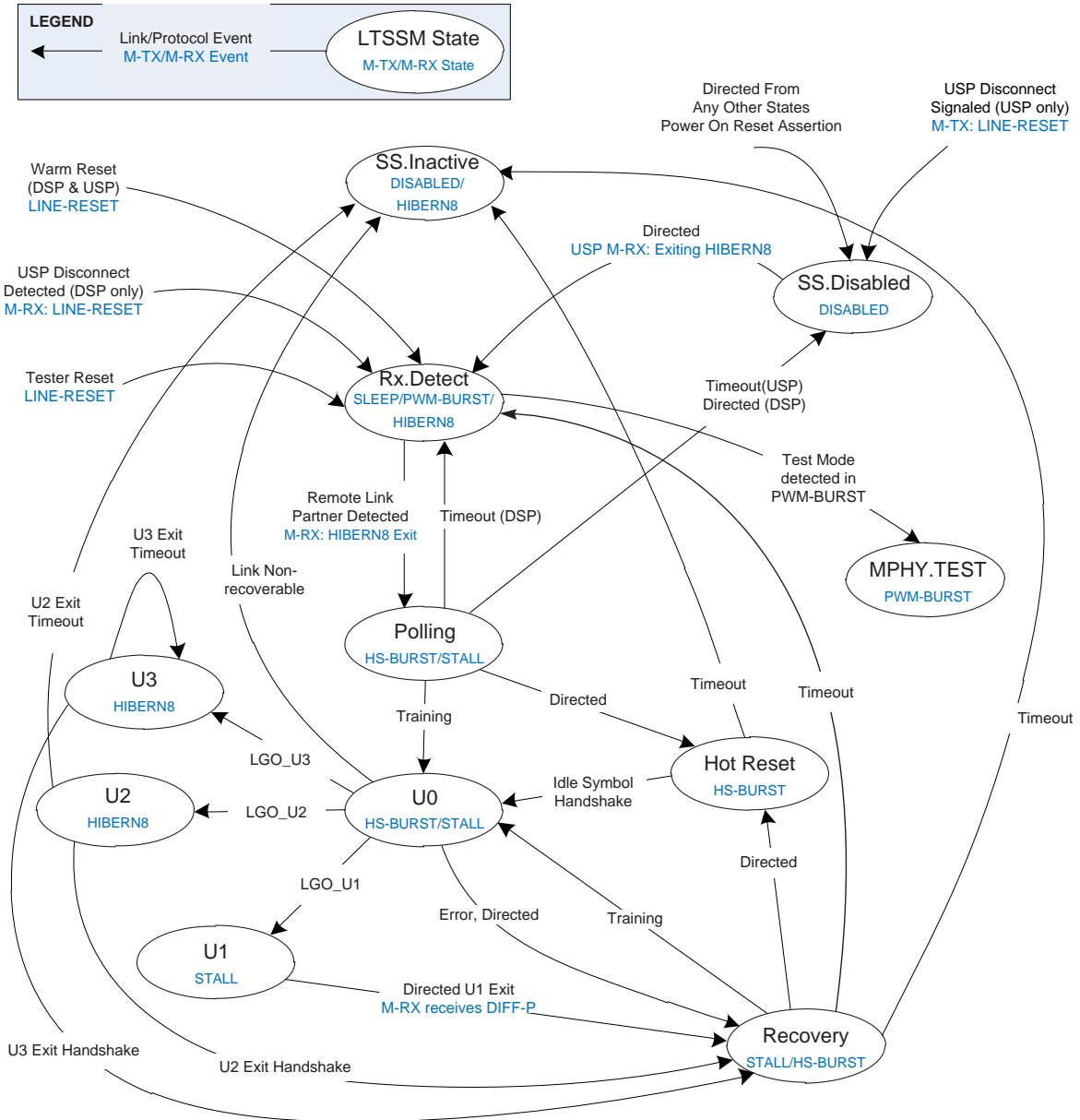
The SSIC Link Training and Status State Machine (LTSSM) of the link layer is shown in Figure 3-7. The figure and following section documents relevant state details, associated transitions and details of the mapping of the LTSSM state to the M-PHY state machines.

395  
396  
397  
398  
399  
400

Unless otherwise noted, requirements for LTSSM states and sub-states defined in [USB 3.0] also apply to this supplement and are not reproduced here. However [USB 3.0] LTSSM requirements corresponding to the physical layer do not apply and instead M-PHY M-TX and M-RX requirements detailed in this section shall be followed. Specifically Low Frequency Periodic Signaling (LFPS) and Receiver Termination Detection and the various signaling mechanisms thereof do not apply to this supplement.

**Implementation Note:** *This section has been specified to allow compliant implementations to be designed using an existing [USB 3.0] compliant LTSSM and a suitable PA layer as shown in Figure 1-2. This does not imply preference for any particular style of implementation, and other implementations are supported, provided they comply to the requirements of this section.*

401



Note: Figure is illustrative only. Not all of the transition conditions are listed. Refer to text for details.

Figure 3-7 SSIC LTSSM state diagram

3.8.1 SS.Disabled

SS.Disabled is a logical power-off state when a port is unpowered or when the SSIC port's functionality is disabled.

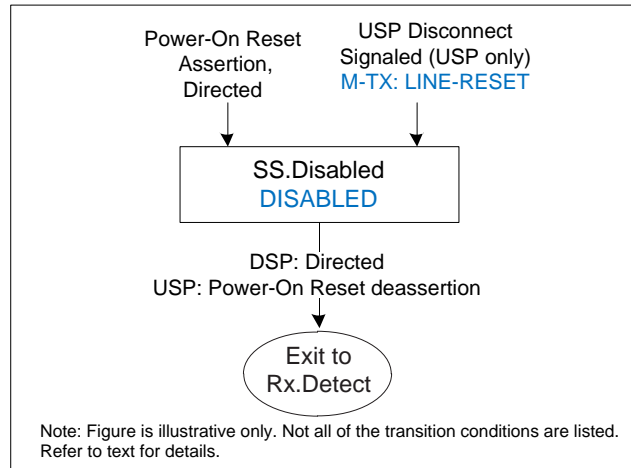
A DSP when directed to do so shall signal a DSP disconnect and transition to this state.

3.8.1.1 SS.Disabled Requirements

The SS.Disabled state does not contain any sub-states as shown in Figure 3-8:



- 411
- 412
- The M-PHY local RESET to the M-RX and M-TX of all PAIRs shall be asserted which maintains the modules in the DISABLED state



413

**Figure 3-8 SS.Disabled state**

414

415 **3.8.1.2 Exit from SS.Disabled**

- 416
- 417
- 418
- 419
- 420
- Exit shall take place for a USP via the deassertion of Power-On Reset and for a DSP when directed to exit:
    - The M-PHY local RESET to the M-RX and M-TX of all PAIRs shall be de-asserted which transitions the modules from the DISABLED to the HIBERN8 state.
    - the LTSSM shall transition to Rx.Detect.Active LTSSM state.

421 **3.8.2 RX.Detect**

422 The Rx.Detect state of the LTSSM is entered in the following scenarios:

- 423
- 424
- 425
- 426
- 427
- 428
- Signaling of a Warm Reset by a DSP
  - Detection of a Warm Reset by a USP
  - Detection of a USP disconnect by a DSP
  - Completion of Power on Reset by both a DSP and USP
  - When Polling or Recovery is unsuccessful for a DSP as defined in [USB 3.0]
  - Signaling of a LINE-RESET by Test Equipment

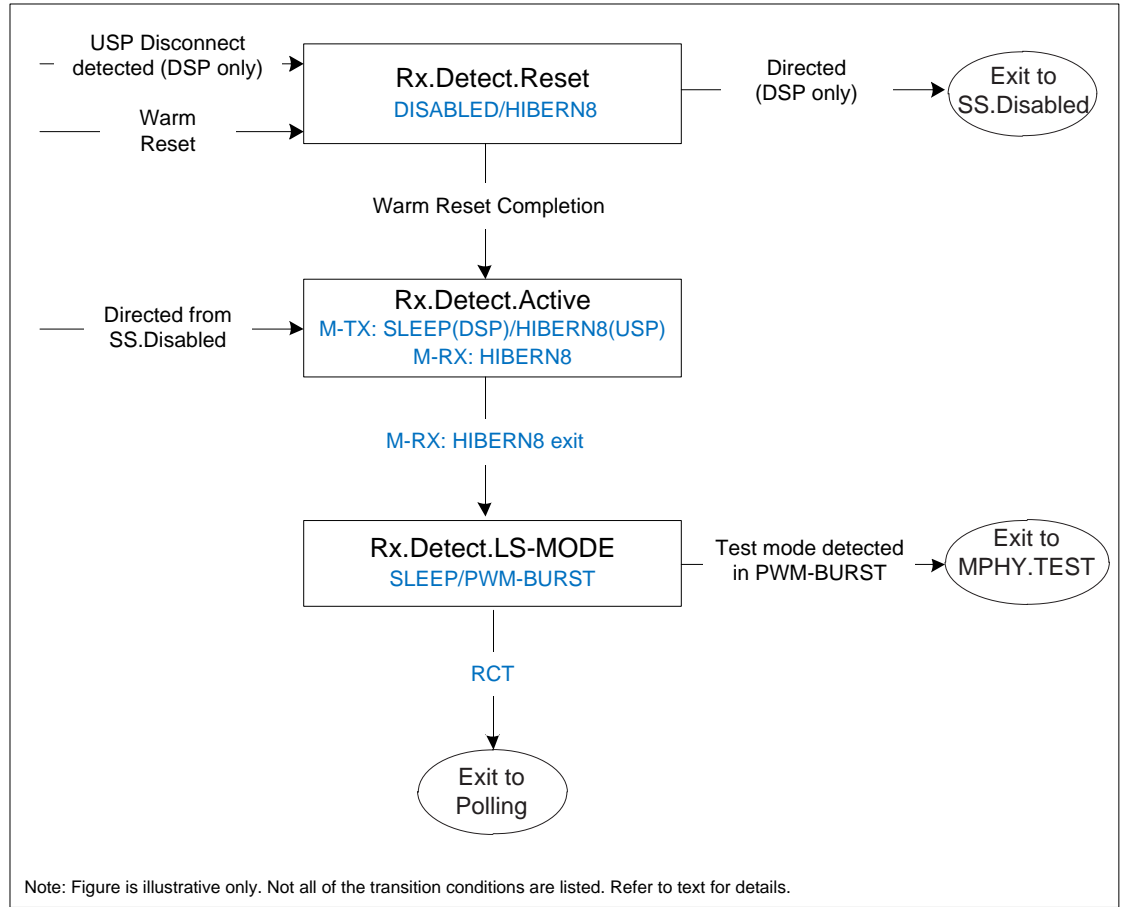
429 The concept of far-end terminations as defined in [USB 3.0] does not apply to this supplement and

430 instead M-PHY based mechanisms shall be used to detect the presence of a link partner and to

431 synchronize operation as defined in this section.

432 Rx.Detect contains a sub-state machine as shown in Figure 3-9 with the following sub-states:

- 433
- 434
- 435
- 436
- Rx.Detect.Reset
  - Rx.Detect.Active
  - Rx.Detect.LS-MODE



437

438

**Figure 3-9 Rx.Detect Sub-state Machine**

439 3.8.2.1 RX.Detect.Reset Requirements

440 This sub-state is entered in following scenarios:

- 441 • LINE-RESET signaled by a DSP as part of Warm Reset as defined in 3.6.2.2 (both USP and
- 442 DSP enter) or
- 443 • LINE-RESET is signaled during a USP disconnect as defined in Section 5.1.1(DSP only enters)
- 444 • LINE-RESET is signaled by Test Equipment
- 445

446 In this sub-state the USP and DSP shall complete the following steps in the following order:

- 447 • Wait for the completion of LINE-RESET signaling.
- 448 • Assert the local M-PHY Reset for all LANEs within Tline\_to\_local\_rst bringing the M-TX and M-
- 449 RX to the DISABLED state on all PAIRs.
- 450 • Keep local M-PHY Reset asserted for Tlocal\_rst
- 451 • De-assert the local M-PHY Reset bringing the M-TX and M-RX to the HIBERN8 state on all
- 452 PAIRs.

453 In the case of a warm reset, a DSP may handle any delays in completion of the above steps by an USP  
454 in an implementation-specific manner.

455 3.8.2.2 Exit from RX.Detect.Reset

- 456
- A port shall transition to Rx.Detect.Active after completing the required steps as defined in
- 457 Section 3.8.2.1.
- A DSP shall transition to SS.Disabled when directed.
- 458

459 3.8.2.3 RX.Detect.Active Requirements

460 Rx.Detect.Active is a sub-state to detect the presence of a link partner.

- 461
- For a DSP:
    - The M-TX shall be configured to exit HIBERN8 into the SLEEP state which results in a
- 462 DIF-N value being driven on all PAIRs.
- The M-RX shall remain in HIBERN8 on all PAIRs until the link partner initiates a
- 463 HIBERN8 exit
- For a USP:
    - The M-TX and M-RX shall remain in HIBERN8 until the link partner initiates a HIBERN8
- 464 exit
- 465
- 466
- 467
- 468

469 3.8.2.4 Exit from RX.Detect.Active

- Upon detection of a HIBERN8 exit on its M-RX on any PAIR the USP shall initiate an exit from
- 470 HIBERN8 on its M-TX of all PAIRs and shall transition to Rx.Detect.LS-MODE.
- Upon detection of a HIBERN8 exit on its M-RX on all PAIRs the DSP shall wait a minimum
- 471 Tactivate time before transitioning to Rx.Detect.LS-MODE.
- A DSP shall transition to SS.Disabled when directed.
- 472
- 473
- 474

475 3.8.2.5 RX.Detect.LS-MODE Requirements

476 Rx.Detect.LS-MODE is a sub-state in which communication takes place in the LS-MODE using the

477 RRAP.

478 The requirements for this sub-state for a USP, DSP are defined in Section 2.5.

479 3.8.2.6 Exit from RX.Detect.LS-MODE

- A DSP shall transition to SS.Disabled when directed.
- An USP and a DSP shall exit to the MPHY.TEST state when an RRAP write command to the
- 481 TEST\_MODE register is received as defined in Table 2-5.
- An USP and a DSP shall execute a RCT to exit this sub-state and enter Polling when configured
- 482 to do so using the RRAP as defined in Section 2.5.3.
- After executing an RCT, the M-TX shall wait for a period equal to the
- 483 RX\_Min\_ActivateTime\_Capability defined in Section 2.2.3 prior to exiting this sub-state into the
- 484 Polling state.
- Note: A delay equivalent to the RX\_Min\_ActivateTime\_Capability timing parameter is prescribed
- 485 in this sub-state to allow flexibility for implementations to prepare for STALL and HS-BURST.
- 486
- 487
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- 489
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491 **3.8.3 Polling**

492 In the Polling state the M-PHY is configured prior to entering HS-BURST. While in HS-BURST, the

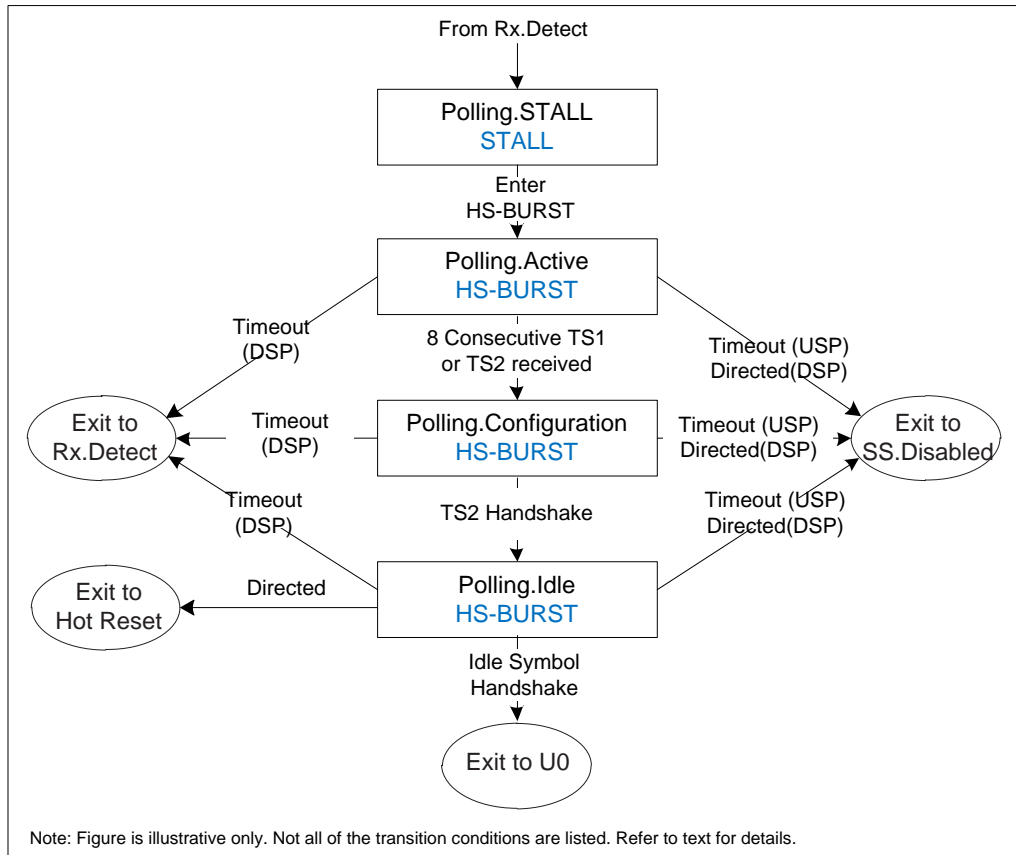
493 training ordered sets of TS1, and TS2 as defined in [USB 3.0] are transmitted.

494 Polling contains a sub-state machine shown in Figure 3-10 with the following sub-states:

- Polling.STALL
  - Polling.Active
- 495
- 496

497  
498  
499

- Polling.Configuration
- Polling.Idle



500

**Figure 3-10 Polling Sub-state Machine**

501

502 3.8.3.1.1 Polling.STALL Requirements

503  
504  
505  
506

- The Polling.STALL sub-state is a transitory sub-state which is used to prepare the M-TX to enter the HS-BURST mode.
- The M-TX and M-RX are in the STALL state.
- An exit from this sub-state should be completed within tPollingSTALLResidency.

507 3.8.3.2 Exit from Polling.STALL

508 The following requirements shall be met in the following order when exiting from this sub-state:

509  
510  
511

- The M-TX shall be transitioned to enter HS-BURST as per [M-PHY] .
- A timer shall be started and set to expire after tRetrain.
- The LTSSM shall transition to Polling.Active.

512 3.8.3.3 Polling.Active/Configuration/Idle Requirements

513  
514  
515  
516  
517  
518

- If the tRetrain timer expires, M-TX shall be cycled from HS-BURST to STALL and then back to HS-BURST, and the tRetrain timer shall then be restarted.
- The M-TX and M-RX shall remain in the HS-BURST state for the remaining Polling sub-states except as required based on tRetrain timer expiration.
- An equivalent of Polling.RxEQ as defined in [USB 3.0] for receiver equalizer training is not required and shall be bypassed.

- 519 • The Disabling Scrambling bit and the Loopback bit in the link configuration field of the TS2
- 520 Ordered Set shall be ignored.
- 521 • Upon successful completion of the Polling sub-states the LTSSM shall transition to U0.
- 522 • The requirements in these sub-states including the handshake sequences and transitions due to
- 523 the expiry of relevant timers are as defined in [USB 3.0], without regard to transitions through
- 524 STALL due to tRetrain timer expiration.
- 525 • Note: M-RX receiver bit synchronization and training is completed using mechanisms specified
- 526 in [M-PHY] . The supplement defines the tRetrain timer as a contingency to enable [M-PHY]
- 527 specific training mechanism to be re-performed. As a result, none of the
- 528 Polling.Active/Configuration/Idle Timeouts defined in [USB 3.0] are expected to expire in SSIC
- 529 implementations with correctly operating M-TX and M-RX modules.

### 530 3.8.4 U0

531 U0 is the normal operational state in which the M-TX and M-RX are in the HS-Burst state and are  
532 actively transmitting and receiving traffic. U0 contains no sub-states.

533 While in U0 the M-TX and the M-RX of a PORT may independently transition between the HS-BURST  
534 and STALL states as shown in Figure 3-11.

535 The M-TX may optionally transition to the STALL state instead of transmitting logical idle symbols. The  
536 conditions under which this transition is made such as number of logical idle symbols that are  
537 transmitted prior to entering the STALL state are not specified in this supplement. For example,  
538 implementations may choose to transition to STALL immediately without transmitting any logical idle  
539 symbols or may continue to transmit logical idle symbols without entering the STALL state.

540 Independently the M-RX shall transition to the STALL state when the link partner's M-TX implementation  
541 chooses to enter the STALL state.

**Implementation Note:**

*In the implementation example described in Figure 1-2, when the PA detects a STALL entry on its M-RX while in U0, the PA may have to manufacture logical idle symbols to be sent to the link layer to maintain the U0 state in the legacy LTSSM.*

542

#### 543 3.8.4.1 Exit from U0

- 544 • A successful LGO\_U1 entry sequence shall transition the link state to U1 and the M-TX/M-RX to
- 545 STALL as follows:
  - 546 ○ The DSP shall initiate LGO\_U1 and shall disable STALL entry on all PAIRs until a LXU
  - 547 is received (indicating abort of U1 entry) or it successfully enters U1.
  - 548 ○ The USP, upon receipt of the LGO\_U1 and if accepting U1 entry, shall in the following
  - 549 order:
    - 550 ▪ disable STALL entry on all PAIRs until it successfully enters U1
    - 551 ▪ respond with a LAU
  - 552 ○ After sending an LPMA, the DSP shall transition to U1 and transition its M-TX to the
  - 553 STALL state on all PAIRs.
  - 554 ○ After receiving an LPMA, the USP shall transition to U1 and transition its M-TX to the
  - 555 STALL state on all PAIRs.
  - 556 ○ U1 can also be initiated by a USP in which case the above sequence takes place with
  - 557 the roles of DSP and USP reversed.
- 558 • A successful LGO\_U2/LGO\_U3 entry sequence shall transition the link state to U2/U3 and the
- 559 M-TX/M-RX to HIBERN8 as follows:
  - 560 ○ The DSP shall in the following order:

- 561                                   ▪ disable S\_TALL entry on all PAIRs and then  
 562                                   ▪ initiate U2/U3 entry via transmission of LGO\_U2/LGO\_U3  
 563           ○ The DSP shall re-enable STALL entry only if either LXU is received (indicating abort of  
 564           U2 entry) or U2/U3 entry is successful  
 565           ○ The USP, upon receipt of the LGO\_U2/LGO\_U3 and if accepting U2/U3 entry, shall in  
 566           the following order:  
 567                                   ▪ disable STALL entry on all PAIRs until it successfully enters U2/U3  
 568                                   ▪ configure M-TX and M-RX modules on all PAIRs for HIBERN8 entry  
 569                                   ▪ respond with a LAU  
 570           ○ The DSP, upon receipt of the LAU shall in the following order:  
 571                                   ▪ configure M-TX and M-RX modules on all PAIRs for HIBERN8 entry  
 572                                   ▪ respond with a LPMA  
 573           ○ After sending an LPMA, the DSP shall transition to U2/U3 and shall terminate the HS-  
 574           BURST on the M-TX of all PAIRs.  
 575           ○ After receiving an LPMA, the USP shall transition to U2/U3 and shall terminate the HS-  
 576           BURST on the M-TX of all PAIRs.

**Implementation Note:**

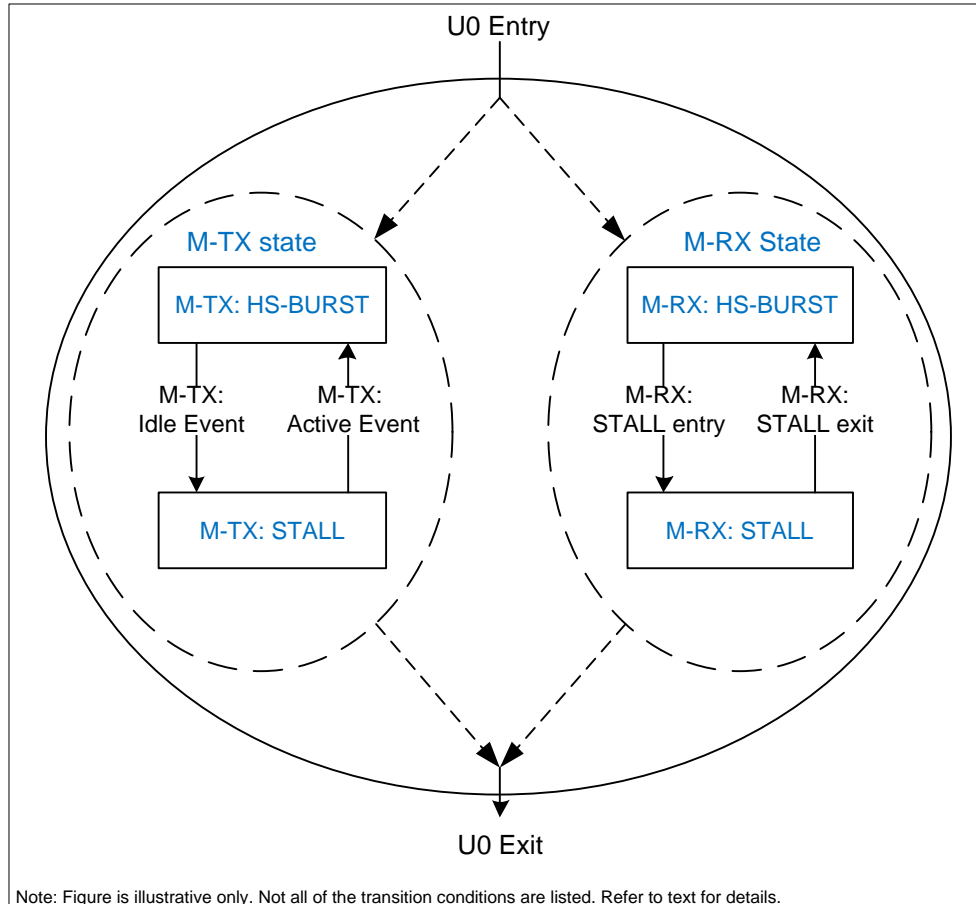
*As per [M-PHY] configuring M-TX and M-RX modules for HIBERN8 entry requires an INLINE-CR registry change and the assertion of the RX\_CfgUpdt/TX\_CfgUpdt signal of the M-RX/M-TX for all PAIRs. As a result of this configuration change, the termination of HS-BURST results in a RCT and causes local M-TX and remote M-RX to enter HIBERN8.*

- 577                                   ○ As per [M-PHY] , the following is guaranteed on HIBERN8 entry:  
 578   ▪ the remote M-RX enters HIBERN8 and shall hold the line in DIF-Z before the  
 579   local M-TX enters HIBERN8  
 580   ▪ During HIBERN8 entry the M-RX ignores any transitions on the line until it  
 581   drives and senses a DIF-Z on the line.  
 582                                   ○ U2 can also be initiated by a USP in which case the above sequence takes place with  
 583                                   the roles of DSP and USP reversed.  
 584                                   ○ U2 can also be initiated by a USP in which case the above sequence takes place with  
 585                                   the roles of DSP and USP reversed.  
 586           • The remaining exit conditions and timeouts for U0 listed in [USB 3.0] also apply.

**Implementation Note:**

*In the event of a LAU corruption event during U2/U3 entry, the link may eventually enter SS.Inactive and may be recovered by the DSP via a Warm Reset.*

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 589



590

591

**Figure 3-11 U0 Sub-state Machine**

592 **3.8.5 U1**

593 U1 is a low-power state with minimum exit latency. Either a DSP or a USP may initiate entry to this state.

- 594
- In this state the M-TX and M-RX state machines shall transition to and stay in the STALL state.

595 This LTSSM state is distinguished from transitions to the STALL state in U0 by the fact that U1 is  
596 entered under direction from the link layer as defined in [USB 3.0].

597 **3.8.5.1 U1 Requirements**

- 598
- SSIC **shall not** support a direct transition from U1 to U2.
  - If the conditions for initiating U2 entry are met, a transition to U0 shall be made prior to initiating an entry to U2 as per criteria in 7.2.4.2.2 of [USB 3.0].
- 599
- 600

601 **3.8.5.2 Exit from U1**

- 602
- The port shall ensure that both M-RX and M-TX are in the STALL state prior to initiating a U1 exit.
  - The port shall exit to Recovery by initiating an HS-BURST on its M-TX or when an HS-BURST is detected by its M-RX.
  - The U1 to SS.Inactive transition due to an unsuccessful U1 exit as defined in [USB 3.0] does not apply to this supplement. When initiated the exit from U1 to Recovery shall be unconditionally completed.
- 603
- 604
- 605
- 606
- 607
- 608

609

610 **3.8.6 U2**

611 U2 is a link state where more power saving opportunities are allowed compared to U1, but with an  
 612 increased exit latency. U2 does not contain any sub-states. Either a DSP or a USP may initiate entry to  
 613 this state.

## 614 3.8.6.1 U2 Requirements

- 615 • The M-TX and the M-RX state machines shall stay in the HIBERN8 state for all PAIRs.
- 616 • The concept of far end receiver termination detection as defined in [USB 3.0] does not apply and  
 617 does not have to be completed while in this state.

## 618 3.8.6.2 Exit from U2

- 619 • The port shall transition to Recovery when a successful U2 exit handshake completes in the  
 620 following manner:
  - 621 ○ The M-RX receives an HIBERN8 exit indication on all PAIRs or M-TX initiates a  
 622 HIBERN8 exit on all PAIRs when port is directed to exit U2 by the link layer and
  - 623 ○ Both M-TX and M-RX successfully exit HIBERN8 on all PAIRs and transition to STALL.
- 624 • The port shall transition to SS.Inactive if the tNoLFPSResponseTimeout timer (as defined in  
 625 [USB 3.0]) expires and if a successful U2 exit handshake as described above is not achieved.

626 The following [M-PHY] capability attributes described in Section 2.2.3 imply a minimum residency of  
 627 200µs in U2:

- 628 • Rx/Tx\_Hibern8Time\_Capability = 100us: Minimum residency time in HIBERN8 state
- 629 • RX\_Min\_ActivateTime\_Capability = 100us: Minimum time to exit HIBERN8

630 The SSIC LTSSM shall ensure that these residency requirements in [M-PHY] are met prior to initiating a  
 631 U2 exit.

632

**Implementation Note:**

[M-PHY] defines the *RX\_Advanced\_Granularity\_Capability* attribute that enables implementations to advertise support for a minimum HIBERN8 residency time and an activate time in granularities smaller than 100us. DSP implementations may discover support for this capability via RRAP and if supported may use it to reduce the default minimum residency of 200 µs in U2.

633

634 **3.8.7 U3**

635 U3 is a link state where a device is put into a suspend state. Though both U2 and U3 map to HIBERN8,  
 636 U3 may provide additional power savings opportunities at a system level due to the requirement to  
 637 complete a handshake upon an exit. Details of such system-level power savings opportunities and the  
 638 means for enabling them are out of scope of this supplement.

639 U3 does not contain any sub-states.

## 640 3.8.7.1 U3 Requirements

- 641 • In this state the M-TX and M-RX state machines are in the HIBERN8 State for all PAIRs.



- 642
- 643
- 644
- 645
- A port not able to respond to U3 exit handshake within  $t_{NoLFPSResponseTimeout}$  (as defined in [USB 3.0]) may respond when it is ready.
  - The concept of far end receiver termination detection as defined in [USB 3.0] does not apply and does not have to be completed while in this state.

646 3.8.7.2 Exit from U3

- 647
- 648
- 649
- 650
- 651
- 652
- 653
- 654
- 655
- 656
- 657
- 658
- 659
- 660
- 661
- 662
- 663
- The port shall transition to Recovery when a successful U3 exit handshake completes in the following manner:
    - One of the following initial conditions is true:
      - The M-TX drives a HIBERN8 exit on all PAIRs when the port is directed to exit U3 by the link layer or
      - the M-RX receives a HIBERN8 exit indication on all PAIRs
    - and the M-TX successfully exit HIBERN8 on all PAIRs and transitions to STALL for a minimum of  $T_{activate}$
    - and a minimum  $T_{activate}$  time has elapsed after M-RX receives a HIBERN8 exit on all PAIRs.
  - The port shall remain in U3 when a successful U3 exit handshake as described above is not achieved.
    - In this case the M-TX which initiated the HIBERN8 exit shall continue to drive DIF-N until the U3 exit handshake successfully completes.
  - Implementations shall ensure that minimum HIBERN8 residency requirements in [M-PHY] are met prior to initiating a U3 exit.

664 3.8.8 Recovery

665 Recovery is a LTSSM state that is entered to retrain the M-PORT. During this state TS1, and TS2

666 training ordered sets are transmitted as defined in [USB 3.0] to synchronize the link and to exchange the

667 link configuration information.

668 Recovery contains the following sub-states:

- 669
- 670
- 671
- Recovery.Active
  - Recovery.Configuration
  - Recovery.Idle

672 3.8.8.1 Recovery.Active Requirements

- 673
- 674
- 675
- 676
- 677
- 678
- 679
- 680
- 681
- 682
- 683
- A timer set to expire after  $t_{RecoveryActiveTimeout}$  (as defined in [USB 3.0]) shall be started upon entry to this sub-state.
  - Initial conditions for this sub-state are dependent on the entry condition:
    - When entered from U0, the M-TX shall be brought to a STALL state in order to re-train the M-TX for a new HS-BURST. The M-RX state is dependent on the link partner M-TX.
    - When entered from U1, the M-RX or M-TX shall initially be in the STALL state as per U1 requirements defined in 3.8.5.2.
    - When entered from U2 or U3, the M-RX and M-TX are initially in the STALL state.
  - The M-TX is then brought to the HS-BURST state and the port shall transmit the TS1 ordered sets upon entry to this sub-state.
  - Upon M-TX entry into HS-BURST, the LTSSM shall start a  $t_{Retrain}$  timer.

684 3.8.8.2 Recovery.Active/Configuration/Idle Requirements

- 685
- 686
- 687
- 688
- If the  $t_{Retrain}$  timer expires, M-TX shall be cycled from HS-BURST to STALL and then back to HS-BURST, and the  $t_{Retrain}$  timer shall then be restarted.
  - The M-TX and M-RX shall remain in the HS-BURST state for the remaining Recovery sub-states, except as required based on  $t_{Retrain}$  timer expiration.

- 689
- 690
- 691
- 692
- 693
- 694
- The requirements for the traffic, handshake sequences and exit conditions for these sub-states are as defined in [USB 3.0], without regard to transitions through STALL due to tRetrain timer expiration.
  - The Disabling Scrambling bit and the Loopback bit in the link configuration field of the TS2 Ordered Set shall be ignored.
  - Upon successful completion of the Recovery sub-states the LTSSM shall transition to U0.

695 **3.8.9 Hot Reset**

696 The Hot Reset state shall be implemented as specified in [USB 3.0].

697 **3.8.9.1 Hot Reset Requirements**

- 698
- 699
- 700
- In this state the M-TX and M-RX are in the HS-BURST state.
  - The port shall implement the Hot Reset sub-states, associated timers and exit conditions as defined in [USB 3.0].

701 **3.8.10 SS.Inactive**

702 SS.Inactive is an error state where the link becomes non-operational.

703 A DSP in this state, shall transition its M-TX and M-RX to the DISABLED state. In this state, the DSP is  
704 not able to receive any communication from the USP. A DSP shall only exit from this state when directed  
705 to issue a Warm Reset. In order to signal a warm reset, the DSP shall transition out of the DISABLED  
706 state and drive a LINE-RESET as defined in [M-PHY] on PAIR0.

707 An USP in this state, shall assert and then de-assert the local M-PHY Reset for all LANEs bringing the  
708 M-TX and M-RX to the HIBERN8 state on all PAIRs. A USP shall only exit upon the receipt of a Warm  
709 Reset. While in SS.Inactive an USP shall ignore any data received on the M-RX until a LINE-RESET is  
710 received.

711 The concept of far end receiver termination detection as defined in [USB 3.0] does not apply and does  
712 not have to be completed while in this state.

713 **3.8.11 MPHY.TEST**

714 MPHY.TEST is an LTSSM state used for testing the M-PHY Physical layer.

715 The initial state of the M-TX and M-RX state machines in this state is PWM-BURST.

716 For details of the operational behavior in this state please refer to Section 6.

717

## 718 4 Protocol Layer

719 Implementations incorporate the protocol layer defined in [USB 3.0] except as defined in this section.

### 720 4.1 Port Capability Link Management Packet (LMP)

721 The Port Capability LMP describes each port's link capabilities and is sent by both link partners after the  
722 successful completion of training and link initialization.

723 Implementations shall ignore the Link Speed field of the Port capability LMP. The operational speed of  
724 the link shall be defined by the profile as defined in Section 2.2.1.

725 Implementations shall ignore the USB 3.0 OTG Capable (OTG) field of the Port Capability LMP. The  
726 Direction (D) field shall be used to identify the DSP and the USP as defined in [USB 3.0].

### 727 4.2 Timing Parameters

728 The protocol-layer timing parameters described in Section 8.13 of [USB 3.0] also apply to this  
729 supplement.

730 However certain timing parameters are modified as shown in Table 4-1 to account for a slower bit-rate  
731 (for HS-G1/G2) and latencies introduced due to STALL entry and exit while in U0.

732 This supplement also relaxes the accuracy of timestamps reported by Isochronous Timestamp Packets  
733 in the following manner: The Delta value of the ITS field shall be required to have an accuracy of  $\pm 5$   
734 `tlsochTimestampGranularity` units.

735 **Table 4-1 Protocol Timing Parameters**

Name	Description	Min	Max	Units
tPingResponse	Time between device reception of the last framing symbol of a ping and the first framing symbol of the ping_response		5000	ns
tNRDYorSTALLResponse	Time between device reception of the last framing symbol for an ACK TP or a DPP or a STATUS TP and the first framing symbol of an NRDY or STALL response		5000	ns
tDPResponse	Time between device reception of the last framing symbol for an ACK TP and the first framing symbol of a DP response		5000	ns
tACKResponse	Time between device reception of the last framing symbol for a DPP or a STATUS TP and the first framing symbol of an ACK response		5000	ns
tMaxBurstInterval	Time between DPs when the device or host is bursting. If the device cannot meet this maximum time, then it shall set the EOB flag in the last DP it sends.		1000	ns

Inter-Chip Supplement to the USB Revision 3.0 Specification

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tHostACKResponse	Time between host reception of the last framing symbol for a DPP and the first framing symbol of an ACK response		5000	ns
------------------	--	--	------	----

- 736 **5 Device Framework**
- 737 Implementations incorporate the device framework defined in [USB 3.0] except as defined in this section.
- 738 **5.1 Dynamic Attachment and Removal**
- 739 Though this interconnect is intended for embedded inter-chip links, there is a usage requirement to  
 740 support dynamic removal and subsequent attachment to support power management goals or to present  
 741 an alternative device configuration. This supplement supports mechanisms to have either the USP or the  
 742 DSP initiate a disconnect as described in the following sections.
- 743 **5.1.1 USP Disconnect**
- 744 The use case for signaling an USP Disconnect is to enable a peripheral to re-enumerate with a different  
 745 device configuration. A USP achieves this by indicating a disconnect and a subsequent re-connect as  
 746 defined in this section.
- 747 The operational model for a USP to signal a Disconnect is as follows:
- 748 • The USP shall signal a Disconnect by signaling a LINE-RESET on its M-TX on PAIR0.
  - 749 • The USP shall maintain a DIF-N prior to driving a DIF-P on its M-TX as per the LINE-RESET  
 750 timing specified in [M-PHY] .
  - 751 • Signaling a LINE-RESET on any M-TX other than that of PAIR0 has undefined results.
  - 752 • Upon completion of the LINE-RESET, the USP shall assert local M-PHY Reset for all LANEs  
 753 within Tline\_to\_local\_rst
  - 754 • The USP shall keep local M-PHY Reset asserted for Tlocal\_rst
  - 755 • The USP M-TX and M-RX of all the LANES shall subsequently transition to the DISABLED state
  - 756 • The USP LTSSM shall transition to the SS.Disabled state.
  - 757 • The Peripheral Upstream Device port shall transition to USDPORT.Powered-Off (as defined in  
 758 Fig 10-25 of [USB 3.0]).
  - 759 • If a USP is in U3, a U3 exit handshake shall be completed prior to signaling a disconnect.  
 760 Signaling of a USP disconnect while in U3 is not supported and has undefined results.
- 761 The operational model for a DSP upon detecting a USP Disconnect is as follows:
- 762 • The DSP shall wait until the completion of LINE-RESET signaling
  - 763 • Upon completion of the LINE-RESET, the DSP shall assert local M-PHY Reset for all LANEs  
 764 within Tline\_to\_local\_rst
  - 765 • The DSP shall keep local M-PHY Reset asserted for Tlocal\_rst
  - 766 • The DSP shall then transition to Rx.Detect.Active as described in Section 3.8.2 in order to detect  
 767 a subsequent re-connect from the USP.
- 768 The operational model for a USP to signal a subsequent re-connect is as follows:
- 769 • When ready to re-connect, the USP shall de-assert local M-PHY Reset on all LANEs.
  - 770 • The USP M-TX and M-RX shall transition to the HIBERN8 state for all LANEs.
  - 771 • The USP LTSSM shall transition to the Rx.Detect.Active state.
  - 772 • The Peripheral Upstream Device port shall transition to USDPORT.Powered On (as defined in  
 773 Fig 10-25 of [USB 3.0]).
- 774 **5.1.2 DSP Disconnect**
- 775 The DSP disconnect is a host-initiated mechanism to enable a peripheral to re-enumerate with a  
 776 different device configuration.

777 An additional use case for signaling a DSP disconnect is to disable the associated port. In this case, a  
 778 USP can re-connect only after the DSP is subsequently re-enabled. A mechanism for the USP to request  
 779 DSP to be re-enabled is out of scope of this supplement.

780 The operational model for a DSP to signal a Disconnect is as follows:

- 781 • The DSP shall signal a Warm Reset on the M-TX of PAIR0 as defined in Section 3.6.2.2.
- 782 • Upon completion of the Warm Reset, the LTSSM shall transition to Rx.Detect.Active and then to  
 783 Rx.Detect.LS-MODE
- 784 • In the Rx.Detect.LS-MODE sub-state, while in PWM-BURST mode, the DSP shall signal a  
 785 disconnect by signaling a RRAP write command and shall ensure a valid RRAP write response  
 786 is received as defined in Section 2.5.2.
- 787 • Upon the receipt of a Write Response with a valid parity from the Target, the Master shall end  
 788 the PWM-BURST on its M-TX.
- 789 • On detecting the closure of the PWM-BURST on its M-RX, the RRAP Target shall end the PWM-  
 790 BURST on its M-TX.
- 791 • A BURST\_CLOSURE RRAP command shall not be transmitted by the DSP prior to terminating  
 792 the PWM-BURST.
- 793 • A DSP shall then assert the local M-PHY reset for all LANES:
  - 794 • The DSP M-TX and M-RX of all the LANES are in the DISABLED state
  - 795 • The DSP LTSSM is in the SS.Disabled state.

796 The operational model for a USP upon detecting a DSP Disconnect is as follows:

- 797 • The USP shall wait for the PWM-BURST to be terminated on its M-RX and then terminate the  
 798 PWM-BURST on its M-TX.
- 799 • The USP shall assert and then de-assert the local M-PHY Reset for all LANES bringing the M-TX  
 800 and M-RX to the HIBERN8 state on all PAIRs
- 801 • The USP LTSSM shall transition to the RxDetect.Active state.
- 802 • The Peripheral Upstream Device port shall transition to USDPORT.Powered-On (as defined in  
 803 Fig 10-25 of [USB 3.0]).
- 804 • This behavior enables a USP to detect a re-connect when the DSP is subsequently re-enabled.
- 805 • The USP may optionally be powered down, the Peripheral Upstream Device port transitioned to  
 806 the USDPORT.Powered-Off state and the M-PHY transitioned to the SS.Disabled state. In this  
 807 case the USP will not be able to detect a re-connect from the DSP. In such a scenario, a  
 808 mechanism for powering up the USP to detect a subsequent re-connect is out of scope of this  
 809 supplement.

810 **5.1.3 Disconnect Timing Parameters**

811 This section defines timing parameters used in the process of USP and DSP disconnect.

812 **Table 5-1 Disconnect Timing Parameters**

Name	Description	Min	Max	Units
Tline_to_local_rst	Time between the detection of local/remote LINE-RESET completion and the subsequent assertion of local reset		5	ms
Tlocal_rst	Duration of USP/DSP local M-PHY Reset assertion	10	1000	ms

813

814

## 6 MPHY.TEST

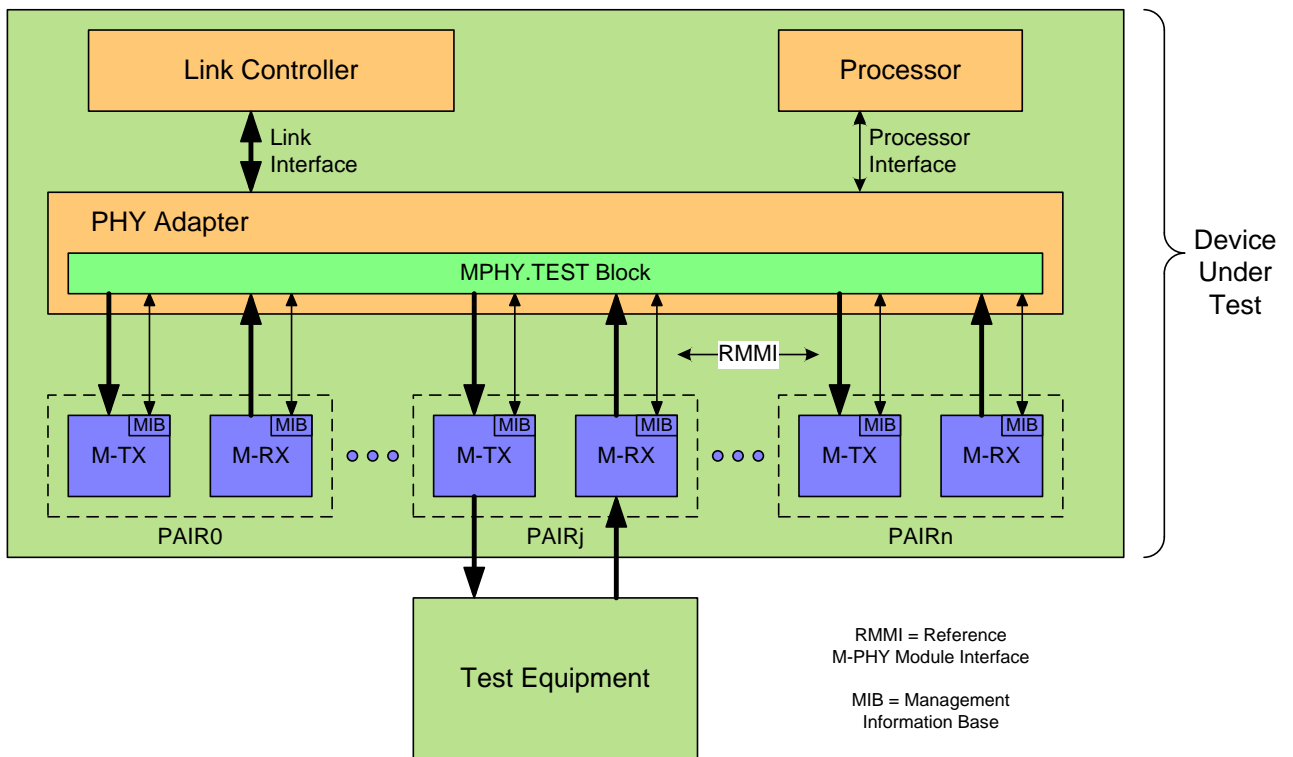
815 The test mechanisms defined in this section are **optional normative** and defines the behavior of a USP  
 816 or a DSP in the optional MPHY.TEST state. If the MPHY.TEST state is supported, the following  
 817 requirements defined in this section shall apply.

### 6.1 Overview

819 The purpose of the MPHY.TEST state is to allow standardized electrical testing of SSIC M-PHYs. For  
 820 example, [CTS] defines a set of M-PHY electrical tests which are independent of the protocol layer. The  
 821 M-PHY based protocols that use these tests are listed in Appendix D of [CTS].

822 Figure 6-1 shows an SSIC Device Under Test attached to Test Equipment and illustrates the various  
 823 components involved in the support of the MPHY.TEST state. In the figure below, “n” indicates the  
 824 number of supported PAIRs.

825



826

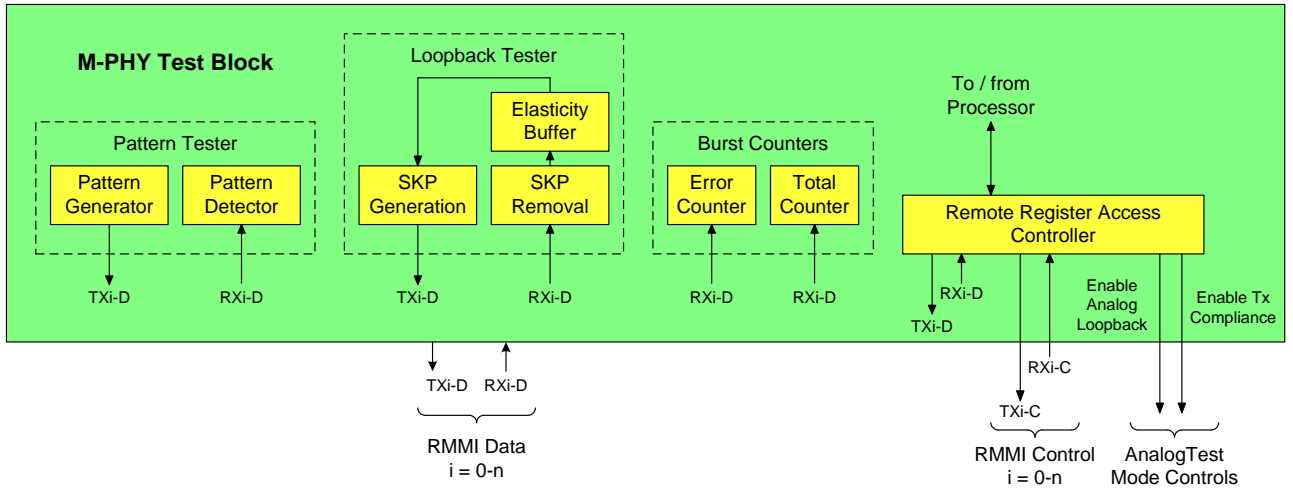
827

Figure 6-1 MPHY.TEST Overview

828

829 This section currently defines support for x1 LANE implementations of SSIC and the PAIR that the Test  
 830 Equipment is attached to is referred to in this section as the PAIR Under Test. After issuing a LINE-  
 831 RESET to the DUT, the Test Equipment transitions the DUT into the MPHY.TEST state using RRAP  
 832 commands. In the MPHY.TEST state, the Test Equipment configures the M-PHY's electrical parameters  
 833 and the the MPHY.TEST Block for either loopback or receive BURST testing.

834



835

836

**Figure 6-2 Example of an MPHY.TEST Block**

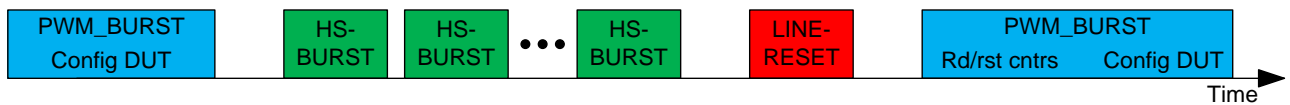
837 Figure 6-2 provides an example of an implementation of various functional blocks in the MPHY.TEST  
838 Block.

839 The functional blocks shown in the Loopback Tester box, enable sensitivity and transmit signal integrity  
840 tests by receiving HS-BURSTS from the Test Equipment and looping them back. (Note: Loopback  
841 Testing and Analog Loopback are two distinct and separate modes as described in Sections 6.3 and 6.6)

842 The functional blocks shown in the Receive Counters block enable testing of HS-BURST entry and exit  
843 parameters such as PREPARE time, SYNC length, Tail-Of-Burst length and STALL time.

844 The Remote Register Access controller enables functionality related to the RRAP for the MPHY.TEST  
845 registers including the control of test modes in the M-PHY such as the Analog loopback and Tx  
846 Compliance modes.

847 Figure 6-3 illustrates an example of a receive BURST testing sequence including an initial PWM-BURST  
848 for DUT configuration, a series of appropriate HS-BURSTS for the actual receive BURST testing, a LINE-  
849 RESET and a final PWM-BURST that is used by the Test Equipment to read the results in the Receive  
850 Counters in the DUT.



851

852

**Figure 6-3 Receive BURST Test Sequence**

853 The following sections detail the following various DUT requirements for:

- 854 • entering the MPHY.TEST state
- 855 • Loopback testing
- 856 • Receive Burst testing
- 857 • MPHY.TEST registers

## 858 6.2 Entering MPHY.TEST

859 The operational model for entering the MPHY.TEST state and the associated DUT requirements are  
860 described below:



- 861 • The DUT shall transition through the Rx.Detect.Reset, Rx.Detect.Active and the Rx.Detect.LS-  
862 MODE states as described in Section 3.8.2.
- 863 • In the Rx.Detect.LS-MODE state, the DUT shall support the receipt of a PWM-BURST from the Test  
864 Equipment on any of the supported PAIRs.
- 865 • In the PWM-BURST mode, the DUT shall support the receipt of a RRAP Write Command to enable  
866 the transition to the MPHY.TEST state and shall issue a valid Write Response as defined in Table  
867 2-5.
- 868 • The DUT shall transition to the MPHY.TEST state.

### 869 **6.3 Loopback Testing**

870 The operational model for enabling Loopback Testing and the associated DUT requirements are  
871 described below:

- 872 • Test equipment transitions the DUT to the MPHY.TEST mode prior to configuring it for Loopback  
873 Testing.
- 874 • Test Equipment issues a RRAP Write Command to set the LOOPBACK\_EN[0] register bit as  
875 defined in Table 6-1.
- 876 • Upon receipt of the Write command, the DUT shall enable Loopback Testing for the PAIR under  
877 Test and shall issue a valid Write Response.
- 878 • Test Equipment appropriately configures the PAIR under Test for HS-MODE.
- 879 • Test Equipment closes the PWM-BURST and ensures conditions are met for a RCT to transition the  
880 DUT to the HS-MODE. A BURST\_CLOSURE RRAP command is not required prior to terminating  
881 the PWM-BURST.
- 882 • Upon detecting the start of HS-BURST on M-RX, the DUT shall initiate a HS-BURST on the M-TX
- 883 • Upon detecting the end of HS-BURST on M-RX, the DUT shall terminate the HS-BURST on the M-  
884 TX.
- 885 • Upon initiating a HS-BURST on the M-TX of the PAIR under Test, the DUT shall loop back received  
886 HS-BURST payloads until a LINE-RESET is received.
- 887 • The DUT shall transmit the payload exactly as received with the exception of inserted or removed  
888 SKP ordered sets, regardless of whether scrambling is enabled or disabled by the Tester Equipment  
889 using the corresponding RRAP command.
- 890 • Upon initiating a HS-BURST on the M-TX of the PAIR under Test, the DUT may insert one or more  
891 MK0 or FLR symbols until the loop back begins.
- 892 • Both M-RX and M-TX shall use the Configuration Attribute values as programmed using RRAP.

893

894 The following additional requirements for the PAIR under Test shall apply during Loopback Testing:

- 895 • The M-TX shall maintain running disparity of transmitted symbols.
- 896 • The PAIR is allowed to discard received SKP ordered sets in order to avoid receiver overflow
- 897 • The PAIR is allowed to inject SKP ordered sets in the transmitted data to avoid transmit underflow
- 898 • The M-TX shall close the HS-BURST when a HS-BURST closure is detected on the M-RX.

899

900 Upon detecting the start of an HS-BURST at the M-RX, the M-TX shall start output a HS-BURST. If the  
901 PREPARE and SYNC period received on the M-RX is longer than the corresponding values in the M-TX,  
902 the M-TX may inject SKP ordered sets after the initial MK0 of the transmit payload. If the PREPARE and  
903 SYNC period received on the M-RX is shorter than the corresponding values in the M-TX, the M-TX may  
904 drop symbols after the initial MK0 of the received payload. Test Equipment can ensure that the  
905 PREPARE and SYNC period received on the M-RX is equal or greater than the corresponding values in  
906 the M-TX, to prevent the dropping of symbols by the PAIR under Test.

907 The size of the Elasticity Buffer shown in Figure 6-2 shall be sufficient to handle the maximum clock  
908 skew allowed by [M-PHY] between two M-PORTs, given that the Test Equipment is required to inject at  
909 least one SKP every 354 symbols.

910

## 911 **6.4 Receive Burst Testing**

912 The following requirements shall apply during Receive Burst Testing:

- 913 • The DUT shall implement the RX\_BURST\_COUNT, RX\_ERR\_COUNT and the  
914 RX\_COUNT\_RESET registers as defined in Table 6-1.
- 915 • The RX\_BURST\_COUNT registers shall increment each time the M-RX of the PAIR under Test  
916 transitions from HS-BURST to STALL.
- 917 • The four RX\_BURST\_COUNT registers implement a 4 Byte counter for the PAIR under Test  
918 with RX\_BURST\_COUNT\_0 indicating the LSB and RX\_BURST\_COUNT\_3 the MSB of the  
919 count.
- 920 • The RX\_ERR\_COUNT registers shall increment each time the M-RX of the PAIR under Test  
921 transitions from HS-BURST to STALL without detecting an MK0 during the burst.
- 922 • The four RX\_ERR\_COUNT registers implement a 4 Byte counter for the PAIR under Test with  
923 RX\_ERR\_COUNT\_0 indicating the LSB and RX\_ERR\_COUNT\_3 the MSB of the count.
- 924 • The RX\_BURST\_COUNT and RX\_ERR\_COUNT registers shall be reset when the DUT  
925 receives a RRAP Write Command that sets the RX\_COUNT\_RESET[0] register. These registers  
926 shall not be reset upon the receipt of a LINE-RESET.
- 927 • The RX\_BURST\_COUNT and RX\_ERR\_COUNT registers shall remain unchanged and not  
928 rollover when they have reached their maximum values.
- 929 • The RX\_BURST\_COUNT and RX\_ERR\_COUNT registers shall always be updated as  
930 described above when in the MPHY.TEST state.

## 931 **6.5 Tx Compliance Mode**

932 The operational model for enabling Tx Compliance mode and the associated DUT requirements are  
933 described below:

- 934 • Test equipment transitions the DUT to the MPHY.TEST mode prior to configuring it in Tx  
935 Compliance Mode.
- 936 • Test Equipment issues a RRAP Write Command to set the TX\_COMP\_MODE\_EN[0] register bit  
937 as defined in Table 6-1.
- 938 • Upon receipt of the Write command, the DUT shall enable Tx Compliance mode for the PAIR  
939 under Test and shall issue a valid Write Response.
- 940 • Test Equipment appropriately configures the PAIR under Test for HS-MODE.
- 941 • Test Equipment closes the PWM-BURST on the M-RX of the PAIR under Test. A  
942 BURST\_CLOSURE RRAP command is not required prior to terminating the PWM-BURST.
- 943 • Upon detecting the end of PWM-BURST on its M-RX, the DUT shall terminate the PWM-BURST  
944 on the M-TX.
- 945 • The M-TX of the PAIR under Test shall then continuously transmit the CRPAT compliance  
946 pattern in HS-MODE as defined in [M-PHY] Annex B.1.2.
- 947 • The DUT shall remain in the Tx Compliance Mode until a LINE-RESET is received from the Test  
948 Equipment.

## 949 **6.6 Analog Loopback Mode**

950 The operational model for enabling Analog Loopback mode and the associated DUT requirements are  
951 described below:

- 952 • Test equipment transitions the DUT to the MPHY.TEST mode prior to configuring it in Analog  
953 Loopback Mode.
- 954 • Test Equipment issues a RRAP Write Command to set the ANALOG\_LOOPBACK\_EN[0]  
955 register bit as defined in Table 6-1.
- 956 • Upon receipt of the Write command, the DUT shall enable Analog Loopback mode for the PAIR  
957 under Test and shall issue a valid Write Response.
- 958 • Test Equipment appropriately configures the PAIR under Test for HS-MODE.
- 959 • Test Equipment closes the PWM-BURST on the M-RX of the PAIR under Test. A  
960 BURST\_CLOSURE RRAP command is not required prior to terminating the PWM-BURST.
- 961 • Upon detecting the end of PWM-BURST on its M-RX, the DUT shall terminate the PWM-BURST  
962 on the M-TX.
- 963 • Subsequently all the data received on the M-RX of the Pair under Test in HS-BURST shall be  
964 transmitted back on the M-TX of the PAIR under Test.
- 965 • This functionality is analogous to the mode defined in [M-PHY] Annex B.2.2 as “Analog  
966 Loopback” mode. Specifically a “Synchronous Loopback” mechanism is employed as described  
967 in Annex B.2.2.1 in which the recovered clock from M-RX is used to retransmit the data on the  
968 M-TX.
- 969 • The DUT shall remain in Analog Loopback Mode until a LINE-RESET is received from the Test  
970 Equipment.

971 The following additional requirements for the PAIR under Test shall apply during Analog Loopback  
972 mode:

973 Upon detecting the start of an HS-BURST at the M-RX, the M-TX shall start output a HS-BURST. If  
974 the PREPARE and SYNC period received on the M-RX is longer than the corresponding values in  
975 the M-TX, the M-TX shall transmit all bits on M-TX with bits received in M-RX. If the PREPARE and  
976 SYNC period received on the M-RX is shorter than the corresponding values in the M-TX, the M-TX  
977 may drop bits. Test Equipment can ensure that the PREPARE and SYNC period received on the M-  
978 RX is equal or greater than the corresponding values in the M-TX, to prevent the dropping of bits by  
979 the PAIR under Test.

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## 981 6.7 MPHY.TEST Block Registers

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**Table 6-1 MPHY.TEST Block Registers**

UpperAddr	LowerAddr	Register Name	Description
0xE	0x00	LOOPBACK_EN	<p>This Register is used to enable Loopback Testing for the PAIR under Test.</p> <p>Read/Write Attributes:</p> <ul style="list-style-type: none"> <li>• R/W</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>• 0x00</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>• Writing 1'b1 enables the loopback mode for the PAIR under Test.</li> <li>• Writing 1'b0 shall have no effect.</li> </ul>

UpperAddr	LowerAddr	Register Name	Description
			<p>Once the bit is set, it shall only be reset via a LINE-RESET issued by Test Equipment.</p> <p>Bit[7:1] Reserved.</p> <ul style="list-style-type: none"> <li>Writes shall be ignored and Reads shall return zero values.</li> </ul>
0xE	0x01-0x04	RX_BURST_COUNT_0 RX_BURST_COUNT_1 RX_BURST_COUNT_2 RX_BURST_COUNT_3	<p>These Registers count the number of bursts by incrementing on each HS-BURST to STALL transition. RX_BURST_COUNT_0 is the LSB.</p> <p>R/W attributes:</p> <ul style="list-style-type: none"> <li>Read Only</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>0x00</li> </ul> <p>This register shall be reset only when RX_COUNT_RESET[0] is set. This register is not affected by a LINE-RESET issued by Test Equipment.</p>
0xE	0x05-0x08	RX_ERR_COUNT_0 RX_ERR_COUNT_1 RX_ERR_COUNT_2 RX_ERR_COUNT_3	<p>These Registers count the number of errors by incrementing on each HS-BURST to STALL transition for which an MK0 was not detected. RX_ERR_COUNT_0 is the LSB.</p> <p>R/W attributes:</p> <ul style="list-style-type: none"> <li>Read Only</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>0x00</li> </ul> <p>This register shall be reset only when RX_COUNT_RESET[0] is set. This register is not affected by a LINE-RESET issued by Test Equipment.</p>
0xE	0x09	RX_COUNT_RESET	<p>This register is used to reset the RX_BURST_COUNT and the RX_ERR_COUNT registers</p> <p>R/W attributes:</p> <ul style="list-style-type: none"> <li>Write Only, Self Clearing</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>0x00</li> </ul> <p>Bit [0]:</p>

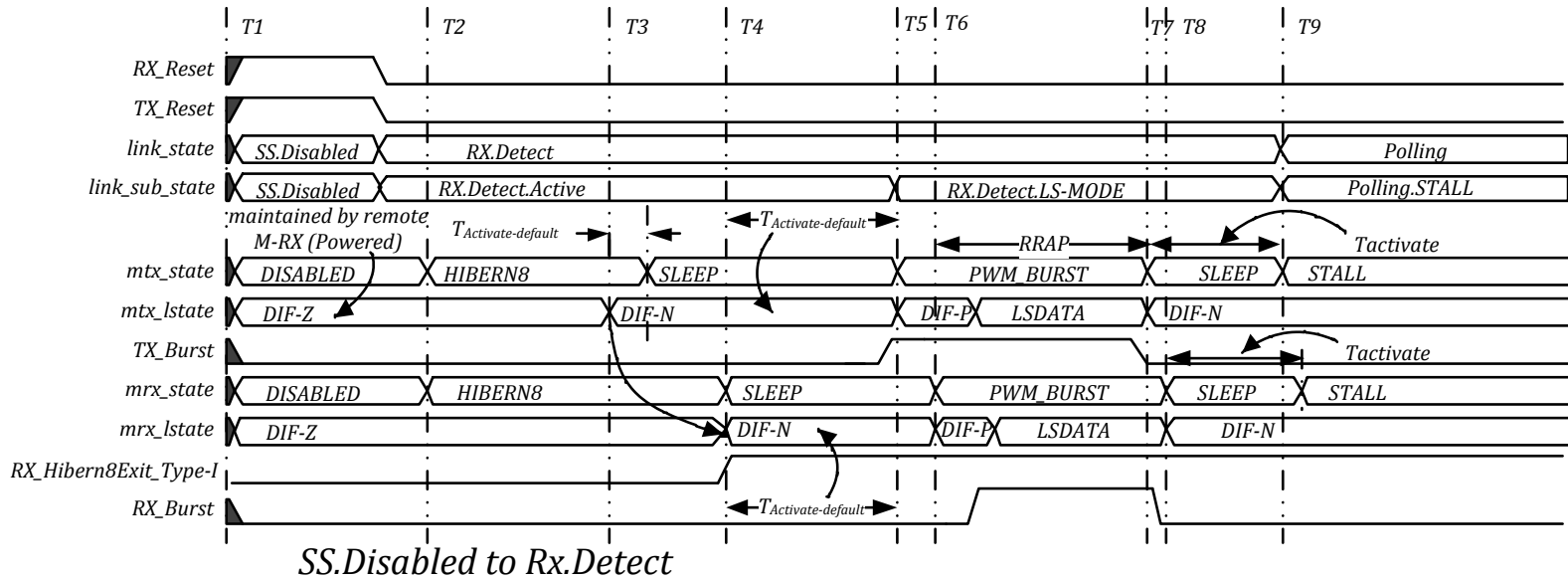
UpperAddr	LowerAddr	Register Name	Description
			<ul style="list-style-type: none"> <li>Writing 1'b1 resets the RX_BURST_COUNT and the RX_ERR_COUNT registers</li> </ul> Bits [7:1]: Reserved.
0xE	0x0A	TX_COMP_MODE_EN	<p>This register is used to enable M-TX of the PAIR under Test in TX Compliance mode.</p> <p>Writes to this register are undefined unless the DUT is in the MPHY.TEST state.</p> <p>R/W Attributes:</p> <ul style="list-style-type: none"> <li>Write Only</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>0x00</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>Writing 1'b1 enables Tx Compliance Mode for the PAIR under Test. In this mode the DUT transmits the Continuous mode CRPAT defined in [CTS].</li> <li>Writing 1'b0 shall be ignored and Reads shall return zero values.</li> </ul> <p>Once the bit is set, it shall only be reset via a LINE-RESET issued by Test Equipment.</p> <p>Bits[7:1] Reserved:</p> <ul style="list-style-type: none"> <li>Writes shall be ignored and Reads shall return zero values.</li> </ul>
0xE	0x0B	ANALOG_LOOPBACK_EN	<p>This register is used to place the M-RX of the PAIR under Test in Analog Loopback mode.</p> <p>Writes to this register are undefined unless the DUT is in the MPHY.TEST state.</p> <p>R/W Attributes:</p> <ul style="list-style-type: none"> <li>Write Only</li> </ul> <p>Reset Default:</p> <ul style="list-style-type: none"> <li>0x00</li> </ul> <p>Bit [0]:</p> <ul style="list-style-type: none"> <li>Writing 1'b1 enables Analog Loopback Mode for the PAIR under Test</li> <li>Writing 1'b0 shall be ignored and Reads shall return zero values.</li> </ul> <p>Once the bit is set, it shall only be reset via a LINE-RESET issued by Test Equipment.</p> <p>Bits[7:1] Reserved:</p>

UpperAddr	LowerAddr	Register Name	Description
			<ul style="list-style-type: none"> <li>Writes shall be ignored and Reads shall return zero values.</li> </ul>
0xE	0x0C- 0xFF	RESERVED	Reserved. Writes shall be ignored and Reads shall return zero values.

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985 **7 Timing Diagrams Appendix (Informative)**

986 **7.1 SS.DISABLED TO RX.DETECT**



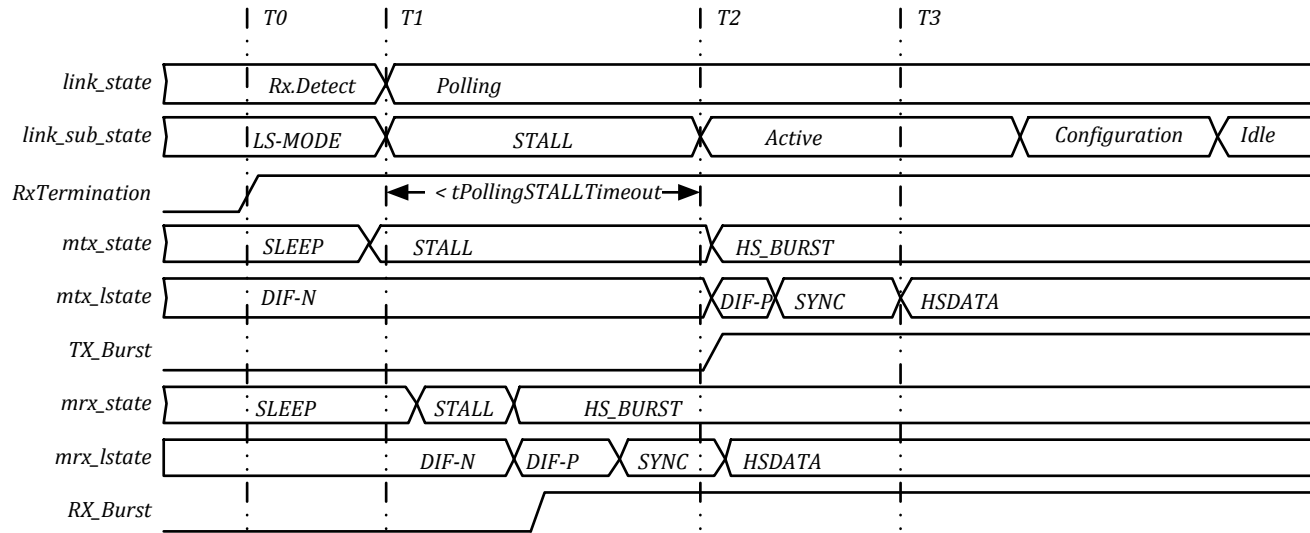
T1: Power On Reset, TX\_Reset and RX\_Reset asserted  
 T2: After finishing Power On Reset, DSP enters into HIBERN8  
 T3: DSP starts HIBERN8 exit on it's M-TX  
 T4: After receiving HIBERN8 exit on M-RX, USP starts HIBERN8 exit on it's M-TX  
 T5: After receiving HIBERN8 exit on M-RX, DSP enters into PWRM\_BURST and starts issuing RRAP commands  
 T6: M-Rx enters PWM-BURST. During PWM-BURST the RRAP Commands and Responses are sent  
 T7: DSP and USP finished all RRAP commands. DSP initiates exit from PWM\_BURST and enters into SLEEP  
 T8: Upon receiving PWM\_BURST exit on M-RX, USP initiates PWM\_BURST exit on it's M-TX and enters into SLEEP  
 T9: After entering SLEEP, both DSP and USP executes RCT and moves to STALL

Note:

- Time between T3 and T4 shown in figure is illustrative only. Spec does not define this time interval
- Tactivate-default is the reset value of TX\_Min\_ActivateTime = 1.5ms as per MPHY spec
- Tactivate is 100us as per SSIC profile definition
- This diagram is for DSP only.

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## 7.2 RX.DETECT TO POLLING



### Rx.Detect to Polling

*T0: RRAP has completed successfully and PA is ready for connect, Indicates termination present to link layer.*

*T1: Link detects termination and moves to Polling state*

*T2: Link enters into Polling.Active state and starts sending TS1 sets, PA puts M-TX into HS\_BURST state*

*T3: Both link partners are in Polling with it's M-TX and M-RX in HS\_BURST and exchanging Training sets*

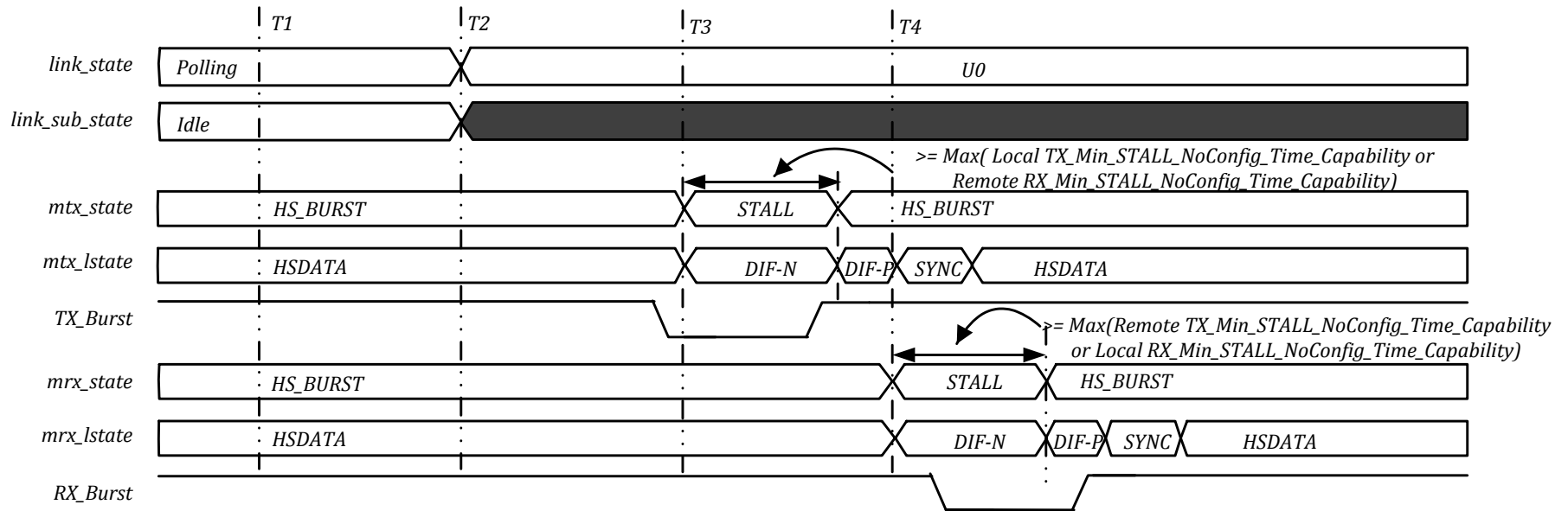
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*Note: RxTermination is conceptual signal indicating remote receiver is present*



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### 7.3 POLLING TO U0

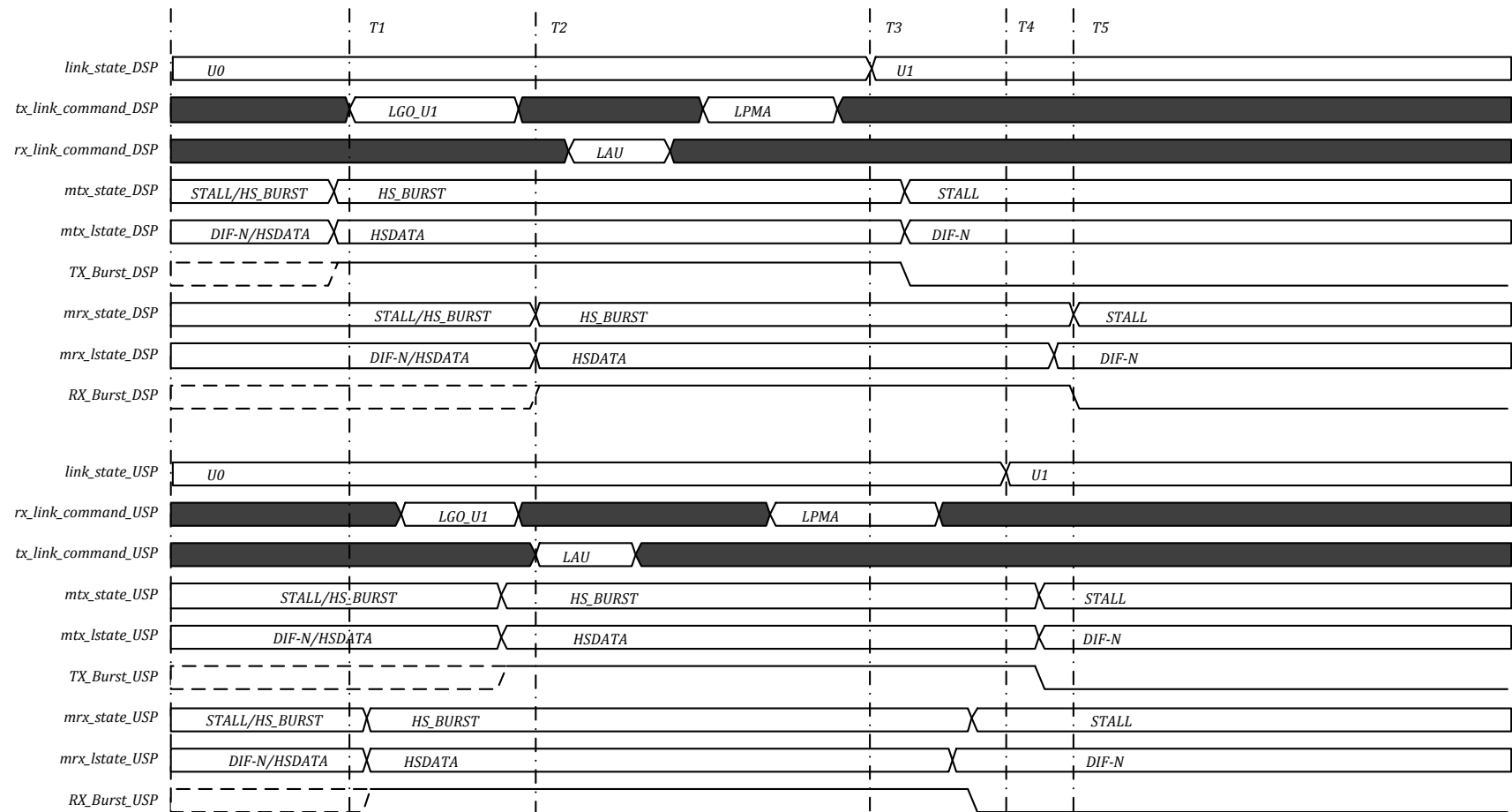


### Polling to U0

- T1: Both Link partner are in Polling state. Both M-TX and M-RX in HS\_BURST state.
- T2: After successful handshake of TS1/TS2/Logical IDLE, Both link partner enters into U0 state.
- T3: M-TX transitions to the STALL state when link is not sending any packets other than logical IDLE symbol
- T4: Independently the M-RX transitions to the STALL state when the link partner's M-TX enter the STALL state

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### 7.4 U0 TO U1



### U0 to U1

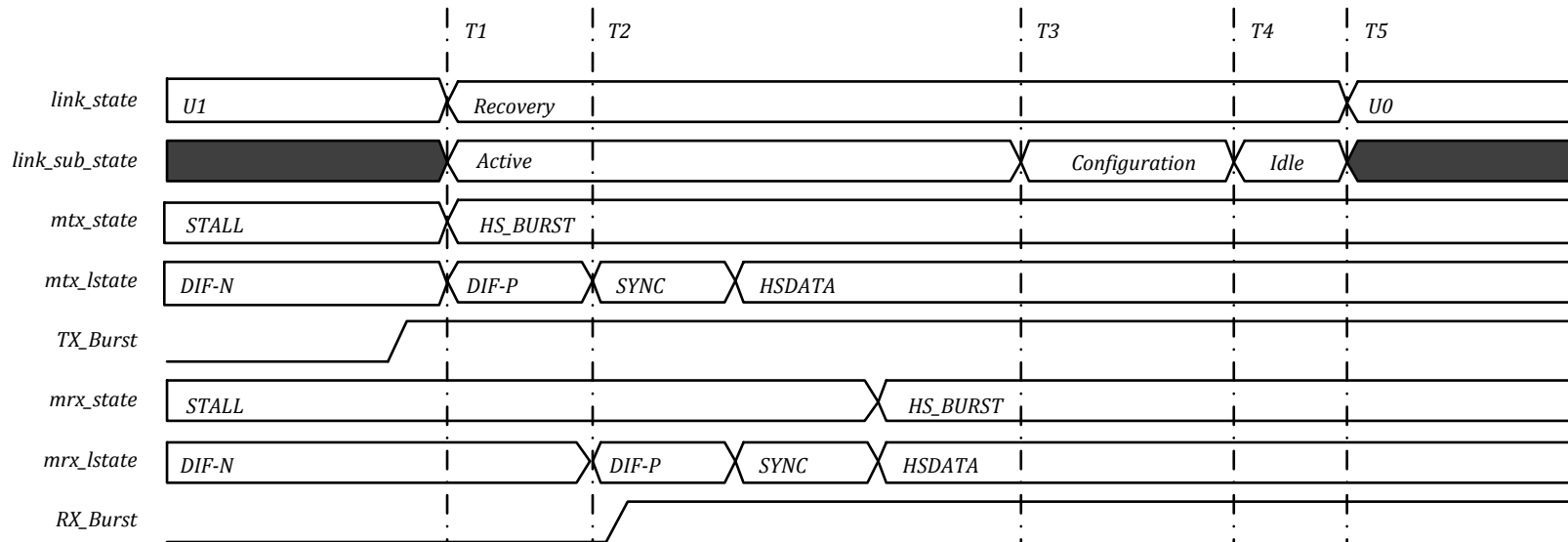
- T1: DSP link sends initiates U1 entry by sending LGO\_U1 and disables its M-TX entering in to STALL
- T2: USP link accepts U1 entry by sending LAU and disables its M-TX entering in to STALL
- T3: After receiving LAU, DSP sends LPMA, enters in U1 and puts its M-TX in to STALL
- T4: After receiving LPMA USP enters in U1 and puts its M-TX in to STALL
- T5: U1 entry completed. Both DSP and USP has its M-TX/M-RX in STALL

Note: link shall not initiates U1 exit until both M-TX (local) and M-RX (local) is in STALL. This is to ensure that both link partner are in U1.  
 Note: In this diagram, U1 entry is initiated by DSP but USP can also initiate U1 entry in a same way.

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## 7.5 U1 TO U0

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### U1 to U0

*T1: Link partner 1 initiates U1 exit by making sure that it's M-RX and M-TX is in STALL*

*T2: Link partner 2 detects U1 exit on it's M-RX and starts HS\_BURST on it's M-TX.*

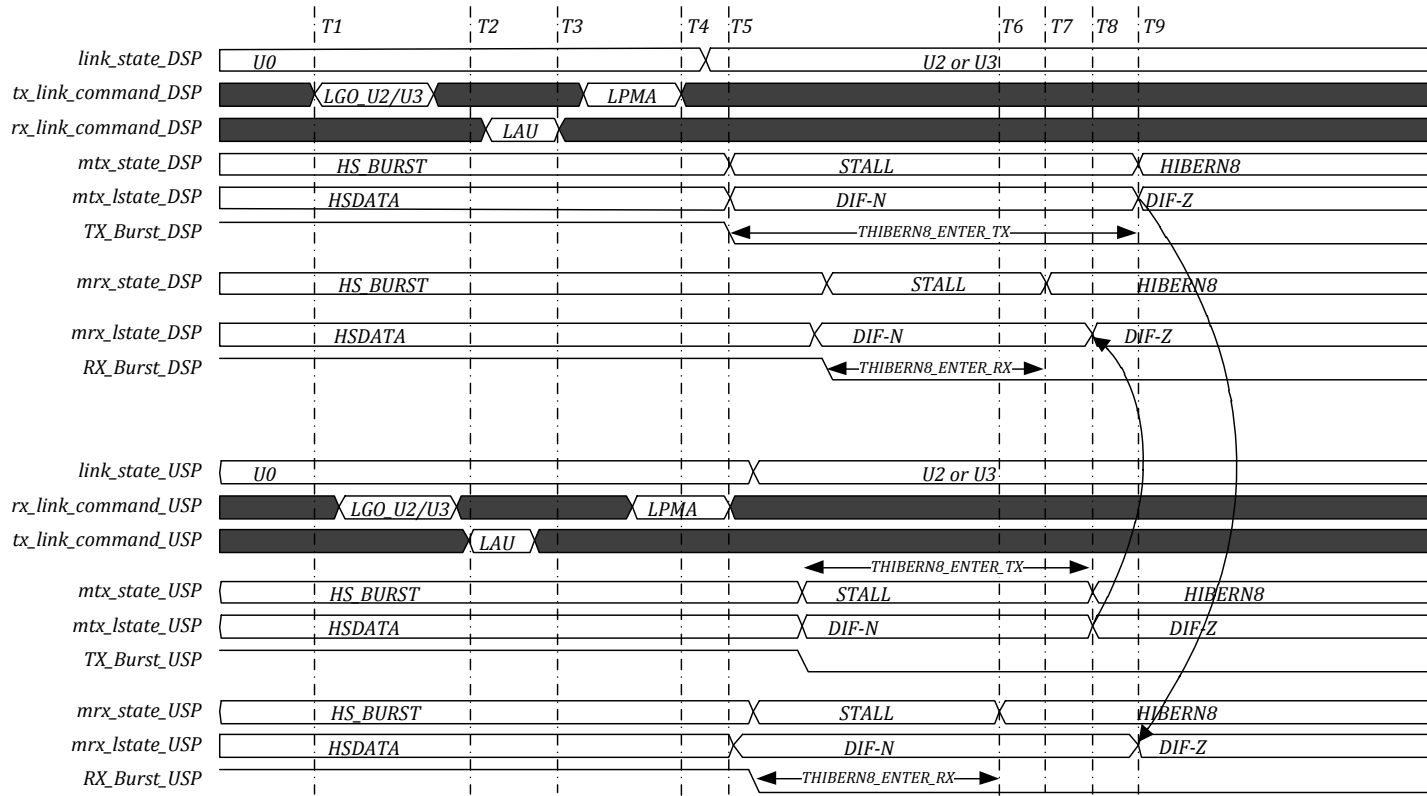
*T3: Both Link partners are in HS\_BURST. Link enters Recovery.Configuration after successful TS1 handshake.*

*T4: Link enters Recovery.Idle after successful TS2 handshake.*

*T5 Link enters U0 after successful LIDLE handshake.*

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7.6 U0 TO U2/U3



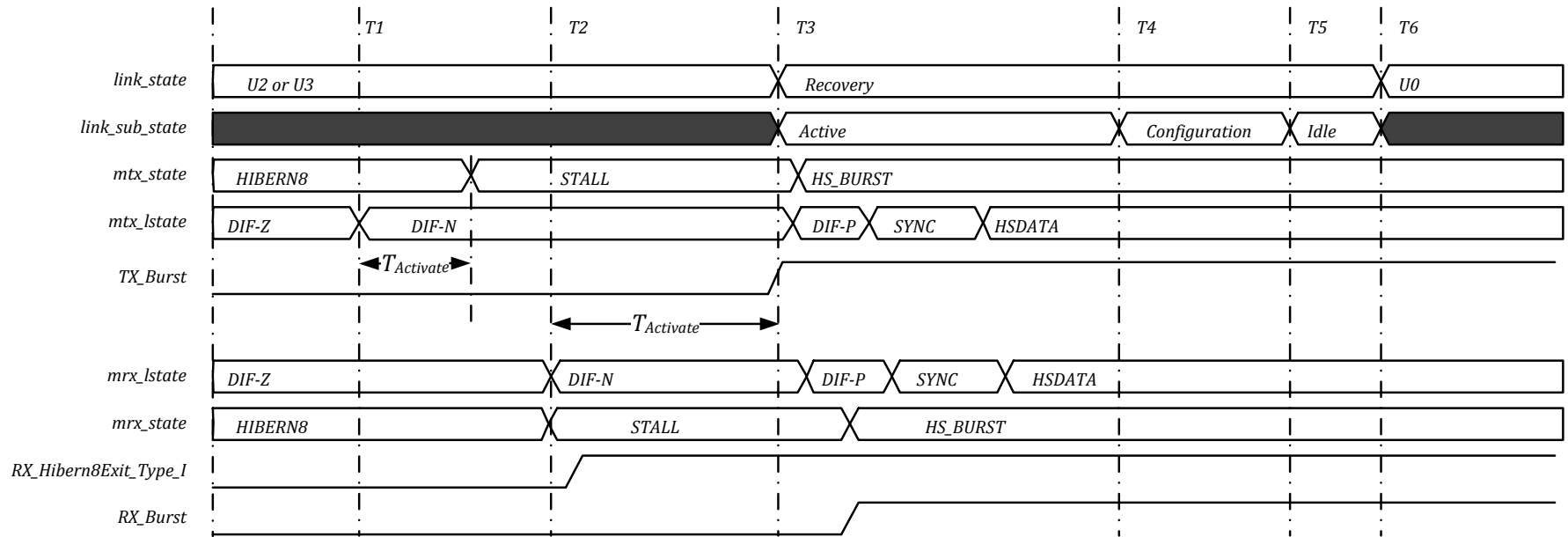
U0 to U2/U3

- T1: DSP send LGO\_U2 or LGO\_U3 and disables STALL entry until it receives LXU or enters into U2/U3 state
- T2: USP accepts low power entry as per section 3.8.4.1 "Exit from U0"
- T3: The DSP, upon receipt of the LAU, configures M-TX and M-RX for HIBERN8 entry and responds with LPMA as per 3.8.4.1 "Exit from U0"
- T4: After sending LPMA, DSP enters into U2/U3 and put it's M-TX into STALL
- T5: After receiving LPMA, USP enters into U2/U3 and put it's M-TX into STALL
- T6: USP M-RX enters into HIBERN8 within THIBERN8\_ENTER\_RX time
- T7: DSP M-RX into HIBERN8 within THIBERN8\_ENTER\_RX time
- T8: USP M-TX enters into HIBERN8 within THIBERN8\_ENTER\_TX time
- T9: DSP M-TX enters into HIBERN8 within THIBERN8\_ENTER\_TX time

Note: In this diagram, U2 entry is initiated by DSP but USP can also initiate U2 entry. However U3 entry can be initiated by DSP only

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### 7.7 U2/U3 TO U0



#### U2/U3 to U0

T1: Link partner 1 initiates U2/U3 exit by making sure that it's M-RX and M-TX is in HIBERN8 for at least Thibern8 time

T2: Link partner 2 detects HIBERN8 exit on it's M-RX and starts HIBERN8 exit on it's M-TX.

T3: Link partner 2 detects STALL exit on it's M-RX and starts STALL exit on it's M-TX.

T4: Both Link partners are in HS\_BURST. Link enters Recovery.Configuration after successful TS1 handshake.

T5: Link enters Recovery.Idle after successful TS2 handshake.

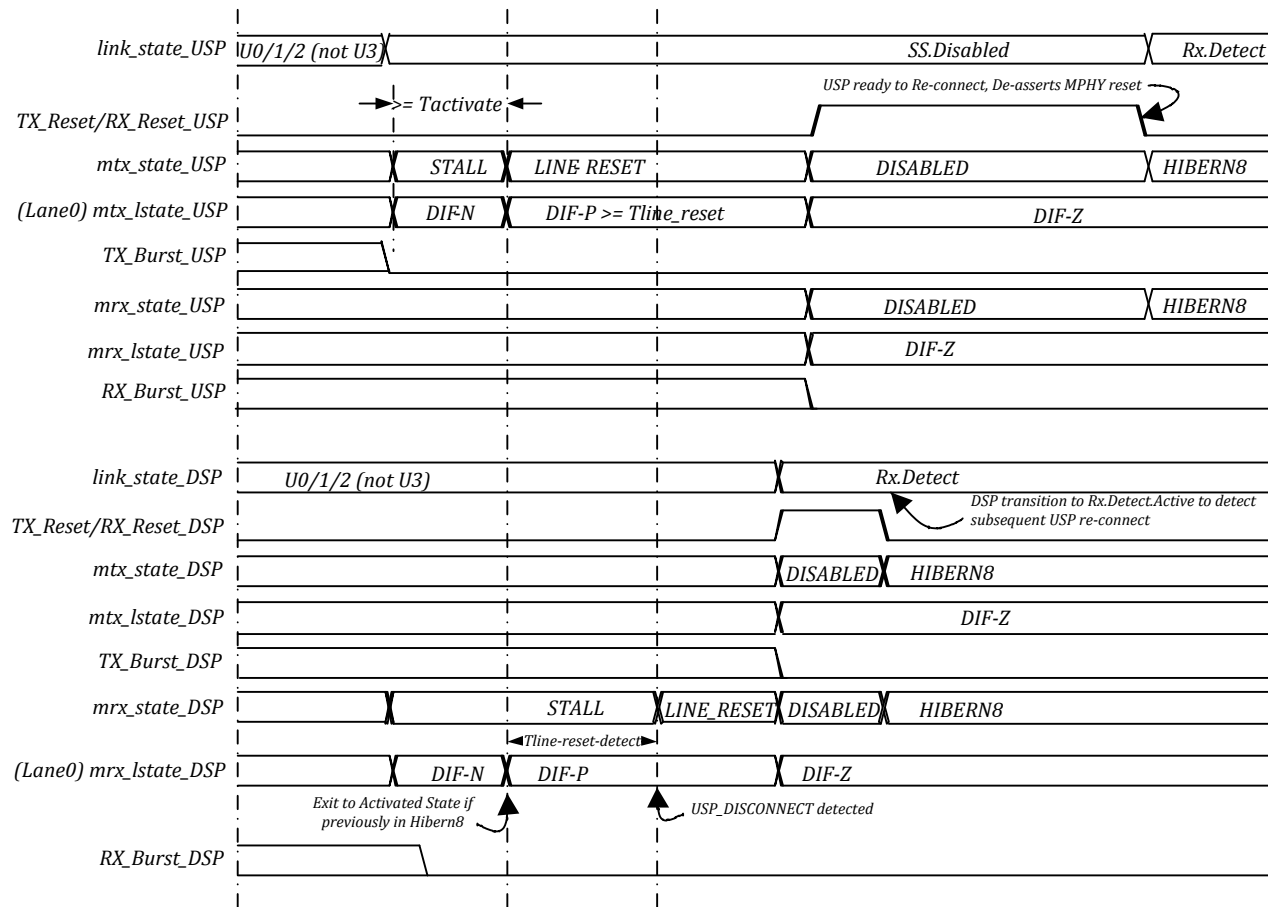
T6 Link enters U0 after successful LIDLE handshake.

Note: TActivate is 100us as per SSIC profile definition

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### 7.8 USP Disconnect



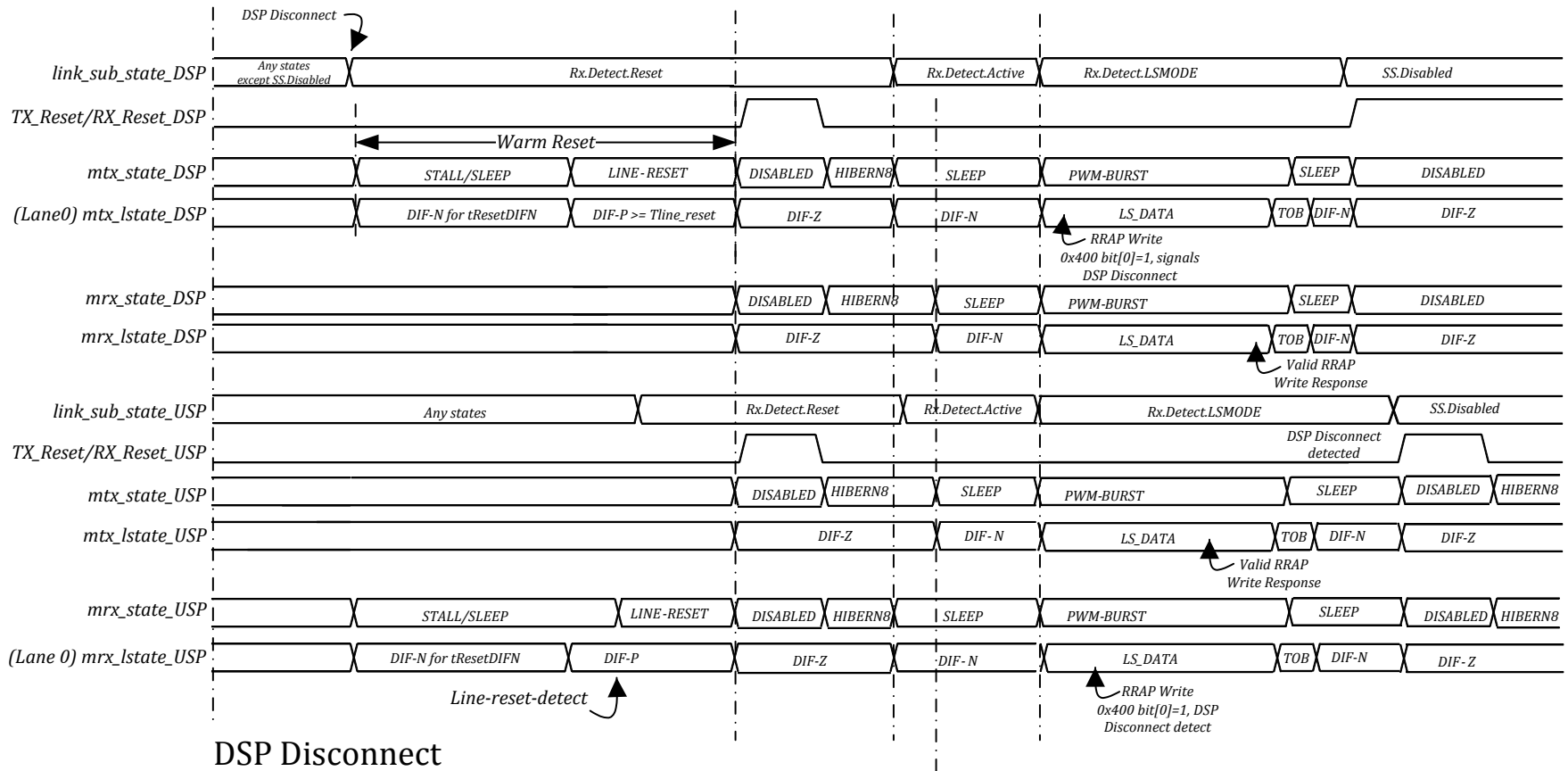
USP Disconnect

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### 7.9 DSP Disconnect



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