USB ENGINEERING CHANGE NOTICE

Title: USB 2.0 DC Resistance

Applies to: Universal Serial Bus Specification, Revision 2.0

Summary of ECN

- Define the maximum series DC resistance (DCR) for D+ and D- in a Cable Assembly
- Define the maximum series DC resistance (DCR) for D+ and D- in high-speed capable Devices
- Define the maximum series DC resistance (DCR) for D+ and D- in high-speed capable Captive Devices
- Add a new compliance test specification for high-speed capable Devices and Hosts to check for “False Connect” and “False Disconnect” events.
- Add a “Silicon Design Guide” to facilitate design of a proper disconnect threshold voltage level (V_{HSDSC}) to avoid “False Connect” and “False Disconnect” events.

Reasons for ECN

The USB2.0 specification doesn’t define the DC resistance (DCR) on the D+ and D- data path between the silicon and the connector. The lack of a DCR requirement in the USB2.0 specification may cause a false disconnect events when high-speed capable USB2 Hosts and Devices are connected. The excessive DCR on the D+ and D- data path may be caused by multiples crossbar switches and/or passive components such as common-mode chokes. A false disconnect event may occur when an high EOP level is present due to 1) a high reflection by high DCR of D+ and D- line and 2) a large output swing (V_{HSOH}) level being required to pass the eye diagram requirement at TP2.

A maximum DCR limit should be defined in the specification along with an appropriate disconnect threshold voltage level in the Host design to ensure the interoperability in the USB2 eco-systems when the maximum DCR channel is present.

Impact on Existing Peripherals and Systems

The DC resistance (DCR) specification for the Cable Assembly is relaxed from 0.6Ohms to 3.5Ohms. No impact on the existing Cable Assembly.

The DC Resistance (DCR) specification for high-speed capable Devices or Captive Devices is new. The impact to the existing Devices or Captive Devices is expected to be small as the maximum DCR limit (20ohms for Device, 23.5ohms for Captive Device) was judiciously estimated to be sufficient for most implementations.

Hardware Implications:

No impact to the Cable Assembly design.

High-speed capable Device designs will have to consider the maximum DCR. Most Devices meet

this requirement now.

High-speed capable Captive Device designs will have to consider the maximum DCR. Most Devices meet this requirement now.

High-speed capable Hosts will need to implement a Disconnect Threshold Voltage (V_{HSDSC}) level which interoperates in the USB2 eco-system with the maximum DCR defined in this ECN. Host designs would have already had to incorporate something similar to pass the USB2 Compliance with higher DCR between the silicon and the connector.

Software Implications:

There are no known software implications.

Compliance Testing Implications:

The following tests shall be added to the compliance test specification.

- Check DCR of Cable Assembly
- Check DCR of high-speed capable Device by performing “false disconnect” test using a calibrated Golden Host
- Check DCR of high-speed capable Captive Device by performing “false disconnect” test using a calibrated Golden Host
- Perform “false disconnect” and “false connect” test for high-speed capable Host using the calibrated load which has the maximum DCR as defined in this ECN.

Specification Changes

(a). Section 6.6.3 Electrical Characteristics

Table 7-1. Description of Functional Elements in the Example Shown in Figure 7-1

From Text:

The DC resistance from plug shell to plug shell (or end of integrated cable) must be less than 0.6 ohms.

To Text:

The DC resistance from plug shell to plug shell (or end of integrated cable) must be less than 3.5 ohms.

(b). Section 7.1.17 Cable Attenuation

From Text:

USB cables must not exceed the loss figures shown in Table 7-6. Between the frequencies called out in the table, the cable loss should be no more than is shown in the accompanying graph.

To Text:

The series DC resistance of D+ or D- in a USB cable shall not exceed 3.5 Ω. USB cables must not exceed the loss figures shown in Table 7-6. Between the frequencies called out in the table, the cable loss should be no more than is shown in the accompanying graph.

(c). Section 7.1, Table 7-1

From Table:

Table 7-1. Description of Functional Elements in the Example Shown in Figure 7-1

Element	Description
Disconnection Envelope Detector	This envelope detector is required in downstream facing ports to detect the high- speed Disconnect state on the line (VHSDSC). Disconnection must be indicated when the amplitude of the differential signal at the downstream facing driver's connector ≥625 mV, and it must not be indicated when the signal amplitude is ≤525 mV. The output of this detector is sampled at a specific time during the transmission of the high-speed SOF EOP, as described in Section 7.1.7.3.
Pull-up Resistor (RPU)	This resistor is required only in upstream facing transceivers and is used to indicate signaling speed capability. A high-speed capable device is required to initially attach as a full-speed device and must transition to high-speed as described in this specification. Once operating in high-speed, the 1.5 kΩ resistor must be electrically removed from the circuit. In Figure 7-1, a control

	line called RPU_Enable is indicated for this purpose. The preferred embodiment is to attach matched switching devices to both the D+ and D- lines so as to keep the lines' parasitic loading balanced, even though a pull-up resistor must never be used on the D- line of an upstream facing high-speed capable transceiver. When connected, this pull-up must meet all the specifications called out for full- speed operation.
Pull-down Resistor (RPD)	These resistors are required only in downstream facing transceivers and must conform to the same specifications called out for low-speed and full-speed operation.

To Table:

Table 7-1. Description of Functional Elements in the Example Shown in Figure 7-1

Element	Description
Disconnection Envelope Detector	This envelope detector is required in downstream facing ports to detect the high- speed Disconnect state on the line (VHSDSC). ~~Disconnection must be indicated when the amplitude of the differential signal at the downstream facing driver's connector ≥625 mV, and it must not be indicated when the signal amplitude is ≤525 mV.~~ A downstream facing transceiver operating in high-speed mode shall implement a proper disconnect threshold voltage (V_{HSDSC}) level to ensure the interoperability in the USB2 eco-systems with the maximum DCR channel defined in the specification. Silicon design guide for Disconnect Threshold Voltage (V_{HSDSC}) implementation is shown in Figure 7-new. The output of this detector is sampled at a specific time during the transmission of the high-speed SOF EOP, as described in Section 7.1.7.3.
Pull-up Resistor (RPU)	This resistor is required only in upstream facing transceivers and is used to indicate signaling speed capability. A high-speed capable device is required to initially attach as a full-speed device and must transition to high-speed as described in this specification. Once operating in high-speed, the 1.5 kΩ resistor must be electrically removed from the circuit. In Figure 7-1, a control line called RPU_Enable is indicated for this purpose. The preferred embodiment is to attach matched switching devices to both the D+ and D- lines so as to keep the lines' parasitic loading balanced, even though a pull-up resistor must never be used on the D- line of an upstream facing high-speed capable transceiver. When connected, this pull-up must meet all the specifications called out for full- speed operation.
Pull-down Resistor (RPD)	These resistors are required only in downstream facing transceivers and must conform to the same specifications called out for low-speed and full-speed operation.
DC Resistance (D+, D-)	The series DC resistance of D+ and D- line shall be equal or less than 19 Ω for a high-speed capable device, equal or less than 25 Ω for a high-speed capable captive device. * Please refer "USB Type-C Specification" for the maximum series DC resistance of D+ and D- lines of Type-C Device and Type-C Captive Device.

(d). Section 7.3.2, Table 7-12

New row:

Table 7-12. Cable Characteristics (Note 14)

Parameter	Symbol	Conditions	Min	Max	Units
Cable DCR (D+, D-)				3.5	Ω

(e). Section 7.1.7.3 Connect and Disconnect Signaling

From Text:

A downstream facing transceiver operating in high-speed mode detects disconnection of a high-speed device by sensing the doubling in differential signal amplitude across the D+ and D- lines that can occur when the device terminations are removed. The Disconnection Envelope Detector output goes high when the downstream facing transceiver transmits and positive reflections from the open line return with a phase which is additive with the transceiver driver signal. Signals with differential amplitudes ≥ 625 mV must reliably activate the Disconnection Envelope Detector. Signals with differential amplitudes ≤ 525 mV must never activate the Disconnection Envelope Detector.

To Text:

A downstream facing transceiver operating in high-speed mode detects disconnection of a high-speed device by sensing the doubling in differential signal amplitude across the D+ and D- lines that can occur when the device terminations are removed. The Disconnection Envelope Detector output goes high when the downstream facing transceiver transmits and positive reflections from the open line return with a phase which is additive with the transceiver driver signal. ~~Signals with differential amplitudes ≥ 625 mV must reliably activate the Disconnection Envelope Detector. Signals with differential amplitudes ≤ 525 mV must never activate the Disconnection Envelope Detector~~. A downstream facing transceiver operating in high-speed mode shall implement a proper disconnect threshold voltage (V_{HSDSC}) level to ensure the interoperability in the USB2 eco-systems with the maximum DCR channel defined in the specification. Silicon design guide for Disconnect Threshold Voltage (V_{HSDSC}) implementation is shown in Figure 7-new.

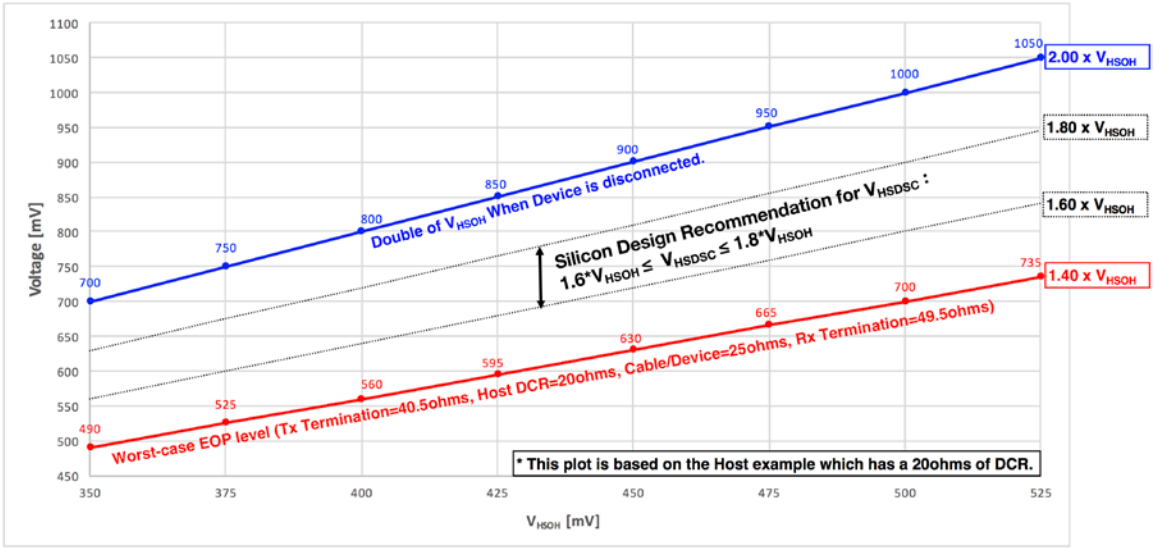

Figure 7-new. Silicon Design Guide for Disconnect Threshold Voltage (V_{HSDSC}) Implementation

(f). Section 7.3.2, Table 7-7

From Table:

Table 7-7. DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Max.	Units
High speed disconnect detection threshold (differential signal amplitude)	VHSDSC	Section 7.1.7.2 (specification refers to differential signal amplitude)	525	625	mV

To Table:

Table 7-7. DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Max.	Units
High speed disconnect detection threshold (differential signal amplitude)	VHSDSC	Section 7.1.7.2 (specification refers to differential signal amplitude)	525	~~625~~Refer Silicon Design Guide for Disconnect Threshold Voltage (VHSDSC) Implementation in Figure 7-new	mV

(g). Section 7.1.4.2

From Text:

In the case of a downstream facing port, a high-speed capable transceiver must include a differential envelope detector that indicates when the signal on the data exceeds the high-speed Disconnect level (VHSDSC) as defined in Table 7-3. (The detector must not indicate that the disconnection threshold has been exceeded if the differential signal amplitude is ≤525 mV, and must indicate that the threshold has been exceeded if the differential signal amplitude is ≥625 mV.)

To Text:

In the case of a downstream facing port, a high-speed capable transceiver must include a differential envelope detector that indicates when the signal on the data exceeds the high-speed Disconnect level (VHSDSC) as defined in Table 7-3. ~~(The detector must not indicate that the disconnection threshold has been exceeded if the differential signal amplitude is ≤525 mV, and must indicate that the threshold has been exceeded if the differential signal amplitude is ≥625 mV.)~~ A downstream facing port operating in high-speed mode shall implement a proper disconnect threshold voltage (V_{HSDSC}) level to ensure the interoperability in the USB2 eco-systems with the maximum DCR channel defined in the specification. Silicon design guide for Disconnect Threshold Voltage (V_{HSDSC}) implementation is shown in Figure 7-new.

(h). Section 7.1.7.2, Table 7-3

From Table:

High-speed Disconnect State (at downstream facing port)	**NA**	**VHSDSC - Downstream facing port must not indicate device disconnection if differential voltage is ≤ 525 mV, and must indicate device disconnection when magnitude of differential voltage is ≥ 625 mV, at the sample time discussed in Section 7.1.7.3.**

To Table:

High-speed Disconnect State (at downstream facing port)	**NA**	**VHSDSC - ~~Downstream facing port must not indicate device disconnection if differential voltage is ≤ 525 mV, and must indicate device disconnection when magnitude of differential voltage is ≥ 625 mV, at the sample time discussed in Section 7.1.7.3.~~ A downstream**

		facing port operating in high-speed mode shall implement a proper disconnect threshold voltage (V_{HSDSC}) level to ensure the interoperability in the USB2 eco-systems with the maximum DCR channel defined in the specification. Silicon design guide for Disconnect Threshold Voltage (V_{HSDSC}) implementation is shown in Figure 7-new.