USB 3.2 ENGINEERING CHANGE NOTICE

Title: BLR Gen1 $SSC_{df/dt}$ Clock Switch Limit
Applied to: USB 3.2_r1.0 Sep. 22, 2017

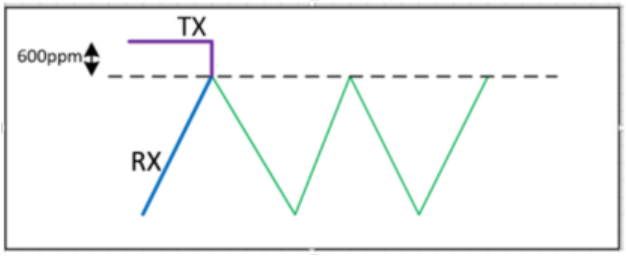
Brief description of the functional changes proposed:

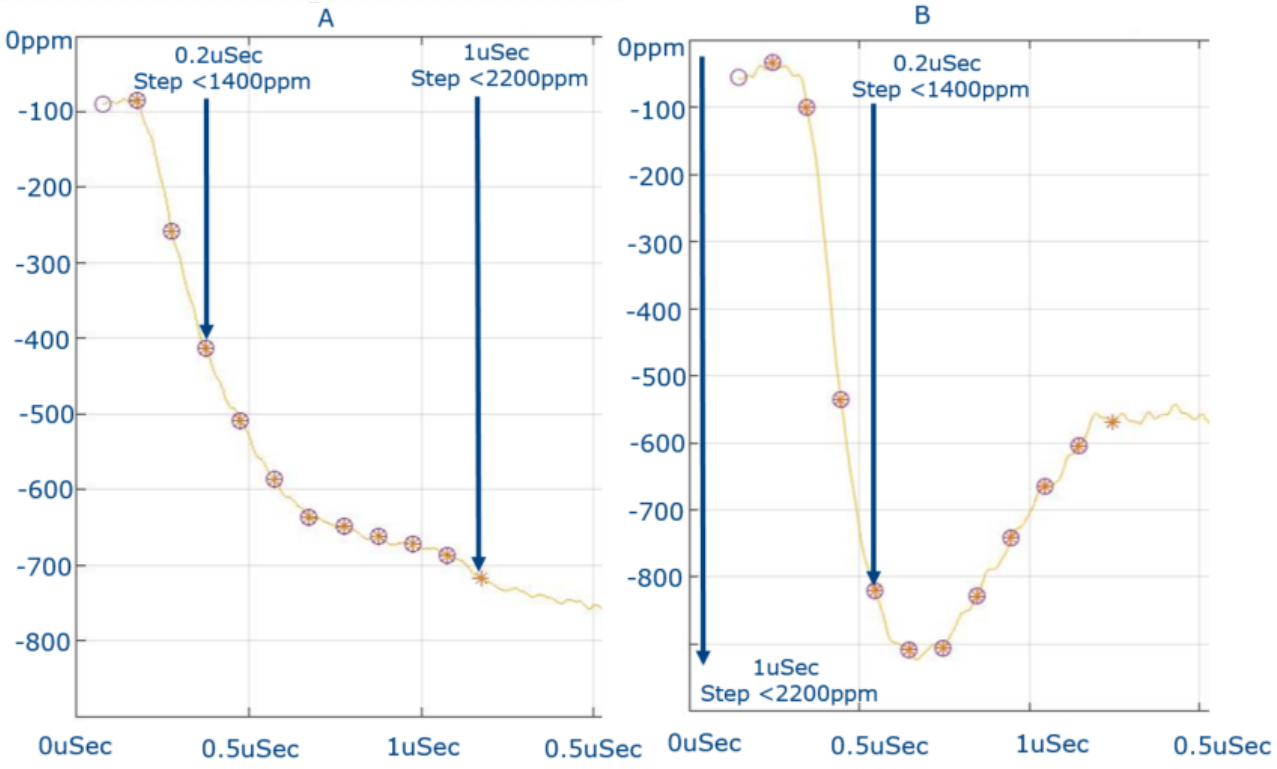
Currently USB Table 6-18 contains the following two requirements:

- Symbol period tolerance +/-300ppm
- Gen1- $t_{CDR\_SLEW\_MAX}$ 10mS/S max slew rate
- Gen2 - Maximal frequency slope 1250 ppm/uSec

It is difficult for devices to comply with the SSCdf/dt in Gen1 or Gen2 for the frequency change during the switch point. There is a need to limit the frequency step slope during switching point. These limits are outside the base spec limits but are believed to not create interoperability problems.

We suggest to modify/add requirement for steady state in Gen1 and for the clock switching period in Gen1 and Gen2. Example: When Re-timer Transmitter frequency has +300ppm offset and it switches to received SSC frequency that has -300ppm offset. Example of maximum frequency Delta at switch point and possible post switch tracking results:





One other change is to update SSC profile to remove the SSC profile previously specified for WiMax friendly radio.

Benefits as a result of the proposed changes:

The key requirement from the frequency transition should be such that enable to keep the next stage receiver CDR tracking without losing lock.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

During the Re-timer clock switch period there is no data transfer yet as Re-timer is sending locally generated or forwarded TS1B which are regarded as corrupted by Host/Device and there is no need to keep error free frequency tracking. At this stage the requirement is Informative.

Summary of current implementations from Re-timer Summit and USB-IF Compliance Workshop #112:

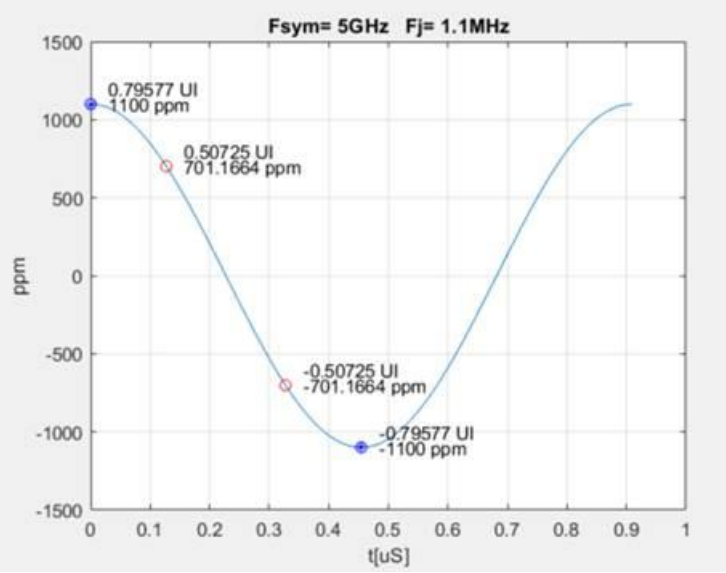
Tx Results Clock Switch SSCdf_dt:

Event/Vendor [ppm/us]	**1**	**2**	**4**	**5**	**6**	**7**
Test event 1	1152.8	845.3	N/A	N/A	N/A	N/A
Test event 2	1263	1209	N/A	N/A	N/A	N/A
Test event 3	N/A	N/A	585.7	1172.9	1184.2	1360.6

Rx Results from USB-IF Compliance Workshop #112:
All vendors passed JTOL Gen1 with **good** margin.

Functional Results from IOP #2:
No issues sighted with single and 4 cascaded Re-timer with Gen1 Devices with overall 500 link bring up events.

Pj stress method results with legacy Gen1 Devices:
# of tested devices – 10 from 5 certified vendors
Test method:
In order to verify that the receiver can tolerate the Transmitter new frequency transition specification, we suggest to inject a signal with predefined jitter that will emulate similar frequency transition as allowed by this change. The jitter pattern is sinusoidal with rate 1.1MHz and deviation 1.6UI ptp



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An analysis of the hardware implications:
Designs in compliance to this ECR only ensure maximum interoperability although not guaranteed.

An analysis of the software implications:
None.

An analysis of the compliance testing implications:
Compliance methodology and tools will be updated for this measurement as part of ecosystem assessment. DUT who will comply with this ECR and all required test specification metrics will be granted certification and ensure maximum interoperability. DUT who fail this ECR will be noted as increased risk of legacy interoperability.

Actual Change

(a). From Text : Add to section E.3.4.4.1

- Upon declaring successful receiver training, a bit-level re-timer shall perform one of the following.
    - If it has detected TS1 OS or TS1B OS at one simplex link, it shall perform the clock switching at its other simplex link and comply with the electrical and timing requirements defined in Chapter 6, specifically in terms of tCDR_SLEW_MAX for Gen 1 operation, and SSCdfdt for Gen 2 operation. It shall continue the TS1A OS transmission at both ports. Note that a bit-level re-timer may receive TS1 OS and/or TS1B OS at both ports. Under this situation, a bit-level re-timer shall perform the clock switching at both simplex links.

      Note that a bit-level re-timer may monitor the clock offset between the recovered clock and its local reference clock, and attempt to perform the clock switching when the clock offset is small. A bit-level re-timer shall expect that the frequency range of a host or device is either within +300ppm to −5300ppm, or within −1700ppm to −5300ppm if a RF-friendly SSC profile is employed. It is desired that a bit-level re-timer to monitor the recovered clock and determine its frequency range before setting the clock switching point.
    - If it has detected TS1A OS, it shall continue the TS1A OS transmission while waiting for incoming TS1 OS or TS1B OS.

(a). To Text :

- Upon declaring successful receiver training, a bit-level re-timer shall perform one of the following.
    - If it has detected TS1 OS or TS1B OS at one simplex link, it shall perform the clock switching at its other simplex link and comply with the electrical and timing requirements defined in Chapter 6~~., specifically in terms of tCDR_SLEW_MAX for Gen 1 operation, and SSCdfdt for Gen 2 operation.~~ It shall continue the TS1A OS transmission at both ports. Note that a bit-level re-timer may receive TS1 OS and/or TS1B OS at both ports. Under this situation, a bit-level re-timer shall perform the clock switching at both simplex links.
    - ~~Note that a bit-level re-timer may monitor the clock offset between the recovered clock and its local reference clock, and attempt to perform the clock switching when the clock offset is small. A bit-level re-timer shall expect that the frequency range of a host or device is either within +300ppm to −5300ppm, or within −1700ppm to −5300ppm if a RF-friendly SSC profile is employed. It is desired that a bit-level re-timer to monitor the recovered clock and determine its frequency range before setting the clock switching point.~~
    - If it has detected TS1A OS, it shall continue the TS1A OS transmission while waiting for incoming TS1 OS or TS1B OS.

- During the clock switching, a bit-level re-timer shall attempt to minimize the frequency jump when switching from its transmit clock based on the local reference clock to the transmit clock based on the recovered clock. This is to maximally ensure its following link partner to maintain its CDR lock during the clock switching. A bit-

level re-timer shall comply with the short-term SSCdf/dt clock switching requirement specified in **TBD Table E-x**.

Table E-x. Bit-Level Re-timer Short-Term Clock Switching Requirement [1]

	Frequency_offset (ppm)	Time interval (us)	Comments
SSCdf/dt_A[2]	< 1400	0.2	waveform under test is defined as window of switching_point (+/-) *0.5/ $t_{SSC\_MOD\_RATE}$
SSCdf/dt_B[2]	< 2200	1.0	

Note [1]. The requirements are outside the specification defined **Table 6-18.** Thus interoperability may not be formally guaranteed but are strongly believed to be adequate.

Note [2]. Refer to TBD Figure X for SSCdf/dt_A and SSCdf/dt_B definition.

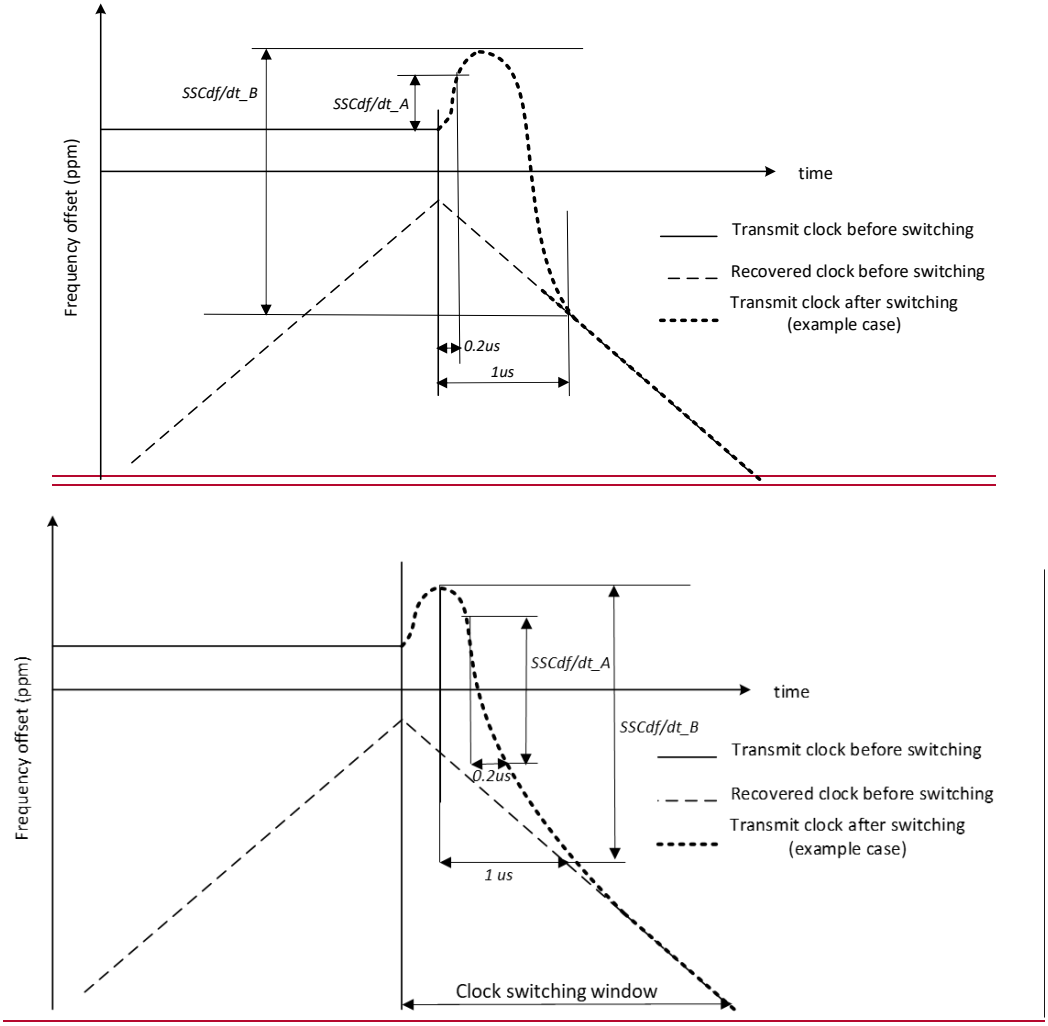

Figure E-X: Definition of SSCdf/dt_A and SSCdf/dt_B